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2	Presence of Ethics committee	https://naac.tkrcet.com/NAAC/wp-content/uploads/2023/03/ethics_merged.pdf
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11

FinFET Process Technology for RF and Millimeter Wave Applications

A. Theja[1]*, Vikas A.[1], Meena Panchore[1] and Kanchan Cecil[2]*

[1]Department of Electronics and Communication Engineering, National Institute of Technology Patna, Bihar, India
[2]Department of Electronics and Telecommunication Engineering, Jabalpur Engineering College, Jabalpur, Madhya Pradesh, India

Abstract

FinFETs are considered as a potential candidate for modern complementary-metal-oxide-semiconductor (CMOS) technology due to reduced short channel effects (SCEs) and better gate controllability over channel. However, with the downscaling of device dimensions, the RF performance at higher current levels is degraded. Therefore, in this chapter, we have presented the scaling effects on RF performance of Fin devices including the parasitic and noise components. This chapter also focused the impact of self-heating and temporal process variability on electrical performance of Fin devices.

***Keywords*:** Fin, scaling, self-heating effect, RF performance, millimeter-wave (mm-Wave)

11.1 Evaluation of FinFET Technology

In planar CMOS transistors, the speed of the device has been increased due to scaling of device dimension. However, the device scaling at sub-micrometer deteriorates the electrical characteristic and affects the analog and RF performance at circuit level. Hence, FinFET is considered as a potential candidate to overcome the limitations of planar devices at sub-nanometer regime. This section briefly covers the limitations of planar bulk CMOS

**Corresponding author*: at.phd20.ec@nitp.ac.in

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transistor over FinFET technology and explains the optimization techniques at millimeter wave applications. Further, the fabrication steps are discussed to build FinFET structure at sub-micrometer node.

Figure 11.1 shows the cross-sectional view of FinFET device. Here, the FinFET gate covers a thin cut of pure silicon, referred as a "fin", and current flows from one end of the fin to the other [1]. The gate controls over the channel, thus avoiding leakage currents and reduces Short Channel Effects (SCEs). The reduced SCE leads to higher intrinsic gain and lower leakage current in the OFF-state condition. The current flows on three facets [2] of the fin, therefore, the equivalent channel width(W) is equal to the sum of width of fin (W_F) and twice of its height (H_F) i.e. $W = W_F + 2H_F$. Typically, width and height are 6 nm and 50 nm respectively. Since, the height of the fin, H_F is not under control of circuit designer, it appears that the width of fin, W_F can be selected such that $W_F + 2H_F$ yields the desired transistor width. However, the width of the fin affects the device characteristics such as drain/source series resistance and channel length modulation. Due to this reason, the width of the fin is also fixed leading discrete values for the width of the transistor. For example, if $W = W_F + 2H_F = 120$nm, then broader transistors can be obtained by increasing the number of fins.

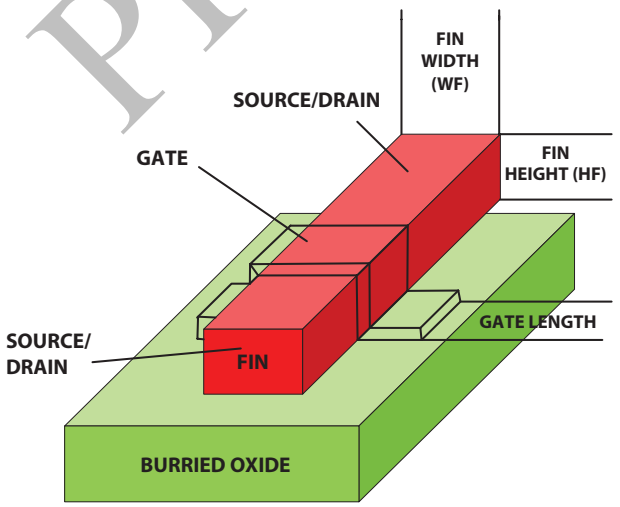

Figure 11.1 Cross sectional view of FinFET.

11.1.1 Steps of Fabrication and Process Flow of FinFET Technology

To understand the device performance of FinFET due to process variations, this section presents the simplified process flow of a FinFET technology as depicted in Figures 11.2 and 11.3. The important steps involved in the fabrication are as follows:

The process starts with the formation of fin and it is done using optical lithography followed by plasma etching. The choice of thickness for the spacer is crucial, as it determines the width of the final fin. After etching process, the sidewalls becomes rough, therefore the process of oxidation and H_2 annealing are performed for the smoothness of the sidewall surfaces. After that, the gate dielectric is developed and then the metal gate is grown. It is preferred to select the V_{th} of the device by using a material (which can also be used to form a gate) that has the appropriate work function instead of doping the channel like in planar MOSFETs. In FinFETs, the channel is usually lightly doped or undoped to suppress SCE, hence,

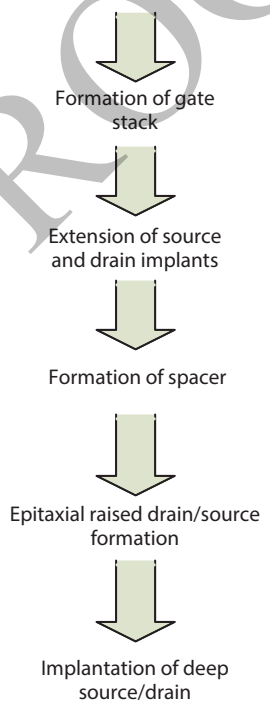

Figure 11.2 Steps involved in fabrication of FinFET technology.

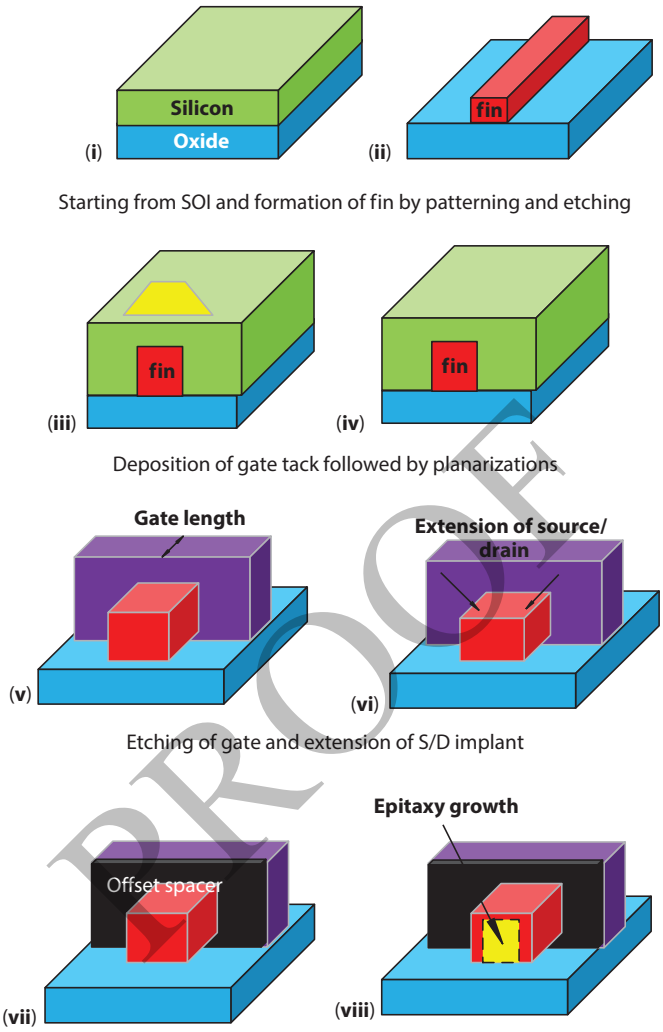

Figure 11.3 Process flow of FinFET technology [4].

the V_{th} is tuned with the help of gate work function. Next step is the gate stacking over the fin, while depositing the gate material. After this step, planarization of the Gate stack is done, so that, the gate etching can be performed. In this etching process, the gate must have a high selectivity to prevent the damage of fin. After this, S/D extensions are developed by

using an implantation. Later, source/drain offset spacers are established along the sidewalls of the fin as well as gate.

11.1.2 Digital Performance

In this section, the digital performance metrics like intrinsic transistor performance (ITP), threshold voltage (V_{TH}) and subthreshold slope (SS) at different High-K gate dielectric [3] of planner MOSFET and FinFET are discussed.

Figure 11.4 shows the ITP of both devices in terms of I_{ON}/I_{OFF} ratio at different High-K dielectric materials. Here, I_{ON} defined as the saturation current, and I_{OFF} represented as the total leakage current, which is the combination of junction leakage, gate leakage and subthreshold leakage currents. By observing the ITP curve, we can say that the planar bulk transistors with SiON dielectric exhibit large OFF-state current as compared to planar MOSFETs with High-K dielectric. The high OFF-state current in planar bulk devices is because of the gate leakage through the SiON dielectric. This also reduces the maximum drive current due to mobility degradation. On the contrary, in FinFETs, the leakage current reduces due to the presence of buried oxide (BOX) layer and enhances drive current due to strong control of gate over channel.

Figure 11.5 shows the comparison of threshold voltage (V_{TH}) of both the devices in saturation region. As observed from the figure, FinFETs exhibit

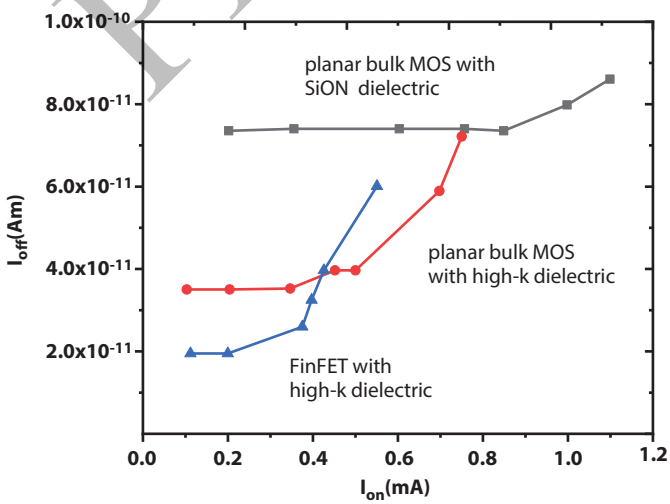

Figure 11.4 ITP performance of FinFETs and planar MOSFETs.

lowered values of V_{TH} (~0.2–0.4 V) compared to bulk planar MOSFETs, which is significant for lower technology nodes. The reduction in V_{TH} of FinFETs is due to the existence of BOX layer and the undoped nature of the fins, which further reduces the voltage drop across the semiconductor,

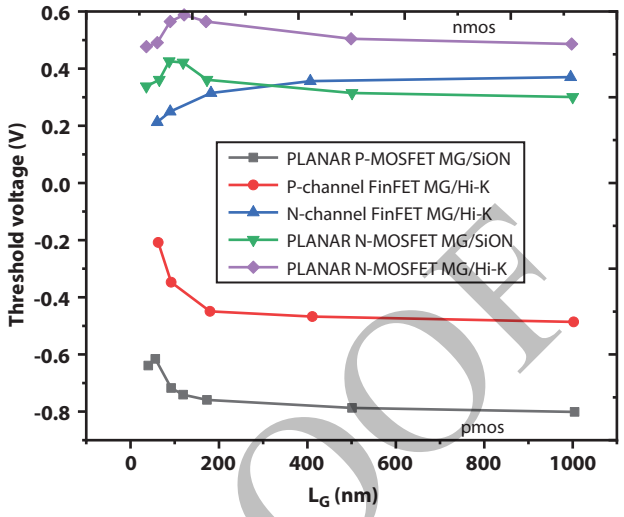

Figure 11.5 Threshold voltage of FinFET and planar MOSFET at different High-K gate dielectric.

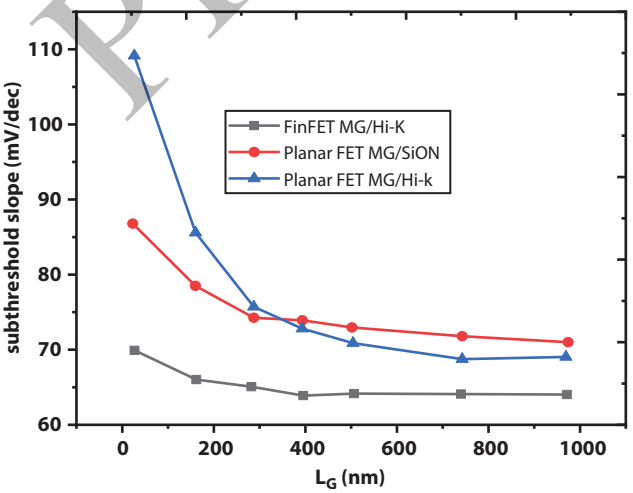

Figure 11.6 Subthreshold slope of FinFET and planar MOSFET at different High-K gate dielectrics.

hence the V_{TH}. Further, the FinFET shows excellent performance in terms of SS which is less than 70 mV/decade as compared to the planar MOSFETs as shown in Figure 11.6.

11.1.3 Analog/RF Performance

In this section, the Analog/RF performance figure of merits (FOMs) like transconductance (G_m), voltage gain (A_V), Output conductance (G_{DS}) and cut-off frequency (f_T) of FinFET as well as planar MOSFET are discussed at different High-k gate dielectrics. Figure 11.7 shows the G_m variations with respect to the physical gate length of both the devices. It has been observed that the transconductance of FinFET and planar MOSFET are similar till $V_{GS} - V_T = 0.3$ V.

After $V_{GS} - V_T = 0.3$ V, the transconductance of the FinFET decreases as compared to that of the planar MOSFET due to the high series resistance of FinFET which reduces the drive current and hence transconductance.

The comparison of output conductance (G_{DS}) of FinFETs as well as of Planar MOSFET is shown in Figure 11.8. It is observed that the FinFETs exhibit reduced output conductance than planar MOSFETs. This is because the FinFET is completely depleted due to the limited fin width and the control of the gate over the channel. Hence, increasing the voltage at the drain, more than the pinch-off voltage, does not deplete the body further. As a result, the channel length modulation, which occurs due to the reduction in the channel length on account of the expansion of the depletion region

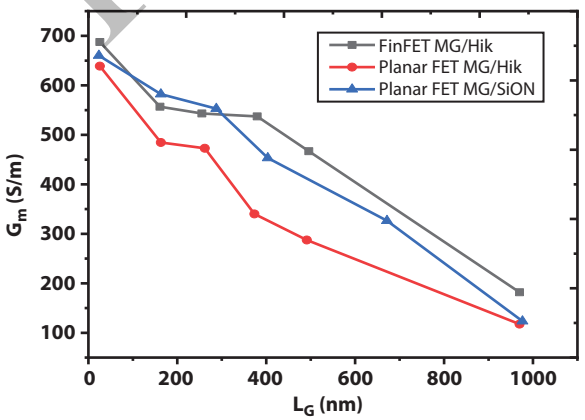

Figure 11.7 Transconductance of FinFET and planar MOSFET at different High-K gate dielectrics.

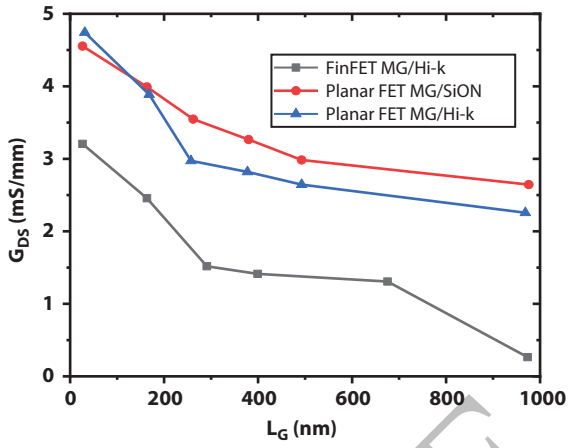

Figure 11.8 Output conductance of FinFET and planar MOSFET at different High-K gate dielectrics.

at the drain, is low. Therefore, the change in drain current with respect to drain voltage, which represents the output conductance is also low.

Figure 11.9 shows the voltage gain (A_V) of FinFET and the planar MOSFET at different High-k gate dielectrics, which is given by the ratio G_m/G_{DS}. FinFET shows higher voltage gain due to high transconductance and low output conductance as compared to the planar bulk MOSFETs.

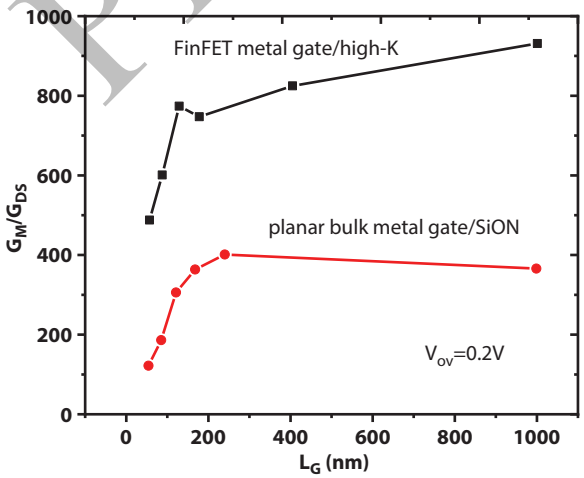

Figure 11.9 Voltage gain of FinFET and planar MOSFET at different High-K gate dielectrics.

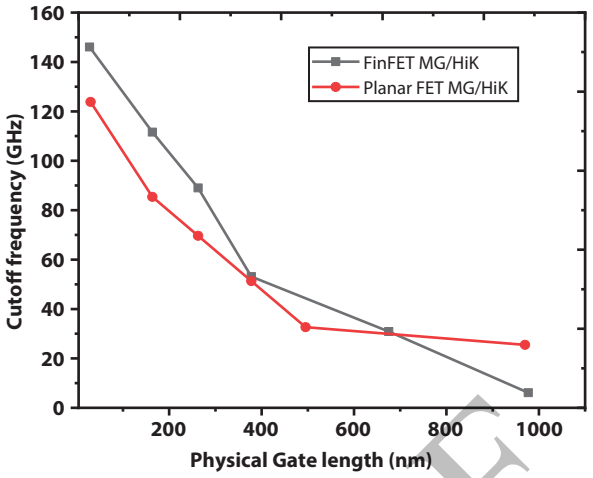

Figure 11.10 Cut-off frequency of FinFET and planar MOSFET at different High-K gate dielectrics.

This is a significant advantage of FinFET over the planar MOSFET for RF circuit applications.

Another parameter that determines the high-frequency performance is the cutoff frequency f_T (= $G_m/2\pi C_{GS}$), which is shown in Figure 11.10. FinFETs and planar MOSFETs exhibits comparable cut-off frequencies because both the devices are having similar values of capacitance (C_{GS}) and transconductance. For analog applications, the other important parameters to be considered are linearity and noise. It has been observed in FinFETs that there is no severe deterioration either in linearity or noise with respect to planar MOSFETs. Therefore, it can be concluded that for analog/RF design, FinFETs exhibit similar value of cut-off frequency and large voltage gain as compared to planar MOSFETs with same linearity and noise levels.

11.2 Distinct Properties of FinFET

In recent time, the requirement of Nanoscale devices with enhanced performance is essential than the conventional CMOS devices. It has been observed that the new emerging devices with add-on features are more suitable for RF/mm-Wave applications. Hence, this section briefly describes some unique properties of FinFET technology which makes it suitable for RF/mm-Wave applications.

11.2.1 Performance with Transistor Scaling

For the past five decades, Moore's law has been sustained through the frequent reduction of transistor channel length which in turn increased transistor density and performance. In the case of planar bulk MOSFETs, the performance improvements have reached saturation level at lower technology nodes, forcing the semiconductor industry to shift from planar to tri-gate structures [5]. The shorter channel length of the transistor leads to the higher transconductance (g_m) scaled by the square of channel length (L^2) and the lower gate capacitance, thus higher unity gain frequency (f_T). However, as the channel length is decreasing day by day, the transistor performance improvement trend has been significantly disturbed. The two major causes for this are velocity saturation and drain induced barrier lowering (DIBL) effect [6].

When gate length is reduced, i.e. the device scales to an utmost level, the source and drain start to interact more through the region below the channel despite of gate potential, and the gate control of the device is reduced. This effect is called short channel effect degradation, and the parameter used to measure this is DIBL. In an ideal device, the potential barrier in the channel is supposed to be lowered only through the gate, which is valid for long channel devices. But this assumption is no longer applicable in case of short channel devices. In FinFETs, the tangential electric field produced at the drain is more strongly screened from the source end of the channel due to closeness of the channel to the second gate, results in suppressed SCEs in particular, better subthreshold swing (SS) and reduced DIBL.

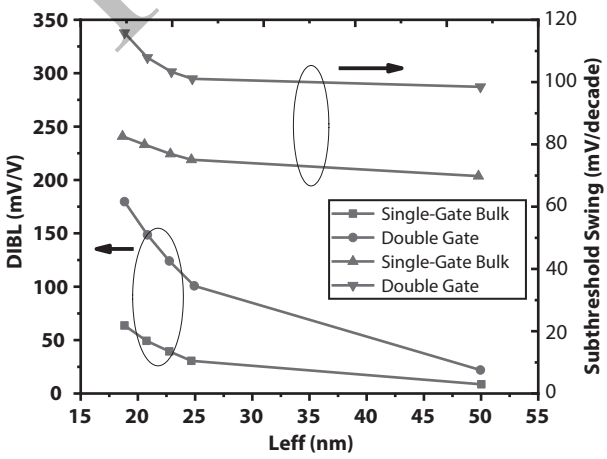

Figure 11.11 DIBL and subthreshold swing of DG and planar MOSFETs.

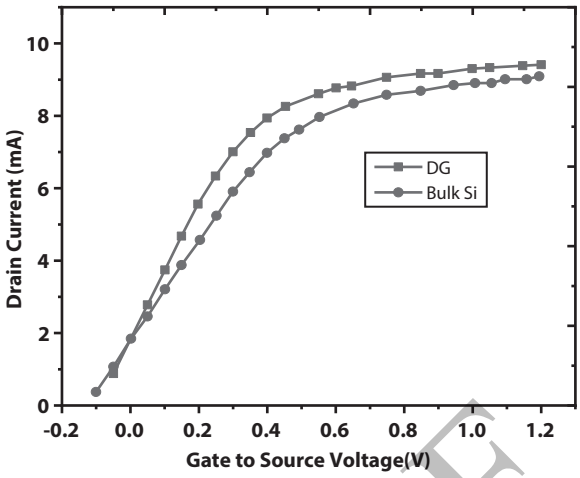

Figure 11.12 Transfer characteristics of DG and planar MOSFETs.

Figure 11.11 shows the Subthreshold swing and DIBL of planar MOSFETs and Double Gate (DG) devices with respect to the effective gate length. It can be observed that both the subthreshold swing and DIBL of the DG devices are significantly enhanced compared to planar MOSFETs.

In planar bulk MOSFETs, DIBL can be reduced by increasing the doping concentration of the body. This in turn also improves the subthreshold swing, thereby desiring higher V_{th} to maintain the low subthreshold current. On the other hand, reducing the doping concentration of body could enhance the subthreshold swing but degrade DIBL. Thus, a compromise is needed for the design of planar MOSFETs.

The transfer characteristics (I_{DS}–V_{GS} curves) of DG and planar MOSFETs are shown in Figure 11.12. From the characteristics, it can be observed that DG-FET has lower threshold voltage for a given off current due to the advantage of gate coupling as discussed earlier. As a result, FinFETs attain large drive currents at reduced power-supply voltages compared to bulk MOSFETs.

11.2.2 Nonlinear Gate Resistance by Three Dimensional Structure

Unlike the bulk MOSFETs, gate resistance of FinFET exhibits a non-linear relationship with respect to channel width. The FinFET has a 3-D channel (known as fin) is wrapped around by the gate. Figure 11.13 shows the three dimensional structure of FinFET. One can analyze from the figure that the

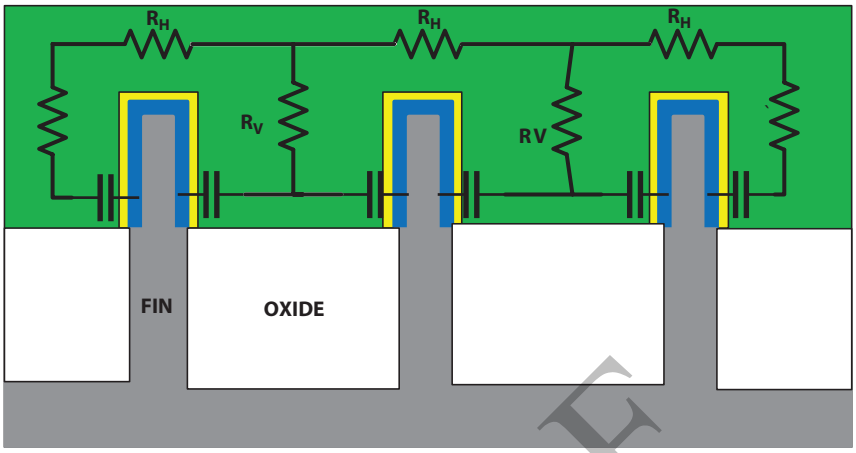

Figure 11.13 Three-dimensional channel of FinFET showing vertical (R_V) and horizontal (R_H) gate resistance components.

gate resistance in FinFET has two components namely, vertical resistance and horizontal resistance [7].

The decomposition of resistance components of FinFET technology is shown in Figure 11.14. The contact resistance R_1 represents the resistance at the edge of the gate material to the metal interface. The combination of R_2 and R_3 is represented by the vertical resistance R_V and the effective R_4 represents open-end resistance. The parallel connection of R_5 and R_6 is represented by the horizontal resistance R_H. The total equivalent gate

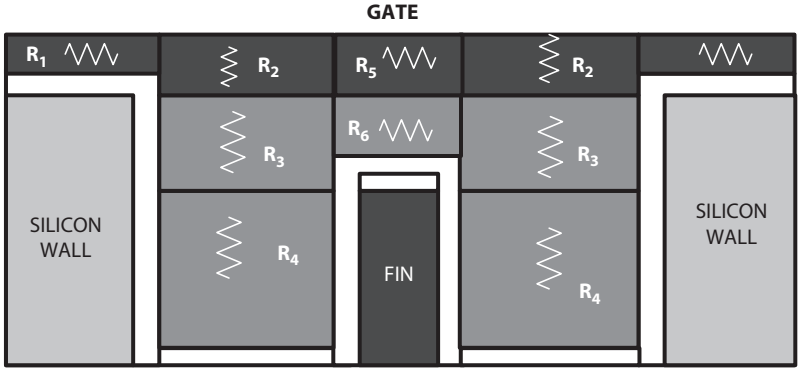

Figure 11.14 Decomposition of resistance components of FinFET technology.

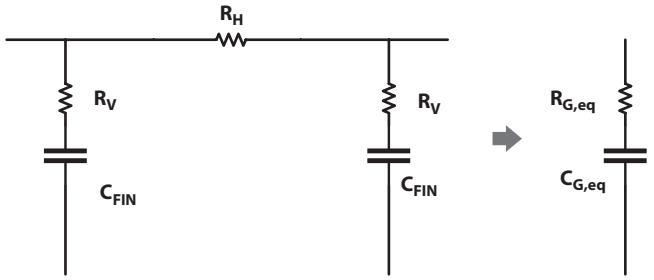

Figure 11.15 Simplified power-equivalent RC network.

resistance of FinFET is denoted by $R_{G,eq}$ or simply R_G and it is calculated by considering the power equivalent network [8] as shown in Figure 11.15.

For the single fin structure, the gate resistance can be calculated as follows:

The gate resistance is given by

$$R_G = R_{CONTACT} + \frac{R_V}{2} + \frac{R_H}{6} \tag{11.1}$$

$$R_{CONTACT} = R_1 \tag{11.2}$$

$$R_V = R_2 + R_3 + \frac{R_4}{3} \tag{11.3}$$

$$R_H = R_5 || R_6 \tag{11.4}$$

Where, $R_{CONTACT}$ is the contact resistance, and R_V & R_H are the vertical and the horizontal resistances. If the number of fin increases, then the gate resistance can be calculated as given by:

$$R_G = R_{CONTACT} + \frac{N}{3}\left(1 - \frac{1}{4N^2}\right)R_H + \left(\frac{1}{N} - \frac{1}{2N^2}\right)R_V \tag{11.5}$$

Where 'N' is number of fins. If 'N' is very large, then the equation for gate resistance can be simplified as

$$R_G \approx R_{CONTACT} + \frac{NR_H}{3} + \frac{R_V}{N} \tag{11.6}$$

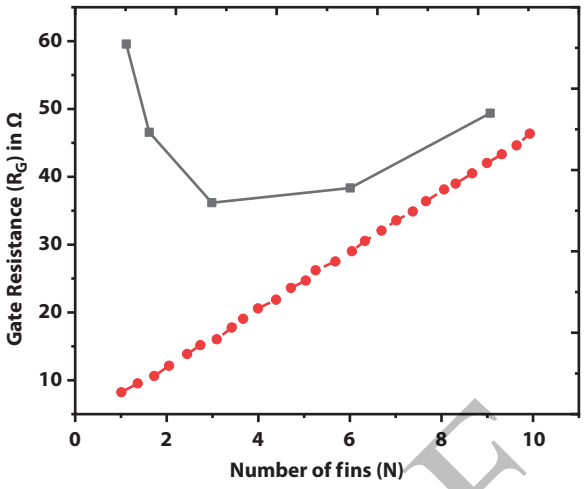

Figure 11.16 Variation of gate resistance with respect to number of fins.

Due to the nonlinear relationship of vertical resistance with the number of fins, gate resistance [9] starts to decrease as 'N' increases until the horizontal resistance begins to dominate. In FinFET, as the width of the channel increases, the R_H becomes stronger, and then the gate resistance shows linear variation with respect to channel width as shown in Figure 11.16.

11.2.3 Self-Heating Effect in FinFETs

In recent years, the self-heating effect (SHEs) [10] has been a major issue in silicon industry because of the continuous downscaling of device dimensions. In planar bulk MOSFETs, the heat produced in the channel dissipates to the substrate easily by lateral spreading. On the other hand, unlike planar MOSFETs, the materials used in FinFETs have poor thermal conductivity; hence the self-heating effect in FinFETs is likely to be more significant than planar MOSFETs.

In CMOS devices, on application of the driving voltage, minority carriers in the channel gains sufficient energy and they tunneled into the cramped volume. Throughout this operation, scattering event of the phonon increases which continues to heat up the silicon substrate. But the heat released in this process does not completely absorbed by the buried oxide, and is accumulated in the channel. Hence, local temperature of the channel increases, which is referred as "self-heating effect".

11.3 Assessment of FinFET Technology for RF/mm-Wave Applications

Nowadays FinFETs offers superior control over the SCE but their speed of operation is limited to an extent [1] and the scaling of the gate length is insufficient for better RF performance. Therefore, for optimum performance from FinFETs, the understanding of parasitic's major role and their reduction techniques becomes utmost important. In a tri-gate FinFET, a high parasitic capacitance exists and hence, the cutoff frequency (f_T) is less than the planar architecture. Therefore, in spite of good DC characteristics and scaling benefits, one may hesitate to use FinFET for RF/mm-Wave circuit design because of relatively less peak f_T than the planar technology. In addition to this, the source-drain resistance (R_{SD}) can be reduced with many techniques reported in the literature. The reduction in spacer width causes increase in short channel effect. This would in turn causes higher f_T and lower maximum oscillation frequency (f_{max}) [1], hence better RF performance. It is important to consider the transistor with higher gain and frequency for reliable lifetime operation. The reduction in source-drain resistance without effecting SCE may be achieved by proper selection of epitaxial growth. By using this approach, the speed may increase but at the cost of increase in the parasitic capacitance. The two RF figure of merit, namely f_T and f_{max} to be considered [11] are calculated as under:

$$f_T = \frac{gm}{2\pi\sqrt{C_{gs}^2 + 2C_{gs}C_{gd}}} \times\left\{1 - \frac{C_{gs}+C_{gd}}{C_{gs}^2+2C_{gs}C_{gd}} \times [g_{ds}(C_{gs}R_s + C_{gs}R_d + C_{gd}R_d) + g_m(C_{gd}R_d - C_{db}R_s)]\right\} \tag{11.7}$$

$$f_{max} = \frac{f_t}{2}\left\{g_{ds}R_g + 2\pi f_t C_{gd}R_g + \frac{C_{gd}+C_{db}}{C_{gs}+C_{gd}}2\pi f_t C_{gd}R_g - \frac{C_{db}}{C_{gs}+C_{gd}}2\pi f_t C_{gs}R_s + \frac{C_{gs}^2 g_{ds}R_d + C_{gs}^2 g_{ds}R_s}{(C_{gs}+C_{gd})^2}\right\}^{-\frac{1}{2}} \tag{11.8}$$

where g_m is transconductance, g_{ds} is the output conductance, C_{gs} & C_{gd} are gate-to-source and gate-to-drain capacitances, R_s & R_d are source and drain extrinsic resistances, C_{db} is drain-to-bulk junction capacitance, and R_g is the gate resistance. In order to obtain the intrinsic characteristics along with g_m and g_{ds}, a 3-D simulation is shown.

11.3.1 RF Performance

With the evaluation of three-dimensional structure, it is observed that the gate resistance has horizontal and vertical resistance components. In the previous discussions, the total gate resistance for multiple fins is calculated. In the total gate material across multiple fins, some of the material between the Fins is not functional, as it does not contribute to the transconductance of the device but still contributes to the parasitic loads ($R_{out,DC}$). The non transconductance contributing section of the gates increases the total gate resistance, the parasitic capacitance [11] between gate-to-drain/source interface ($C_{gd,par}$, $C_{gs,par}$) and the gate to outside channel fin ($C_{g,finr}$). Hence, more gate material between the fins degrades the peak f_T as compared to the planar devices. The recent silicon evidence proves that the peak f_T of FinFET is 20% less than that of planar devices. The vertical portion of gate resistance, reduces the total gate resistance up to a certain number of fins as shown in Figures 11.17 and 11.18. The value of f_{max} is high in case of FinFET which makes it suitable for mm-Wave circuit design.

From recent literature survey, it has been observed that the peak f_T and peak f_{max} degrades with respect to poly pitch tightening, due to large

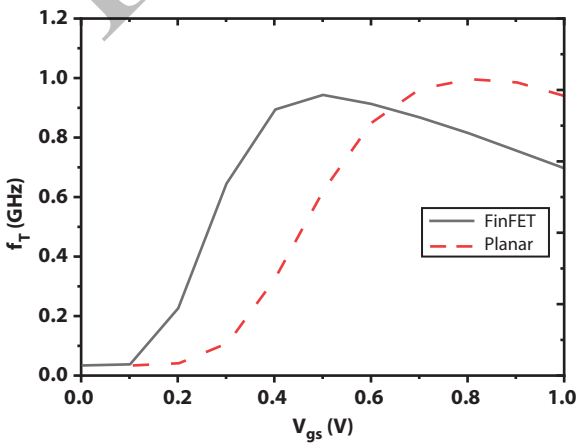

Figure 11.17 f_T variations in FinFET and Planar devices with respect to V_{gs}.

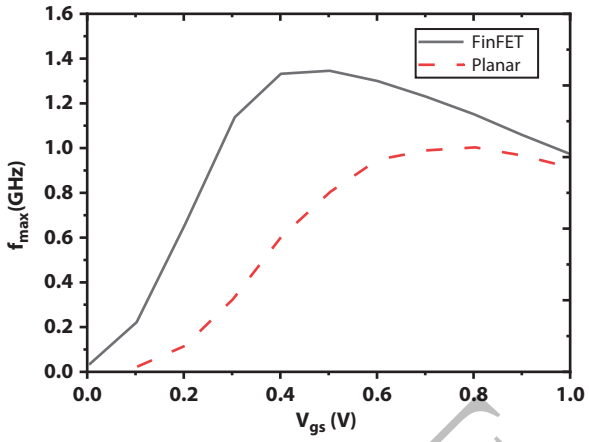

Figure 11.18 f_{max} variations in FinFET and Planar devices with *respect to* V_{gs}.

parasitics. The peak f_T and peak f_{max} in planar devices constantly improved by scaling channel length, increasing the transconductance and decreasing the gate capacitance. In FinFET technology, the enhancements in transconductance are associated with channel length shrinking because of velocity saturation. The complete trend of peak f_T and peak f_{max} has reached 22nm [6, 12] technology peaks for both planar and FinFET technologies as shown in Figures 11.19 and 11.20.

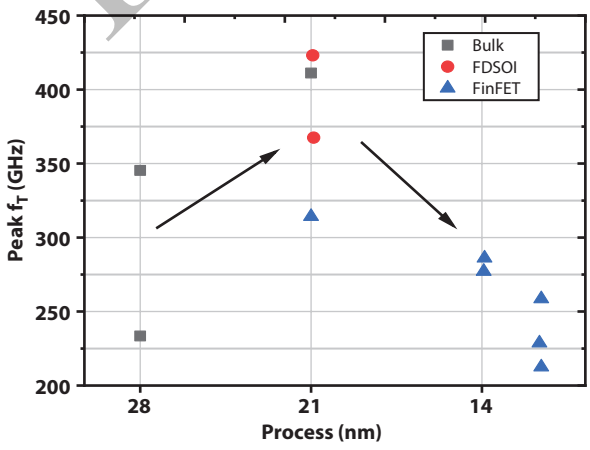

Figure 11.19 Variation in f_T with process technology.

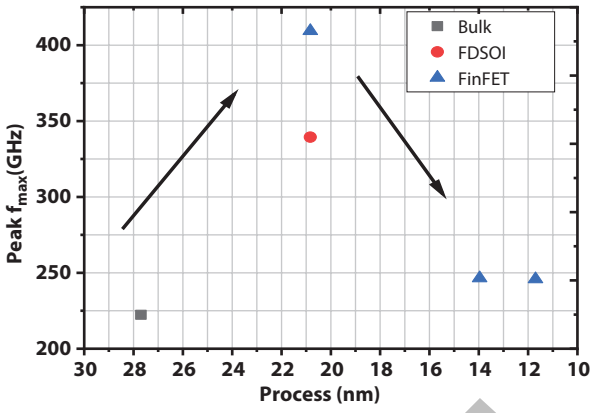

Figure 11.20 Variation in f_{max} with process technology.

11.3.1.1 Parasitic Extraction

1. Series resistance (R_S):
The distance between the gate edge and drain (L_{GD}) and Fin width can be adjusted in order to decrease the source-drain resistance R_{SD} only if the technology permits. Several experiments shown that the scaling down of L_{GD} up to 40nm reduces the effective R_{SD} by 25%. It is because the path of current in the extension is decreased and the final effective fin width is increased according to fin curvature.
2. Gate resistance (R_G):
Designing of gate resistance (R_G) plays very important role in RF performance as it effects f_{max}. In addition, R_G becomes very significant with

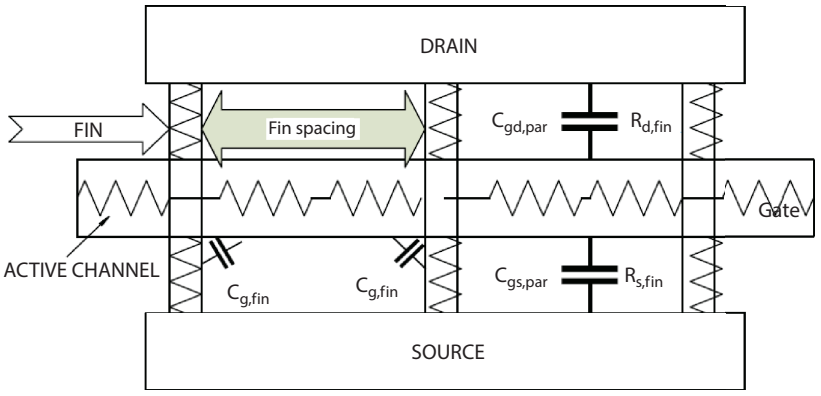

Figure 11.21 FinFET parasitic representation.

downscaling of L_G. Compared with the planar devices, in FinFET devices, the gate is placed over a non-uniform substrate. The gate resistance can be considered by taking a series connection of RC components in transmission lines as shown in Figure 11.21.

3. Substrate resistance (R_{sub}):

The substrate resistance(R_{sub}) can be extracted from a conventional off-state equivalent circuit as shown in Figures 11.22 and 11.23 [13]. The extracted R_{sub} of a planar device with a gate length (L_G) of 50 nm, a channel width (W) of 140 nm has notable frequency dependency. Whereas in FinFET, the substrate resistance has less frequency dependency with increase in size of the device.

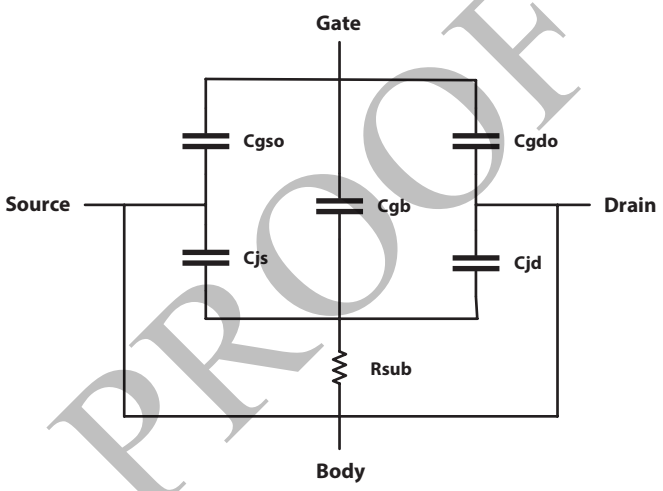

Figure 11.22 Off-state small signal equivalent circuit of MOSFET for RF modelling.

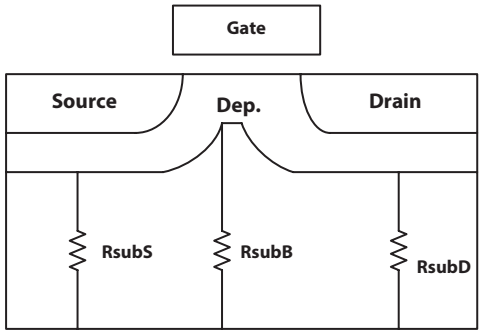

Figure 11.23 Two dimensional cross sectional view of substrate resistances [14].

4. Parasitic capacitance:
A higher value of capacitance is observed in FinFET as compared to a planar transistor. It has been found that the speed of the device may increase if the existing parasitic capacitance of the finger interconnection and back-end-of line (BEOL) is reduced. When the interconnect is de-embedded, the f_T improves by 20%. The drain to source interconnect capacitance can be reduced if the distance between active areas increases and when the layers above metal 1 are suppressed. The scalable model can be implemented by taking only first order parasitic into consideration. The model depicts an increase in C_p with N_{finger}, even when the total width is kept constant, i.e., N_{finger}. N_{fin} = constant. This is proved experimentally by a 15% f_T variation for different folding.

Although the peak f_T is reduced in FinFET technology due to parasitics, yet it offers better performance for RF and mm-Wave design over the planar. It is worthwhile to note that the peak f_T and f_{max} of planar device required 60% higher V_{gs} than FinFET due to SCEs or DIBL effect.

11.3.2 Noise Performance

With the rapid increase in scaling of CMOS technology, the noise personation in terms of robustness became more important, hence gearing up voltage margin is reduced as transistor size shrinks. So the noise study is important to understand the reliability issues. In addition, 1/*f* can be used as a most reliable diagnostic tool to check the quality of interface between oxide/substrate, gate/oxide and the oxide itself.

For better understanding of noise performance and also to provide the better results for circuit simulation, two physical models are proposed, which explains the 1/*f* noise [14] and speculate a gate bias dependence on noise spectra. The McWhorter theory model demonstrates that 1/*f* noise occurs because of carrier fluctuations (Δn) in the channel due to capturing and releasing of carriers in dielectrics. Whereas, Hooge theory model demonstrates that the noise is generated with mobility fluctuation (Δu), because of carrier separation by photons. To discuss the emergence of flicker-noise, which is still unresolved in the above models, the bias temperature instability (BTI) [15] used as an alternate tool. BTI becomes the critical issue for both NMOS and PMOS devices on application of the high metal gate potential. The positive BTI (PBTI) in NMOS is because of electron trapping, which occurs at high potential. On the other hand, PMOS has worst negative BTI (NBTI) performance.

A two-port noise network is shown in Figure 11.24, where one can reconstruct the noisy two port network to noiseless equivalent two port

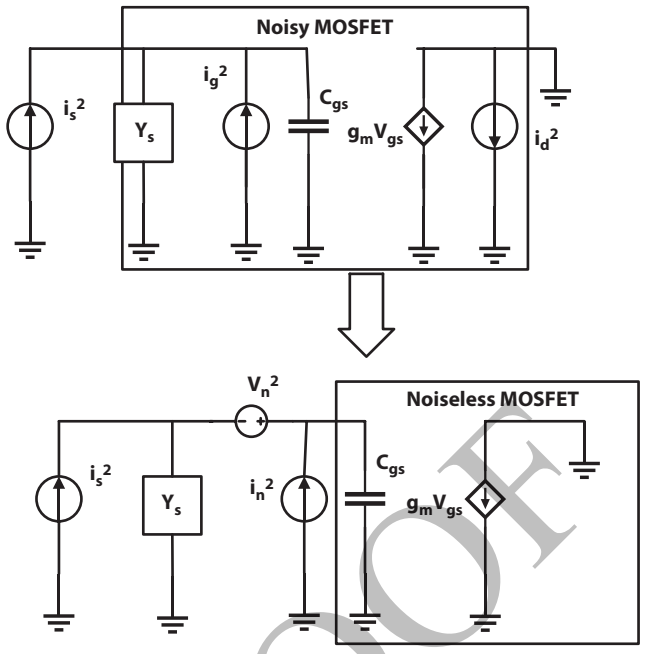

Figure 11.24 Two-port noisy and noiseless models of MOSFET.

network. From the equivalent model, we can derive the noise factor (F), minimum possible noise factor (F_{min}), optimum noise impedance (Z_{opt}), and equivalent noise conductance (G_n) as:

$$F = F_{min} + \frac{G_n}{R_s} | Z_s - Z_{opt} |^2 \tag{11.9}$$

$$F_{min} = 1 + 2\left(\frac{\omega}{w_t}\right) b_3 \Upsilon \tag{11.10}$$

$$Z_{opt} = \frac{1}{\omega C_{gs}}\left(\frac{b_3}{b_2}\right) + j\frac{1}{\omega C_{gs}}\left(\frac{b_1}{b_2}\right) \tag{11.11}$$

$$G_n = \frac{\gamma(\omega C_{gs})^2}{g_m} \tag{11.12}$$

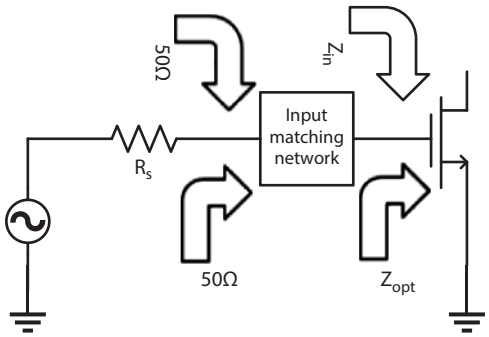

Figure 11.25 f_T and intrinsic gain for the bias condition.

Where

$$b_1 = 1 + \Delta\,|\,c\,|, b_2 = 1 + 2\Delta\,|\,c\,| + \Delta^2, b_3 = \Delta\sqrt{1 - |\,c\,|^2} \text{ and } \Delta = \sqrt{\frac{\delta}{5\gamma}}$$

Where C is the noise correlation coefficient, ɣ and δ, are the thermal noise excess factor and thermal noise parameter respectively. The noise correlation coefficient (C) is frequency independent and also decreases as channel length decreases.

From the above equations, it can be observed that overall NF_{min} reduces as unity gain frequency ($wt = 2\pi f_t$) increases and G_n is most sensitive to C_{gs} than w_t. We can conclude that G_n determines the sensitivity of the device to noise mismatch by increasing the amount of mismatch between the source impedance and the optimum noise impedance.

To attain overall improved noise performance *viz.*, lowering NF_{min} and G_n can achieve the lower total noise factor. It has been already determined that the unity gain frequency ωt of FinFET exceeds the planar by more than 50% at reduced bias conditions. Hence, a significant improvement is achieved in thermal noise for the gain at V_{cc} = 1V and $30GH_z$ as confirmed by the Figure 11.25.

11.3.3 Noise Matching with Gain at the mm-Wave Frequency

The LNA (low noise amplifier) design suffers due to noise and input mismatch. We know that, there is a mismatch between the conjugate of input impedance $\left(Z_{in}^*\right)$ and optimum noise impedance (Z_{opt}), and Z_{in}^* can be expressed as

$$Z_{in}^{*} = r_g + j\frac{1}{\omega C_{gs}} \tag{11.13}$$

Where r_g is the gate resistance. This mismatch determines that how much noise performance degradation occurs when the input matching network is designed for minimum signal reflection and vice versa. The mismatch between the optimum noise impedance (Z_{opt}) and the input matching impedance (Z_{in}) cannot be neglected for planar devices. Hence, it is a major challenge in LNA design to adjust the matching condition to equalize the two impedances Z_{in}^{*} and Z_{opt} by various circuit techniques, such as inductive source degeneration, etc. To match Z_{in}^{*} with Z_{opt} the relationship to be maintained is:

$$r_g \approx \frac{1}{\omega C_{gs}}\frac{b_3}{b_2} \tag{11.14}$$

$$b_1 \approx b_2 \tag{11.15}$$

The above equations require a low-noise correlation coefficient *c* and a low-noise gamma factor ɣ. This ɣ in FinFET already have been reported but still research is required to validate the low-noise correlation coefficient.

With increase in frequency, the noise matching point is reached where Z_{opt} and Z_{in} become closer to each other. The Z_{opt} and Z_{in}^{*} are conjugate, and so therefore no significant effort is required to design the input matching network.

11.4 Design Process of FinFET for RF/mm-Wave Performance Optimization

The FinFET oriented logic technology process has been successfully adopted due to improved scalability, low-power requirements and better performance results at very low technology nodes *viz.*, 14-nm and 16-nm technology. With more device counts in LTE supported phones and coming up sub-6GH_z 5G bands, area scaling is key factor to place number of chipsets within specified cellphone area taking power scaling also in consideration.

Table 11.1 Comparison of 14nm FinFET and 28nm Planar FET at different process technology ~~[16]~~.

Technology parameter	**14-nm FinFET (without high-k)**		**28-nm planar FET (with high-k)**	
Device	NFET	PFET	NFET	PFET
$L_{gate}\,(nm)$	14	14	30	30
Contact poly pitch (nm)	78	78	126	126
$V_{dd}\,(V)$	0.8	0.8	1.05	1.05
Drain saturation current, $I_{dsat}\left(\frac{\mu A}{\mu m}\right)$	1523	1433	670	450
Transconductance, $G_{msat}\left(\frac{\mu S}{\mu m}\right)$	3017	2748	985	395
$F_t/F_{max}\,(GHz)$	314/180	285/140	308/159	185/102

RF and analog compatibility of the FinFET technology plays a major role in realizing RF performance along with logic System on Chip (SoC) to enhance the logic power, performance characteristics and area grading. The 14-nm FinFET has clear benefits over 28-nm planar FETs with drive current (I_d) and transconductance (g_m) for a given design specification as shown in Table 11.1 [16]. Q1

11.4.1 Cascaded Chain Design Consideration for Wireless System

Wireless system design aims for two primary performance goals: noise and linearity. Obtaining the performance target is one thing, but market competitiveness of the end product requires attention to power dissipation and area. The silicon area of the wireless system is more dominated by passive components, such as an embedded coil. And this coil technology is highly independent of process nodes. Due to design rule complications and excessive parasitics in the device and metal interface within such a less accessible space, the transistor node scaling does not always bring positive impact on silicon area scaling. Hence, the total radio frequency integrated

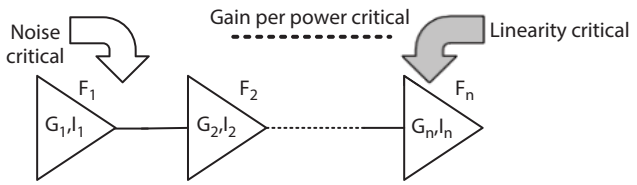

Figure 11.26 Cascaded chain with n-stages.

circuit (RFIC) power dissipation is the major challenging factor among the products in the market.

In wireless system design process, the signal link is optimized by using the cascaded chain shown in Figure 11.26. Noise factor (F) and the linearity ($IIP3$) in the cascaded chain are expressed as:

$$F = F_1 + \frac{F_2}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \tag{11.16}$$

$$\frac{1}{IIP3} = \frac{1}{I_1} + \frac{G_1}{I_2} + \frac{G_1 G_2}{I_3} + \ldots \tag{11.17}$$

As depicted from equations, the first stage predominates the noise performance (F_{total}), while the last stage dictates the linearity performance ($IIP3_{total}$). The remaining stages will focus more on power efficiency to optimize the overall power dissipation.

11.4.2 Optimization of Noise Figure with G_{max} for LNA Within Self-Heat Limit

With the continuous down scaling of technology, RF performance of CMOS devices has been enhanced accordingly. In the deep-submicron technology, from the device point of view, short-channel MOSFETs exhibits high-frequency figure of merits (FoMs) like cut-off frequency (f_T) and the maximum oscillation frequency (f_{max}) which are more than 100GHz. These FoMs usually do not give any design insights for RF circuit optimization, instead they suggest the flexibility of CMOS devices for operating in RF range. $g_m f_T / I_D$ has been considered as an FoM in case of RF MOSFETs. g_m^2 / I_D has been considered as an FoM in case of analog amplifiers to get gain performance, as it gives power gain per unit dc power consumption.

For LNA design [16], the three basic parameters viz., gain (G), noise figure (F) and power consumption (P) are related as:

$$FoM_{LNA} = \frac{G}{(F-1).P} \tag{11.18}$$

The figure-of-merit may include bandwidth as well, but for this, we need to derive the bias condition for a mm-Wave LNA design. Mason gain U, a reference device metric for mm-Wave design methodology is required for G_{max} extension to overcome the F_{max} limitation with neutralization techniques. As discussed earlier, the gate resistance is a nonlinear function of number of fins, so it became an important factor to determine the number of fins for the design under consideration based on the distance between Z_{in}^{*} and Z_{opt} It shows that the peak G_{max} and minimum of Noise figure, NF_{min} can be obtained in a relatively same bias condition.

Each performance factor in LNA's FoM can be analyzed by using small-signal equivalent circuit. Assuming the perfectly matched condition, which is practically suitable at lower target frequency, the signal gain can be given as

$$G = \frac{P_{load}}{P_{in}} = \frac{1}{4}\left(\frac{g_m}{\omega.C_{gs}}\right)^2 \propto g_m^2 \tag{11.19}$$

Here, C_{gs} is constant in the strong inversion region and the signal gain is almost proportional to g_m^2. It is also observed that lower noise figure requires higher g_m, hence high current density is required for planar technology. In FinFET, the overall DC power in the device should be limited or maintained within the certain range to avoid the self-heating effect. By taking the self-heating under consideration, the values for NF_{min} and G_{max} maintained at a constant power limit, called FiSH limit swept for current density, J_D.

The mason gain U is also known for constant power limit after penalized by NF_{min}, written as $U(dB) - NF_{min}(dB)$ This is the modified FoM of LNA (FoM_{LNA}) [17]. Taking the FiSH power limit as reference, the DC power term in the original FoM_{LNA} is constant and hence can be removed. With the elimination of DC power term in the equation, the NF_{min} adjusted by Mason gain, $U(dB) - NF_{min}(dB)$ is approximated to the original FoM_{LNA}. The modified FoM_{LNA} is maximum if G_{max} highest bias point and the NF_{min} lowest bias point are closest. For a four-fin device, the maximum FoM_{LNA}

point has been observed while both G_{max} and NF_{min} reach their optimum performance at the closer bias condition.

11.4.3 Gain Per Power Efficiency

Mason has given the unilateral gain, known as Mason gain (U). It describes that maximum stable gain (MSG) is obtained if there is only forward gain in the lossless network. The mason gain (U) is used to measure F_{max} by simply measuring the frequency where the mason gain is unity. It is the absolute measure of F_{max}, where the device operates with the positive power gain if there is any feedback compensation technique available in the device. From Figure 11.27 [8], it is to be noted that for any active device if the frequency increases there will be reduction in its gain due to the increased passive loss in the device network.

As the modern wireless systems used to integrate more wireless standard supporting many frequency bands in a single chip, modern RFIC design emphasizes even more on low-power design.

For a low-power design, one can trade the number of amplifier stages for the total power dissipation by maximizing the gain per stage under the condition that avoids unnecessary power waste for gain as shown in Figure 11.28 [8]. It is estimated that the total number of amplifier stages to achieve a total target gain by dividing over the mason gain of the device by assuming that mason gain is maximum achievable gain per device at a given frequency. Here, the product of I_d/g_m and the total number of amplifier stages

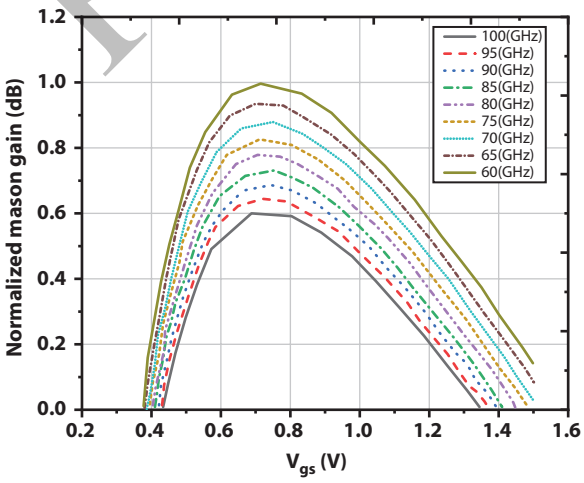

Figure 11.27 Mason gain at different frequencies.

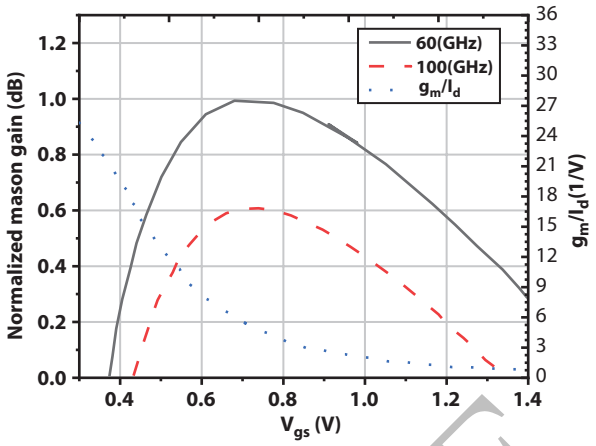

Figure 11.28 Mason gain variation at 60 GHz and 100 GHz with *respect to* V_{gs} (V).

is the division of total target gain over mason gain U. It is possible to maximize the inverse of the product of I_d/g_m and the number of stages, which can be defined as Gain-Power Figure of merit (FoM_{GP}) given as:

$$FoM_{GP} = U\frac{g_m}{I_d} \tag{11.20}$$

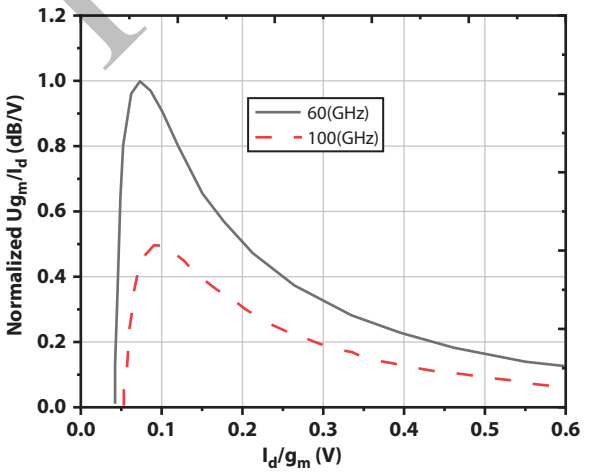

Figure 11.29 Variation in FoM_{GP} with I_d/g_m.

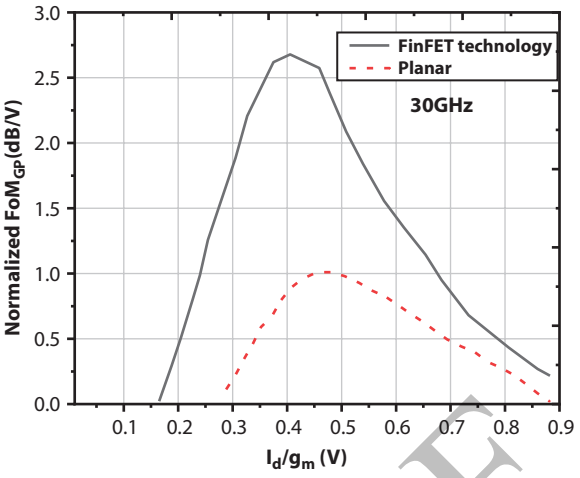

Figure 11.30 Comparison of FoM_{GP} for FinFET and Planar devices at 30GHz with I_d/g_m.

Figure 11.29 shows the FoM_{GP} normalized to peak value at 60 GHz. It has been noticed that FoM_{GP} reaches the peak value at a certain point, which is the optimum bias condition to maximize device gain per power dissipation. The most current planar technology exhibits around a 70–160% improvement in FoM_{GP} over the FinFET technology, which means 40–60% less power dissipation to obtain the same amount of gain as shown in Figure 11.30 [8].

11.4.4 Linearity for Gain and Power Efficiency

Linearity [18] is a critical property for the wireless system configuration represented by *IIP*3 or P_{1-dB}. Linearity describes the overall performance degradation by blockers and jammers. Among the various linearity measurement techniques, the double-tone intermodulation distortion is widely used, and is specified by 3rd order intercept point, IP3. This IP3 data can be examined by using either measured or simulated I-V data or double-tone measurement. However, existing reports are mainly for 130nm or older technologies, and depending on first order IP3 theory that relates IP3 to 3rd order derivative of I_{DS} with respect to V_{GS} only. The simple expression of third-order input interception point (*IIP*3) can be given as

$$IIP3 = \frac{1}{6R_s}\frac{(1+(\omega C_{gs}R_s)^2)}{\left|\frac{K_{3gm}}{g_m}\right|} \tag{11.21}$$

Where

$$K_{3gm} = \frac{1}{6}\frac{\partial^3 I_{DS}}{\partial^3 V_{GS}}$$

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}}$$

To increase the linearity, it is required to maximize the ratio called as linearity figure-of-merit (FoM_{LIN}), which approaches to unity when the third-order term K_{3gm} is minimized as given by

$$FoM_{LIN} = \frac{g_m}{g_m + |K_{3gm}|} \tag{11.22}$$

Figure 11.31 depicts that FoM_{LIN} increases as I_d/g_m increases which confirms that the improvement in linearity needs more power dissipation.

If both the gain and linearity improvements are considered, the product of FoM_{GP} and FoM_{Lin} derives another figure-of-merit defined as gain-power-linearity figure-of-merit (FoM_{GPL}), which defines the optimum gain-linearity balanced performance per power dissipation shown in Figure 11.32 [8].

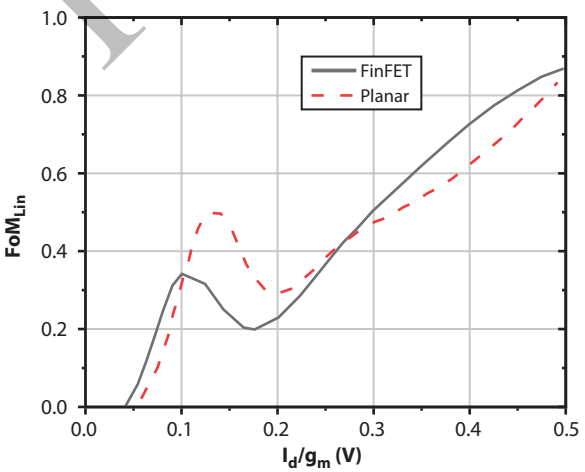

Figure 11.31 Comparison of FoM_{Lin} for FinFET and Planar devices with respect to I_d/g_m.

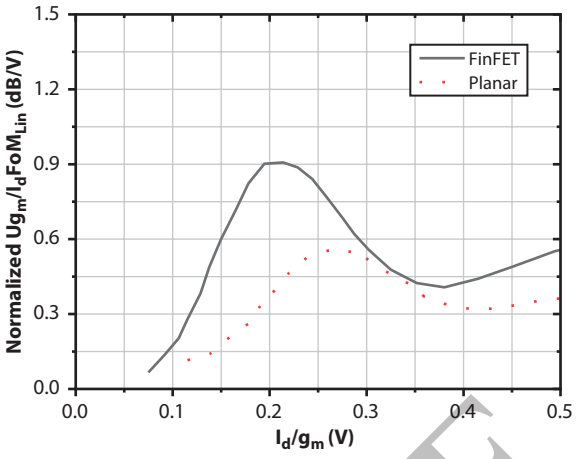

Figure 11.32 Comparison of FoM_{GPL} for FinFET and Planar with respect to I_d/g_m.

This confirms over 80% benefits of FinFET devices over planar devices with less current density requirements.

11.4.5 Neutralization for mm-Wave Applications

We have compared the FinFET technology against planar using unilateral gain, assuming no feedback network. But, in reality the FinFET offers higher feedback capacitance, C_{gd}, than the planar. This capacitance is a key contributor in limiting the maximum oscillation frequency F_{max}. Hence, it is being advantageous to adopt a technique which can reduce or eliminate

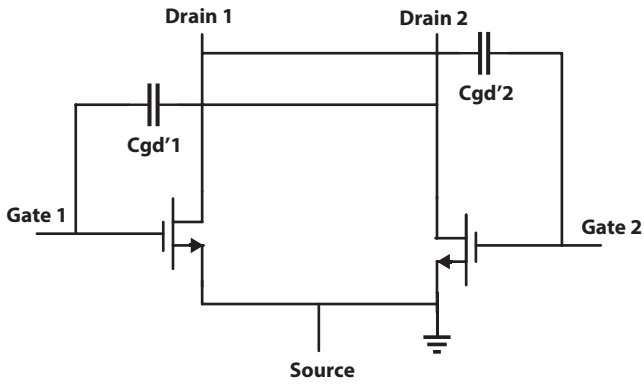

Figure 11.33 Differential neutralization technique.

the feedback capacitance in order to increase the F_{max}. This causes an increase in the gain (G_{max}), generally 4-5dB with the neutralization.

The typical neutralization technique is shown in Figure 11.33. This technique is completely based on cross-coupled capacitor structure to generate the negative C_{gd}, or alternately neutralize the device C_{gd}. This technique consists of differential configuration and provides the neutralization for wide bandwidth range. However, it is evident that the input impedance changes after neutralization. After neutralization, Z_{in}^{*} and Z_{opt} are no longer close to each other i.e., they move further apart, especially the real part of input impedance. Z_{opt} remains constant before and after neutralization. So, Z_{opt} is less susceptible to the stability issues. These effects need to be considered while applying the neutralization techniques.

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Q1 Kindly check if Table 11.1 citation is correctly inserted here, if not kindly provide citation for Table 11.1 in text (for example: "A short comparison of merits and demerits of linearization methods utilized for characterization of PA linearity is discussed in Table 12.1.")