Dt. 26.01.2024

BoS (On-Line) meeting for approval of R22. III Year, IV Year Syllabus & Open Electives

Agenda of Meeting:

Reason for changing course structure from R20-R22
Inclusion of new courses.

Minutes of Meeting- Discuss about III Year, IV Year syllabus & open electives for R-22 Regulation.

Briefing of syllabus is given by HoD for Regular III Year & IV Year.

Course Structure in discussed by BOS Chairman Dr. B. Swapna Rani.

The progress in curriculum grouping based on course components for batch of 2022-2026 is done by categorizing 20.62% for Hs & BS, 14.30% ES, 57.5% PC & 7.5 % for inter disciplinary.
Engineering Sciences are important now a days as it helps the students to develop knowledge about different Career opportunities, problem-solving skills, and technological advancements. Therefore the categorization percentage has been increased from R20-R22 regulation by introducing Engineering Workshop and Python Programming Lab.

Changes in course structure are done, Compared to R-20 Regulation to meet.

a) Employability is given weightage in Curriculum design & development, as the student can recruit as Embedded Systems Design Engineer, VLSI Design Engineer, Machine learning Engineer, Telecommunications Engineer etc.
b) To provide thinking process in students, this facilitates the faculty to inculcate creativity & innovations in students.
c) To have reasonable no. of multidisciplinary courses, where the structure is well organized with links progress one course to another course, steadily for good comprehension of all courses.
d) The introduction of fundamental core courses in I Year to facilitate better understanding of Circuit related courses & develop affinity toward Dept.

The Cause of Revision and use of Revision of new Courses

1. Applied Python can be used in Circuit design and analysis, data acquisition and Processing, Control Systems, Signal Processing, Image processing, Machine learning etc.

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Electronics & Communication Engineering
TKR College of Engineering & Technology
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Medbowli, Meerpet, Hyderabad-97.

2. C^{++} & Data Structures is introduced in PE-I as it an essential for system level programming and Embedded system.
3. Mini Projects is introduced in 7^{th} semester for the students to have practical exposure in the fields of IoT, Image processing, VLSI etc.
4. AI is the branch of Machine learning is introduced in PE-2, PE-3 as it has various ECE related applications such as Signal Processing, Data Compression, Error correction, Modulation, encrypts etc.
5. Advanced Communication Lab is introduced in the structure which helps the students to learn circuits for transmission & Receiving Analog & Digital Signals.
6. Students need to produce applications which have social benefits. They should be taught well-being of human society. Discipline & ethical issues related to what they create is important, in this regard Cyber Security in 6^{th} semester & Professional Ethics in the 7^{th} semester are introduced.
7. Discussed about open Electives that are to be offered to other dept.

Suggestions Given by the External board Committee.

- Committee has gone through course outcomes & suggested to articulation matrix in syllabus with cognitive level.
- Suggested Textbook names in syllabus copy should be in IEEE format suggested by committee.
- VLSI design subject pre requisite in required.
- "Testing of Chips" in VLSI subject syllabus.
- Cognitive names to be removed.
- Latest topics "Cognitive Radio" topic need to be added in syllabus has been suggested by committee in further regulations.
- Encryption Techniques should be added in open elective (Data Communication) subject.
- IV-I 5G Technology & 4G Syllabus is to be introduced in syllabus.
- Industrial visit for having good exposure to new technology in suggested by committee.
- Electromagnetic compatibility interface esteem need to be included in syllabus.
- Discussed about grading system also.

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Dt: 26.01.2024

BOS (ON-Line) For Approval of R22 Open Elective & III year & IV year Syllabus

Agenda of Meeting

→ Final approval of III year & IV year R-22 Syllabus & open Elective syllabus.
→ Reason for changing course structure.
→ Inclusion of new courses.

Minutes of Meeting → To discuss about R-22 open Elec, III year & IV years syllabus.

→ Briefing of syllabus is given by HOD regarding III year & IV yeas
→ course structure is discussed by BOS chairman Dr. B. SwapnaRani
→ committe has gone through course outcomes & suggested to articulation matrix in syllabus with cognitive levels
→ Suggested Text book names in syllabus copy should be in IEEE format suggested by committe.
→ VLSI design subject - Pre requisite is required
→ 'Testing of chips' in VLSI subjects syllabus
→ cognitive need to be Removed

→ latest topic "cognitive Radio" topic need to be added in syllabus has been suggest by committe too in further Regulations.

→ Encryption Techniques should be added in open Elective (Data communication) subject.

→ IV-I Sem Technology (6th sem syllabus is to be introduced in syllabus)

→ Industrial visit for having good exposure to new Technology is suggested by committe.

→ Electromagnetic compatibility / interference subject need to be included in syllabus

→ Discussed about Grading System also.

→ changes in course structure is done, compared to R-09 Regulation to meet.

(a) Employability is given weightage in curriculum designe & developement

(b) To provide thinking process in students which facilitate faculty to inculcate creativity & innovations in students

(c) To have reasonable no of multidiciplanary courses, where the structure is well organised with links progress one course to another course, steadily for good comprehension of all courses.

(d) The introduction of fundamental core courses in I year to facilitate better understading of circuit related courses & develope affinity toward Dept.

→ Applid Python

→ c++ & Data structures in introduced as in PE-I as it is essential for system level progams. & embeded system.

→ Mini Projects is introduced in 7th Semester for the students to have practical exposure in the fields of IOT, image process, VLSI etc.

→ AI is branch of Machine learning is introduced in PE-2, PE-3 as it has various ECE related applications such as signal processing, Data compression, Error correction, modulation, Encription etc.

→ Advanced communication Lab is introduced in the structure which helps the students to, learn how to design ckts for transmiss & Receiving analog & Digital signals.

→ Students need to produce applications which have social benifits, they should be taught well being of human society Dicipline & ethical issues related to what they create. in this regard professional Ethics is a subject includes in 7th sem & Cyber Security in 6th Sem.

→ The program curriculum grouping based course components for batch of 2022-2026 is done by following 20.62% for HS. & B.S, 14.30% ES, 57.5% PC & 7.5% for interdisciplinary.

→ Discussed about open Electives, that are to be offered to other Dept.

→ Mini Projects in VI Sem is Evaluated 40 marks for Internal & 60 marks for external during course work. The student is declared to have failed if he/she 1. Doesn't submit report 2. Doesn't make presentation before internal & external committe during course work. 3. Secured less than 40% marks.

Members of BOS

1. Dr. A. Rajani
Prof & H.O.D, JNTUH.

2. Dr. B. Rajendra Naik.
Prof, University College of Engg. O.U.

3. Dr. N. P. Supriya.
Scientist 'F', Defence Electronics Research Lab (DLRL), HYD.

4. Dr. C. Venkata Narsimhulu.
Prof & Principal. - CBIT., HYD.

5. Dr. M. Mahesh.
Prof, HOD.
26/01/2024.

6. Dr. D. Nageshwar Rao.
Prof, COE. - TKRCET
Senior Staff.
26/01/2024.

7. Dr. B. Swapna Rani
Assoc. prof, BOS Chairperson
26/01/2024

8. Dr. J. Smitha Kumari
Assoc. prof, Senior Staff.
31/01/2024.

9. Mrs. Sudha Rani
Assoc. prof, Senior Staff
26/01/2024.

10. Mr. Ganesh, Asst. prof.
26.01.24

Composition of BOS

Board of studies of every department shall be constitute as per the Good Governance Document guidelines **Date:26.01.2024**

S. No	Category	Name	Position (Status)	Designation in BOS	Subject Specialization	Contact No.	Email ID	Sign
1	Head of the Department concerned.	Dr.Mahseh	Professor, HoD	Member	Image Processing	8309165487	maskimahesh@tkrcet.com	
2	Senior Staff of the Dept.	Dr.D.Nageshwar Rao	Prof of ECE & CoE	Member	VLSI Design	9912713150	nageshwarrao@tkrcet.com	
3	Senior Staff of the Dept.	Dr.B.Swapna Rani	Assoc. Prof,	Chairman	VLSI Design	9866104554	swapnarani@tkrcet.com	26/01/2024
4	Two experts in the subject from outside the college to be nominated by Academic council.	Dr. B. Rajendra Naik	Professor, Dept of ECE, Univeristy College of Engineering Osmania University,Hyd	Member	VLSI Design	9441222226	rajendranaikb@osmania.ac.in	
		Dr.C. Venkata Narashimlu	Principal & Professor Dept of ECE, CBIT,Hyd	Member	Signal & Image Processing	9866472744	principal@cbit.ac.in	
5	One expert nominated from a panel of six recommended by the Vice chancellor of University (University Nominee)	Dr. A Rajani	Professor & HoD, Department of ECE, JNTUH, Hyderabad	Member	Signal & Image Processing	9989922228	rajani.akula@jntuh.ac.in	
6	One representative from industry/Corporate sector/allied area relating to placement.	Dr. N.P.Supriya	Scirentist 'F'Defence Electronics Research Laboratory(DLRL),Hyd	Member	Electromagnetic Compatibility	9490956264	supriya.np.dlrl@gov.in	
7	One postgraduate meritorious alumnus to be nominated by the principal.	S.Prathyusha	Asst.Prof,Dept of ECE Teegala Krishna Reddy Engineering College	Member	VLSI Design	9705269485	prathyusha.415@gmail.com	
8	Staff of The ECE Department	Ms. Ch. Divya	Asst.Prof	Member	Embedded Systems	9550899776	divyachitla@tkrcet.com	
9	Staff of The ECE Department	Ms. K. Shalini	Asst.Prof	Member	Embedded Systems	8686065979	shalinik@tkrcet.com	

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY (AUTONOMOUS)

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B.TECH. - ELECTRONICS & COMMUNICATION ENGINEERING

Course Structure R-22

SEMESTER V

S. No.	Course Classification	Course Code	Name of the Subject	L	T	P	C	I	E	Total
1	PC	D45PC15	Control Systems	3	1	0	4	40	60	100
2	PC	D45PC16	Microprocessors and Microcontrollers	3	0	0	3	40	60	100
3	HS	D5HSBF	Business Economics and Financial Analysis	3	0	0	3	40	60	100
4	PE	D45PE1	**Professional Elective-I** 1.C++ and Data Structures 2. Data Communications and Computer Networks 3. Introduction to Embedded Systems 4. Artificial Intelligence	3	0	0	3	40	60	100
5	OE	D45OE1	Open Elective-I	3	0	0	3	40	60	100
6	PC	D45PC17	Microprocessor & Microcontrollers Lab	0	0	2	1	40	60	100
7	PC	D45PC18	Advanced Communications Lab	0	0	2	1	40	60	100
8	HS	D5HSE3	Advanced English Communication Skills Lab	0	0	4	2	40	60	100
9	MC*	MC005	Entrepreneurship*	3	0	0	0	0	0	0
TOTAL				18	1	8	20	320	480	800

University Nominee (Subject Expert)
Name: Dr. A Rajani
Signature:

Industry Nominee (Subject Expert)
Name: Dr. N.P.Supriya
Signature:

External Subject Expert-I
Name: Dr.B. Rajendra Naik
Signature:

External Subject Expert-II
Name: Dr.C. Venkata Narashimlu
Signature :

Dr. B. Swapna Rani
Chairman BoS

Dr. D. Nageshwar Rao
Senior Staff

Dr. M. Mahesh
HoD, ECE

B.TECH. - ELECTRONICS & COMMUNICATION ENGINEERING

Course Structure R-22

SEMESTER VI

S. No.	Course Classification	Course Code	Name of the Subject	L	T	P	C	I	E	Total
1	PC	D46PC19	Antennas and Wave Propagation	3	0	0	3	40	60	100
2	PC	D46PC20	Digital Signal Processing	3	1	0	4	40	60	100
3	PC	D46PC21	VLSI Design	3	0	0	3	40	60	100
4	PE	D46PE2	**Professional Elective-II** 1. Digital Design through Verilog HDL 2.Cellular and Mobile Communications 3. Advanced Microcontrollers 4. Digital Image Processing	3	0	0	3	40	60	100
5	OE	D46OE2	Open Elective-II	3	0	0	3	40	60	100
6	PC	D46PC22	Digital Signal Processing Lab	0	0	2	1	40	60	100
7	PC	D46PC23	VLSI Design Lab	0	0	2	1	40	60	100
8	PC	D46PC24	Internet of Things Lab	0	0	2	1	40	60	100
9	PC	D46PC25	Mini Projects	0	0	2	1	40	60	100
10	MC*	MC006	Cyber Security*	3	0	0	0	0	0	0
TOTAL				18	1	8	20	360	540	900

University Nominee (Subject Expert)
Name: Dr. A Rajani
Signature:

Industry Nominee (Subject Expert)
Name: Dr. N.P.Supriya
Signature:

External Subject Expert-I
Name: Dr.B. Rajendra Naik
Signature:

External Subject Expert-II
Name: Dr.C. Venkata Narashimlu
Signature :

Dr. B. Swapna Rani
Chairman BoS

Dr. D. Nageshwar Rao
Senior Staff

Dr. M. Mahesh
HoD, ECE

B.TECH. - ELECTRONICS & COMMUNICATION ENGINEERING

Course Structure R-22

SEMESTER VII

S. No.	Course Classification	Course Code	Name of the Subject	L	T	P	C	I	E	Total
1	PC	D47PC26	Microwave Engineering	3	1	0	4	40	60	100
2	HS	D7HSPE	Professional Ethics	2	0	0	2	40	60	100
3	PE	D47PE3	**Professional Elective –III** 1.Analog and Digital IC Design 2. Radar Engineering 3. Embedded System Design 4. Machine Learning	3	0	0	3	40	60	100
4	PE	D47PE4	**Professional Elective –IV** 1. Low Power VLSI Design 2. Satellite Communications 3. Real Time Operating Systems 4. Artificial Neural Networks	3	0	0	3	40	60	100
5	PC	D47PC27	Microwave Engineering Lab	0	0	2	1	40	60	100
6	PW	D47PW1	Project Stage-I	0	0	14	7	100		100
TOTAL				11	1	16	20	300	300	600

University Nominee (Subject Expert)
Name: Dr. A Rajani
Signature:

Industry Nominee (Subject Expert)
Name: Dr. N.P.Supriya
Signature:

External Subject Expert-I
Name: Dr.B. Rajendra Naik
Signature:

External Subject Expert-II
Name: Dr.C. Venkata Narashimlu
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B.TECH. - ELECTRONICS & COMMUNICATION ENGINEERING

Course Structure R-22

SEMESTER VIII

S. No.	Course Classification	Course Code	Name of the Subject	L	T	P	C	I	E	Total
1	PE	D48PE5	**Professional Elective –V** 1.Memory Technologies 2. Optical Fiber Communications 3. Embedded C 4. Electronic Measurements and Instrumentation	3	0	0	3	40	60	100
2	PE	D48PE6	**Professional Elective –VI** 1.CPLD & FPGA Architectures and Applications 2. 5G Technology 3. ARM Architectures & Interface Protocols 4. Digital Signal Processors and Architectures	3	0	0	3	40	60	100
3	OE	D48OE3	Open Elective –III	3	0	0	3	40	60	100
4	OE	D48OE4	Open Elective –IV	3	0	0	3	40	60	100
5	PW	D48PW2	Project Stage-II	0	0	16	6	40	60	100
6		D48PWCV	Comprehensive Viva-Voce				1	100		100
7		D48PWTS	Technical Seminar				1	100		100
TOTAL				12	0	22	20	400	300	700

University Nominee (Subject Expert)
Name: Dr. A Rajani
Signature:

Industry Nominee (Subject Expert)
Name: Dr. N.P.Supriya
Signature:

External Subject Expert-I
Name: Dr.B. Rajendra Naik
Signature:

External Subject Expert-II
Name: Dr.C. Venkata Narashimlu
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Dr. D. Nageshwar Rao
Senior Staff

Dr. M. Mahesh
HoD, ECE

B.TECH. ELECTRONICS & COMMUNICATION ENGINEERING

ARTIFICIAL INTELLIGENCE (D45PE1)

B.Tech. V Semester **L/T/P/C**
3/0/0/3

Course Objectives:

The objectives of the course are to:

1. To impart knowledge about Artificial Intelligence.
2. To give understanding of the main abstractions and reasoning for intelligent systems.
3. To enable the students to understand the basic principles of Artificial Intelligence in various applications.

Course Outcomes: Upon completing this course, the students will be able to

1. Relate the basics of the theory and about intelligent agents.
2. Capable of using heuristic searches, apply problem solving methods
3. Apply AI techniques to real-world problems to develop knowledge representation of intelligent systems.
4. Relate appropriately from a range of techniques and acquire knowledge when implementing intelligent systems.
5. Analyze structure of expert systems

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	3	2	2	1	1	1	-	-	-	-	1	-	
CO2	3	3	2	2	1	1	1	-	-	-	-	1	-	
CO3	3	3	2	2	3	1	1	-	-	-	-	1	2	
CO4	3	3	3	2	3	1	1	-	-	-	-	1	2	
CO5	3	3	3	2	3	1	1					1	2	

UNIT- I: Introduction

Introduction–Definition – foundation of AI and history of AI intelligent agents: Agents and Environments, the concept of rationality, the nature of environments, structure of agents, problem solving agents, problem formulation

UNIT- II: Problem Solving Methods

Problem solving Methods – Search Strategies- Searching for solutions, uniformed search strategies – Breadth first search, depth first Search. Search with partial information (Heuristic search) Hill climbing, A* ,AO* Algorithms, Problem reduction, Game Playing-Adversial search, Games, mini-max algorithm, optimal decisions in multiplayer games, Problem in Game playing, Alpha-Beta pruning, Evaluation functions.

UNIT- III: Knowledge Representation

First Order Predicate Logic – Prolog Programming – Unification – Forward Chaining-Backward Chaining – Resolution – Knowledge Representation – Ontological Engineering-Categories and Objects – Events – Mental Events and Mental Objects – Reasoning Systems for Categories – Reasoning with Default Information

UNIT- IV: Knowledge Acquisition

Introduction to Learning, Rule Induction, Learning from observation Inductive learning, Decision trees, Explanation based learning, Statistical Learning methods, Reinforcement Learning. Learning Using neural Networks, Probabilistic Learning Natural Language Processing.

UNIT- V: Expert systems

Introduction, basic concepts, structure of expert systems, the human element in expert systems how expert systems works, problem areas addressed by expert systems, expert systems success factors, types of expert systems, expert systems and the internet interacts web, model based reasoning, case based reasoning, explanation & meta knowledge inference with uncertainty representing uncertainty. Concepts, structure of expert systems, the human element in expert systems how expert systems works, problem areas addressed by expert systems, expert systems success factors, types of expert systems, expert systems and the internet interacts web, model based reasoning, case based reasoning, explanation & meta knowledge inference with uncertainty representing uncertainty.

TEXT BOOKS:

1. S. Russel and P. Norvig, "Artificial Intelligence – A Modern Approach", Second Edition, Pearson Education
2. David Poole, Alan Mackworth, Randy Goebel," Computational Intelligence: a logical approach",Oxford University Press.

REFERENCE BOOKS:

1. G. Luger, "Artificial Intelligence: Structures and Strategies for complex problem solving", Fourth Edition, Pearson Education.
2. J. Nilsson, "Artificial Intelligence: A new Synthesis", Elsevier Publishers.

B.TECH. ELECTRONICS & COMMUNICATION ENGINEERING

VLSI DESIGN (D46PC21)

B.Tech.VI Semester **L/T/P/C**
3/0/0/3

Pre-Requisites: Analog Electronics, Digital logic Design

Course Objectives:

1. Acquire qualitative knowledge about the fabrication process of integrated circuit using MOS, CMOS and Bi CMOS transistors and knowledge about basic electrical properties of MOS.
2. Preparing the layout of any logic circuit which helps to understand and estimate parasitic of any logic circuit.
3. Designing of different types of logic gates using CMOS logic and analyze their transfer characteristics.
4. Provide design concepts required to design data path building blocks and memories.
5. Design logic circuits using PLA, PAL, FPGA and CPLD. Understand different types of faults that can occur in a system and learn the concept of testing and adding extra hardware to improve testability of system.

Course Outcomes:

Upon successfully completing the course, students will be able to:

1. Demonstrate the fabrication process of integrated circuits using MOS transistors, including understanding the steps involved and the overall process flow.
2. Design the layout of a logic gates, considering parasitic effects and estimating their impact on circuit performance.
3. Analyze the time delay of CMOS inverter and to investigate the effect of capacitive loads
4. Build the different data path subsystem and serial access memories.
5. Construct the programmable logic devices and illustrate the testing strategies.

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2
CO1	2		3	3									3	
CO2	3	3	2											3
CO3		2	3	2										2
CO4	2	3		3									3	
CO5		2	3		2									3

UNIT-I

Introduction to IC Technology: Introduction, MOS, PMOS, NMOS, CMOS & Bi CMOS technologies, new trends in VLSI.

Basic Electrical Properties: Basic Electrical Properties of MOS: Ids-V_{ds} relationships, MOStransistor threshold Voltage V_t ,trans conductance g_m, output conductance g_{ds}, figure of merit ωo; Various pull ups, NMOS Inverter, CMOS Inverter an analysis and design, Bi-CMOS Inverters.

UNIT-II

VLSI Circuit Design Processes: VLSI Design Flow, Stick Diagrams, MOS Layers, Design Rules and Layout, 2μm CMOS Design rules for wires, Contacts and Transistors, Layout for NMOS and CMOS Inverters and Gates, Scaling of MOS circuits

UNIT-III

Gate Level Design: Designing static CMOS circuits for Logic Gates, Switch logic, Alternate gate circuits, power, time delays, Driving large Capacitive Loads, Wiring Capacitances, Fan-in and fan-out, Choice of layers.

UNIT-IV

Data Path Subsystems: Subsystem Design, Adders, Parity generators, Zero/One Detectors, Comparators, Shifters, Counters.

Array Sub systems: ROM, Serial access memories, SRAM, DRAM.

UNIT-V

Programmable Logic Devices: Programmable Logic Array (PLA), Programmable Array Logic (PAL), FPGAs, CPLDs, Standard Cells.

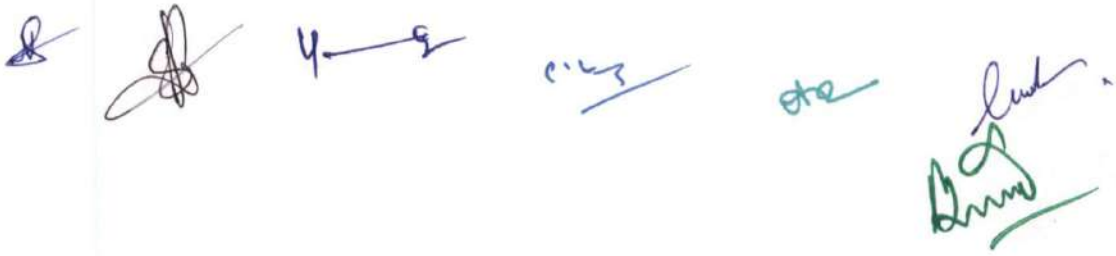
CMOS Testing: CMOS Testing, Need for testing, Test Principles, Design Strategies for test, Chip level Test Techniques.

TEXTBOOKS:

1. Kamran Eshraghian, Eshraghian Dougles and A.Pucknell, "Essentials of VLSI circuits and systems-, PHI, 2005 Edition.
2. Neil H.E.Weste, David Harris, Ayan Banerjee,"CMOS VLSI Design- a circuits and systems perspective", Peason, 2009.
3. M.Michael Val, "VLSI Design", 2001, CRC Press.

REFERENCEBOOKS:

1. Ming-BOL,"Introduction to VLSI Systems: A Logic, Circuit and systems Perspective"-, CRC Press, 2011.
2. P. Uyemura , "CMOS logic circuit Design-John", Springer, 2007.
3. Wayne Wolf, "Modern VLSI Design"-, Pearson Education, 3rd Edition, 1997.
4. N.H.E.Weste & D.Harris, "CMOS VLSI Design: A Circuits and Systems Perspective", 4th Edition, Pearson, 2011.
5. J.Rabey & B.Nikolic, "Digital Integrated circuits", 2nd Edition, Pearson, 2003.



TKR COLLEGE OF ENGINEERING AND TECHNOLOGY
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B.TECH. ELECTRONICS & COMMUNICATION ENGINEERING

ADVANCED MICROCONTROLLERS (D46PE2)

B.Tech. VI Semester

L/T/P/C
3/0/0/3

COURSE OBJECTIVES:

1. Explore the architecture and instruction set of ARM processor.
2. To provide a comprehensive understanding of various programs of ARM Processors.

COURSE OUTCOMES: Upon completing this course, the student will be able to

1. Analyze the selection criteria of ARM processors by understanding the functional level trade off issues.
2. Analyze the ARM instruction set and Thumb instruction set.
3. Illustrate the technical details of ARM Cortex M processors.
4. Operate ASM level program using the instruction set.
5. Generalize floating point operations using Cortex processors.

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2
CO1	3	2											2	
CO2	3	2											2	
CO3	3	2											2	
CO4	3	2											2	
CO5	3	2										2	2	

UNIT-I:

ARM Embedded Systems: RISC design philosophy, ARM design philosophy, embedded system hardware, embedded system software.

ARM Processor Fundamentals: Registers, Current Program Status Register, Pipeline, Exceptions Interrupts and Vector Table, Core Extensions, Architecture Revisions, ARM Processor Families.

Architecture of ARM Processors: Introduction to the ARM architecture

UNIT-II:

Introduction to the Arm Instruction Set: Data processing instructions, branch instructions, loadstore instructions, software interrupt instructions, program status register instructions, loading constants, ARMv5E extensions, Conditional execution.

Introduction to the Thumb Instruction Set: Thumb Register Usage, ARM-Thumb Interworking, Other Branch Instructions, Data Processing Instructions, Single-Register Load-Store Instructions, Multiple-Register Load-Store Instructions, Stack Instructions, Software Interrupt Instruction.

UNIT-III:

Technical Details of ARM Cortex M Processors: General information about Cortex-M3 and cortex M4 processors-Processor type, processor architecture, instruction set, block diagram, memory system, interrupt and exception support, Features of the cortex-M3 and Cortex-M4 Processors Performance, code density, low power, memory system, memory protection unit, interrupt handling, OS support and system level features, Cortex-M4 specific features, Ease of use, Debug support, Scalability, Compatibility.

UNIT-IV:

Instruction set of ARM Cortex M Background to the instruction set in ARM Cortex-M Processors, Comparison of the instruction set in ARM Cortex-M Processors, understanding the assembly language syntax, Use of a suffix in instructions, Unified assembly Language (UAL), Instruction set.

UNIT-V:

Cortex-M4-specific instructions, Barrel shifter, Accessing special instructions and special registers in Programming.

Floating Point Operations About Floating Point Data, Cortex-M4 Floating Point Unit (FPU)-overview, FP registers overview, CPACR register, Floating point register bank, FPSCR, FPU->FPCCR, FPU-> FPCAR, FPU->FPDSCR, FPU->MVFR0, FPU->MVFR1.

TEXTBOOKS:

1. Andrew N. SLOSS, Dominic SYMES, Chris WRIGHT, "ARM System Developer's Guide Designing and Optimizing System Software", Elsevier Publications, 2004.
2. Joseph Yiu, "The Definitive Guide to ARM Cortex-M3 and Cortex-M4 Processors", Elsevier Publications, 3rd Ed.,

REFERENCES:

1. Steve Furber ,"Arm System on Chip Architectures" –, Edison Wesley, 2000.
2. David Seal, "ARM Architecture Reference Manual" –, Edison Wesley, 2000.

B.TECH ELECTRONICS & COMMUNICATION ENGINEERING
EMBEDDED SYSTEM DESIGN (D47PE3)

B.Tech. VII Semester **L/T/P/C**
3/0/0/3

COURSE OBJECTIVES:

1. To provide an overview of Design Principles of Embedded System.
2. To provide clear understanding about the role of firmware, operating systems in correlation with hardware systems.

COURSE OUTCOMES:

On completion of the course, student will able to

1. Build the selection procedure of Processors in the embedded domain.
2. Design Procedure for Embedded Firmware.
3. Design Procedure for Communication Interface.
4. Analyze the role of Real time Operating Systems in Embedded Systems.
5. Detect the Correlation between task synchronization and latency issues.

Course	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	2						2						2	
CO2		2	2										2	
CO3		2	2										2	
CO4	2	3												2
CO5			3											2

UNIT– I:

Introduction to Embedded Systems: Definition of Embedded System Embedded Systems Vs. General Computing Systems, History of Embedded Systems, Classification, Major Application Areas, Purpose of Embedded Systems, Characteristics and Quality Attributes of Embedded Systems.

UNIT–II:

Typical Embedded System: Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS).

Embedded Firmware: Reset Circuit, Brown-our Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer, Embedded Firmware Design Approaches and Development Languages.

UNIT–III:

Trends in Embedded Industry: Processor Trends in Embedded Systems, Embedded OS Trends, Development Language Trends, Open Standards, Frame works & Alliances, Bottlenecks, Development Platform Trends, Cloud, Internet Of Things (IoT) & Embedded Systems.

Communication Interface: On board and External Communication Interfaces.

UNIT–IV:

RTOS Based Embedded System Design: Operating System Basics, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling.

UNIT–V:

Task Communication: Shared Memory, Message Passing, Remote Procedure Call and Sockets, Task Synchronization: Task Communication/Synchronization Issues, Task Synchronization Techniques, Device Drivers, How to Choose an RTOS.

TEXTBOOKS

1. Shibu K.V, "Introduction to Embedded Systems", Mc Graw Hill.

REFERENCEBOOKS

1. Raj Kamal,"Embedded Systems", Mc Graw Hill Education.
2. Frank Vahid, Tony Givargis, "Embedded System Design", John Wiley.
3. Lyla,"Embedded Systems", Pearson, 2013.
4. David E. Simon,"An Embedded Software Primer", Pearson Education.

B.TECH. ELECTRONICS & COMMUNICATION ENGINEERING

Machine Learning (D47PE3)

B.Tech. VII Semester

L T P C
3 0 0 3

Course Objectives:

1. To introduce the foundations of Artificial Neural Networks
2. To acquire the knowledge on Deep Learning Concepts
3. To learn various types of Artificial Neural Networks
4. To gain knowledge to apply optimization strategies

Course Outcomes:

1. Ability to apply the concepts of Neural Networks.
2. Ability to relate the Learning Networks in modelling real world systems.
3. Able to apply and use an efficient algorithm for Deep Models.
4. Ability to apply optimization strategies for large scale applications.
5. Able to analyze graphical models.

Course	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	3	2	2	1	1	1					1		
CO2	3	3	2	2	1	1	1					1		
CO3	3	3	2	2	3	1	1					1		
CO4	3	3	2	2	3	1	1					1		
CO5	3	3	2	2	3	1	1					1		

UNIT - I

Artificial Neural Networks Introduction, Basic models of ANN, important terminologies, Supervised Learning Networks, Perceptron Networks, Adaptive Linear Neuron, Back-propagation Network. Associative Memory Networks. Training Algorithms for pattern association, BAM and Hopfield
Networks.

UNIT - II

Unsupervised Learning Network- Introduction, Fixed Weight Competitive Nets, Maxnet, Hamming Network, Kohonen Self-Organizing Feature Maps, Learning Vector Quantization, Counter Propagation Networks, Adaptive Resonance Theory Networks. Special Networks-Introduction to various networks.

UNIT - III

Linear Models: Linear Basis Function Models -Maximum likelihood and least squares, Geometry of least squares , Sequential learning, Regularized least squares, Multiple outputs , The Bias-Variance Decomposition, Bayesian Linear Regression -Parameter distribution, Predictive, Equivalent, Bayesian Model Comparison, Probabilistic Generative Models-Continuous inputs, Maximum likelihood solution, Discrete features, Exponential family, Probabilistic Discriminative Models -Fixed basis functions, Logistic regression, Iterative reweighted least squares, Multiclass logistic regression, Probit regression, Canonical link functions

UNIT - IV

Kernel Methods: Constructing Kernels, Radial Basis Function Networks - Nadaraya-Watson model, Gaussian Processes -Linear regression revisited, Gaussian processes for regression, Learning the hyper parameters, Automatic relevance determination, Gaussian processes for classification, Laplace approximation, Connection to neural networks, Sparse Kernel Machines- Maximum Margin Classifiers, Overlapping class distributions, Relation to logistic regression, Multiclass SVMs, SVMs for regression, Computational learning theory, Relevance Vector Machines- RVM for regression, Analysis of sparsity, RVM for classification.

UNIT-V

Graphical Models: Bayesian Networks, Example: Polynomial regression, Generative models, Discrete variables, Linear-Gaussian models, Conditional Independence- Three example graphs, D-separation, Markov Random Fields -Conditional independence properties, Factorization properties, Illustration: Image de-noising, Relation to directed graphs, Inference in Graphical Models- Inference on a chain, Trees, Factor graphs, The sum-product algorithm, The max-sum algorithm, Exact inference in general graphs, Loopy belief propagation, Learning the graph structure.

TEXT BOOKS:

1. C. Bishop ,"Pattern Recognition and Machine Learning",Springer, 2006.
2. Simon Haykin,"Neural Networks and Learning Machines", 3rd Edition, Pearson Prentice Hall.

REFERENCE BOOKS:

1. Nils J. Nilsson ,"Introduction to machine learning", Stanford University Stanford.
2. William J. Deuschle ," Undergraduate Fundamentals of Machine Learning", thesis Harvard College, Cambridge.
3. Shai Shalev-Shwartz, Shai Ben-David,"Understanding Machine Learning, From theory to Algorithms", Cambridge University press, 2014.

B.TECH. ELECTRONICS & COMMUNICATION ENGINEERING
LOW POWER VLSI DESIGN (D47PE4)

B.Tech. VII Semester **L/T/P/C 3/0/0/3**

COURSE OBJECTIVES
The student will be able to
1. Understand the Fundamentals of Low Power VLSI Design.
2. Study low-Power Design Approaches, Power estimation and analysis.
3. Study and analyze the Low-Voltage Low-Power Adders, Multipliers.
4. Know concepts of Low-Voltage Low-Power Memories and Future Trend and Development of DRAM.

COURSE OUTCOMES:
Students are able to
1. Infer about the second order effects of MOS transistor characteristics.
2. Analyse and implement various CMOS static logic circuits.
3. Investigate the design techniques low voltage and low power CMOS circuits for various applications.
4. Organize the different types of memory circuits and their design.
5. Design and implementation of various structures for low power applications.

Course	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	2	3	3										3	
CO2	3	2	2										2	
CO3	3	3	2										2	
CO4	2	2	3										3	
CO5	2	3	3										2	

UNIT–I: Fundamentals: Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT–II: Low-Power Design Approaches: Low-Power Design through Voltage Scaling: VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches. Switched Capacitance Minimization Approaches: System Level Measures, Circuit Level Measures and Mask level Measures.

UNIT– III : Low-Voltage Low-Power Adders: Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look-Ahead Adders, Carry Select Adders, Carry Save Adders, Low Voltage Low-Power Design Techniques –Trends of Technology and Power Supply Voltage, Low Voltage Low-Power Logic Styles.

UNIT–IV: Low-Voltage Low-Power Multipliers: Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh-Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT–V : Low-Voltage Low-Power Memories: Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

TEXT BOOKS:

1. Sung-Mo Kang, Yusuf Leblebici, "CMOS Digital Integrated Circuits – Analysis and Design", TMH, 2011.
2. Kiat-Seng Yeo, Kaushik Roy, "Low-Voltage, Low-Power VLSI Subsystems", TMH Professional Engineering.

REFERENCE BOOKS:

1. Ming-BO Lin, "Introduction to VLSI Systems: A Logic, Circuit and System Perspective", CRC Press.
2. Anantha Chandrakasan, "Low Power CMOS Design", IEEE Press, /Wiley International, 1998.
3. Kaushik Roy, Sharat C. Prasad, "Low Power CMOS VLSI Circuit Design", John Wiley, & Sons, 2000.
4. Gary K. Yeap, "Practical Low Power Digital VLSI Design", Kluwer Academic Press, 2002.
5. Bellamour, M. I. Elamasri, "Low Power CMOS VLSI Circuit Design", A Kluwer Academic Press.
6. Siva G. Narendran, AnathaChandrakasan, "Leakage in Nanometer CMOS Technologies", Springer, 2005.

B.TECH. ELECTRONICS & COMMUNICATION ENGINEERING
ARTIFICIAL NEURAL NETWORKS (D47PE3)

B.Tech. VII Semester

L/T/P/C
3/0/0/3

Prerequisite: Calculus, Linear Algebra, Probability

Course Objectives:

1. To understand the biological neural network and to model equivalent neuron models.
2. To understand the architecture, learning algorithms
3. To know the issues of various feed forward and feedback neural networks.
4. To explore the Neuro dynamic models for various problems.

Course Outcomes: Upon completing this course, the student will be able to

1. Build the similarity of Biological networks and Neural networks
2. Practice the training of neural networks using various learning rules
3. Demonstrate the concepts of forward and backward propagations.
4. Practice Self Organization Maps
5. Construct the Hopfield models.

Course	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1		3	2	2									2	
CO2		3	2	2									2	
CO3		3	2	2									2	
CO4		2	2	2										
CO5		3	3	3										

UNIT-I:

Introduction: A Neural Network, Human Brain, Models of a Neuron, Neural Networks viewed as Directed Graphs, Network Architectures, Knowledge Representation, Artificial Intelligence and Neural Networks

Learning Process: Error Correction Learning, Memory Based Learning, Hebbian Learning, Competitive, Boltzmann Learning, Credit Assignment Problem, Memory, Adaption, Statistical Nature of the Learning Process

UNIT-II:

Single Layer Perceptrons: Adaptive Filtering Problem, Unconstrained Organization Techniques, Linear Least Square Filters, Least Mean Square Algorithm, Learning Curves, Learning Rate Annealing Techniques, Perceptron –Convergence Theorem, Relation Between Perceptron and Bayes Classifier for a Gaussian Environment

Multilayer Perceptron: Back Propagation Algorithm XOR Problem, Heuristics, Output Representation and Decision Rule, Computer Experiment, Feature Detection

UNIT-III:

Back Propagation: Back Propagation and Differentiation, Hessian Matrix, Generalization, Cross Validation, Network Pruning Techniques, Virtues and Limitations of Back Propagation Learning, Accelerated Convergence, Supervised Learning

UNIT-IV:

Self-Organization Maps (SOM): Two Basic Feature Mapping Models, Self-Organization Map, SOM Algorithm, Properties of Feature Map, Computer Simulations, Learning Vector Quantization, Adaptive Patter Classification

UNIT-V:

Neuro Dynamics: Dynamical Systems, Stability of Equilibrium States, Attractors, Neuro Dynamical Models, Manipulation of Attractors as a Recurrent Network Paradigm
Hop field Models–Hop field Models, restricted boltzmen machine.

TEXT BOOKS:

1. Simon S Haykin,"Neural Networks a Comprehensive Foundations", PHI Ed.
2. Jacek M.Zurada,"Introduction to Artificial Neural Systems", JAICO Publishing House ,Ed.2006.

REFERENCE BOOKS:

1. Li Min Fu,"Neural Networks in Computer Intelligence", TMH,2003.
2. James A Freeman David, MS Kapura,"Neural Networks", Pearson Ed., 2004.
3. B.Vegnanarayana,"Artificial Neural Networks", Prentice Hall of India, P.Ltd,2005.

B.TECH. ELECTRONICS & COMMUNICATION ENGINEERING
EMBEDDED C (D48PE5)

B.Tech. VIII Semester **L/T/P/C**
3/0/0/3

COURSE OBJECTIVES:

1. To explore the difference between general purpose programming languages and Embedded Programming Language.
2. To provide case studies for programming in embedded systems.

COURSE OUTCOMES:

1. Illustrate the basics of Embedded C with reference to 8051.
2. Operate how to handle control and data pins at hardware level.
3. Illustrate the objective nature of Embedded C.
4. Demonstrate the knowledge about real time constraints.
5. Apply the specifications of real time embedded programming with case studies.

Course	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2											2	
CO2	3	2											2	
CO3	3	2											2	
CO4	3	2											2	
CO5	3	2												

UNIT-I: Programming Embedded Systems in C:
Introduction, What is an embedded system, Which processors should you use, Which programming language should you use, Which operating system should you use, How do you develop embedded software, Conclusions.

Introducing the 8051Microcontroller Family: Introduction, What's in a name, The external interface of the Standard 8051, Reset requirements, Clock frequency and performance, Memory issues ,I/O pins, Timers, Interrupts, Serial interface, Power consumption, Conclusions.

UNIT-II: Reading Switches: Introduction, Basic techniques for reading from port pins, Example: Reading and writing bytes, Example: Reading and writing bits (simple version), Example: Reading and writing bits (generic version), the need for pull-up resistors, Dealing with switch bounce, Example: Reading switch inputs (basic code), Example: Counting goats, Conclusions.

UNIT–III: Adding Structure to your Code
Introduction, Object-oriented programming with C, The Project Header (MAIN.H), The Port Header (PORT.H), Example: Restructuring the 'Hello Embedded World' example, Example: Restructuring the goat-counting example, Further examples, Conclusions

UNIT–IV: Meeting Real-Time Constraints

Introduction, Creating hardware delays using Timer 0 and Timer 1, Examples on delay, timeouts, Conclusions.

UNIT–V: Case Study: Intruder Alarm System

Introduction, The software architecture, Key software components used in this example, running the program, the software, Conclusions.

TEXT BOOKS:

1. Michael J.Pont,"Embedded C",Pearson Education.

REFERENCE BOOKS:

1. Nigel Gardner,"PIC micro MCU C-An introduction to programming, The Microchip PIC in CCS C " .

1.1.3 Details of courses offered by the institution that focus on employability/ entrepreneurship/ skill development during the year.

1.2.1 Details of courses introduced across all programmes offered during the year

Name of the Course	Course Code	Activities/Content with a direct bearing on Employability/ Entrepreneurship/ Skill development	Link to the relevant document
Linear Algebra and Ordinary Differential Equations	D1BSM1	Skill development	
C Programming for Problem Solving	D1ESCP1	Employability	
Engineering Physics	D1BSEP1	Employability	
Electrical Circuits	D1ESEC1	Employability	
Engineering Physics Lab	D1BSEP2	Employability	
Basic C Programming for Problem Solving Lab	D1ESCP2	Employability	
Computer Aided Engineering Graphics	D1ESCEG	Employability	
Electrical Circuits Lab	D1ESEC2	Employability	
Mathematical Transforms	D2BSM3	Skill development	
Applied Chemistry	D2BSAC1	Skill development	
Network Analysis	D2ESNA1	Employability	
English for Skill Enhancement	D2HSE1	Employability	
Basic Workshop	D2ESBW1	Employability	
Applied Chemistry Lab	D2BSAC2	Skill development	
English Language and Communication Skills Lab	D2HSE2	Employability	
Network Analysis Lab	D2ESNA2	Employability	
Python Lab	D2ESPP1	Employability	
Environmental Science*	MC001	Skill development	
Complex Analysis andvector Calculus	D3BSM4	Skill development	
Power Systems-I	D23PC1	Skill development	
Analog Electronics	D23PC2	Employability	
Electrical Machines-I	D23PC3	Employability	
Electro Magnetic Fields	D23PC4	Employability	
Analog Electronics Lab	D23PC5	Skill development	
Electrical Machines Lab-I	D23PC6	Employability	

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Data Structures using C Programming Lab	D23PC7	Employability	
Solid Mechanics & Hydraulic Mechines	D4ESHM	Skill development	
Digital Electronics	D24PC8	Employability	
Electrical Mechines -II	D24PC9	Skill development	
Control System	D24PC10	Skill development	
Power System II	D24PC11	Skill development	
Digital Electronics Lab	D24PC12	Skill development	
Electrical Mechines -II Lab	D24PC13	Skill development	
Control System Lab	D24PC14	Skill development	
Constitution of India *	MC002	Skill development	
Power Electronics	C25PC1	Skill development	
Electrical Measurements and Instrumentation	C25PC2	Skill development	
Electrical Machine Design	C25PE3	Skill development	
Power System Dynamics and Control	C25PE3	Skill development	
Digital Signal Processing	C25PE3	Skill development	
Power System-II	C25PC4	Skill development	
Open Elective-I (Computer Networks)	C25OE5	Skill development	
Electrical Systems Simulation Lab	C25PC6	Skill development	
Power Electronics Lab	C25PC7	Skill development	
Advanced English Communication Skills Lab	CHSE3	Skill development	
Electrical Measurements andInstrumentation Lab	C25PC8	Skill development	
MOOCs/Online Course	MC005	Skill development	
Bussiness Economics And Financial Analysis	CHSM 1	Skill development	
Power System Protection	C26PC1	Skill development	
Power System Operation And Control	C26PC2	Skill development	
Microprocessors & Microcontrollers	C26PC3	Skill development	
(Professional Elective -II)Electrical Energy Conservation and Auditing	C26PE4	Skill development	
Computer Architecture	C26PE4	Skill development	
Line-Commutated and Active Rectifiers	C26PE4	Skill development	
(Open Elective -II) Renewable Energy Sources	C26PE5	Skill development	
Reliability Engineering	C26PE5	Skill development	
Optimization Techniques	C26PE5	Skill development	
Power System Lab	C26PC6	Skill development	

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Microprocessors & Microcontrollers Lab	C26PC7	Skill development	
PYTHON PROGRAMMING LAB	C26ES8	Skill development	
1. Personality Development/Skill Development 2. Technical Events 3. Internships	MC006	Skill development	
Hybrid Electrical Vehicles (HEV)	C27PE1	Skill development	
Industrial Electrical Systems Electrical Systems	C27PE1	Skill development	
Flexible AC Transmission Systems	C27PE1	Skill development	
HVDC Transmission Systems	C27PE2	Skill development	
Electrical Drives	C27PE2	Skill development	
Electromagnetic Waves	C27PE2	Skill development	
Operating Systems (Open Elective-III)	C27OE3	Skill development	
Fundamentals of Managemnet (FOM)	CHSM2	Skill development	
Electrical & Electronics Desing Lab	C27PC4	Skill development	
Comprehensive Viva/Test	C27PW5	Skill development	
Major Project Phase I	C27PW6	Skill development	
Competitive Exams	MC007	Skill development	
Cloud Computing (OE-IV)	C28OE1	Skill development	
Electrical Distribution Systems (PE-V)	C28PE2	Skill development	
Modern Control Theory	C28PE2	Skill development	
Computational Electromagnetics	C28PE2	Skill development	
Utilization of Electrical Energy (PE-VI)	C28PE3	Skill development	
High Voltage Engineering	C28PE3	Skill development	
Computer Aided Design of Electrical Machines	C28PE3	Skill development	
Major Project Phase - II	C28PW4	Skill development	

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Department of Information Technology

Introduction of New Courses during the year : 2023-24

Name of the Course	Course Code	Activities/Content with a direct bearing on Employability/ Entrepreneurship/ Skill development
Probability & Statistics (IIyear- Isem)	D3BSPS1	NA
Business Economics & Financial Analysis (IIyear- Isem)	D3HSBF	Entrepreneurship (Analyzing the financial statement of the company through various ratios)
Computer Organization and Architecture (IIyear- Isem)	D3ESCOA	Skill development (Understand the internal organization of a system)
Data Structures (IIyear- Isem)	D63PC1	Skill development (Analyze linear data structures and non-linear data structures)
Object Oriented Programming through Java (IIyear- Isem)	D63PC2	Skill development (Design GUI based applications)
Data Structures Lab (IIyear- Isem)	D63PC3	Employability (Apply data structures for solving real-world problems)
Object Oriented Programming through Java Lab (IIyear- Isem)	D63PC4	Employability (Develop GUI programs)
IT Essentials Lab (IIyear- Isem)	D3ESITE	Employability (Develop Web Applications)
Discrete Mathematics (IIyear- IIsem)	D64PC5	NA
Web Technologies (IIyear- IIsem)	D64PC6	Skill development (Create Dynamic Web pages, Make use of Express JS and and Node JS Frameworks)

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Name of the Course	Course Code	Activities/Content with a direct bearing on Employability/ Entrepreneurship/ Skill development
Operating Systems (IIyear- IIsem)	D64PC7	Skill development (Understand the performance of operating systems)
Database Management Systems (IIyear- IIsem)	D64PC8	Skill development (Understand the design of ER model,RDBMS and formulate SQL queries on the data, normalization and recovery techniques)
Design and Analysis of Algorithms (IIyear- IIsem)	D64PC9	Skill development (Analyze the performance of the algorithms)
Operating Systems Lab (IIyear- IIsem)	D64PC10	Employability (Develop Skills to operate various operating systems)
Database Management Systems Lab (IIyear- IIsem)	D64PC11	Employability (Design and implement a database schema for given problem and develop programs using PL/SQL)
Web Technologies Lab (IIyear- IIsem)	D64PC12	Employability (Develop Dynamic Web pages, Make use of Express JS and and Node JS Frameworks)
Data Warehousing and Data Mining (IVyear- Isem)	C67PC1	Skill development (Analyze methodologies used in data mining and data ware housing)
Information Security (IVyear- Isem)	C67PC2	Skill development (Understand the Policies, Guideline and Framework of Web Security)
Mobile Adhoc Networks (IVyear- Isem)	C67PE4	Skill development (Understands the principles of mobile ad hoc networks)
Internet of Things (IVyear- Isem)	C67PE5	Skill development (Develop web based services on IoT devices.)
Data Warehousing and Data Mining Lab (IVyear- Isem)	C67PC6	Employability (Make use of methodologies used in data mining and data ware housing)

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Name of the Course	Course Code	Activities/Content with a direct bearing on Employability/ Entrepreneurship/ Skill development
Storage Area Networks (IVyear- IIsem)	C68PE2	Skill development (Understands the different network storage options for different application environments.)
Semantic Web & Social Networks (IVyear- IIsem)	C68PE3	Skill development (Learn the various semantic web applications)

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8th BoS Meeting

Dt. 27.01.2024
(online Mode)

Agenda: 1. R22 Model curriculum and detailed Syllabus approvals for R22 III and IV years

2. Approval of R22 open Electives offered to other departments

3. Major changes of R22 Syllabus subject w.r.t R20 Syllabus

a) In Semester V, Title "Hydrology & water resources Engineering" has been renamed to "Water Resources Engineering-I"

b) In Semester V, in 'Design of reinforced concrete structures', Unit III & Unit IV are swapped

c) In Semester V, in 'Computer Aided Detailed Drawing Lab', three experiments are added and three experiments are removed w.r.t R20 syllabus to cover all the topics.

d) In semester VI, in 'Soil Mechanics' Unit II - "Critical Hydraulic gradient" topic is added.
In Unit V: in Types of laboratory tests for strength parameters; direct shear test, tri axial compression Test, Unconfined compression Test, Vaneshear

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test were included and "Skempton's pore water parameters" topic is added.

e) In semester VI, in 'Environmental Engineering", in Unit IV; "Wetland Management' topic is added and in Unit V: "Noise pollution: causes and effects of noise pollution - measurement of noise pollution, Standard values" is added.

f) In Semester VI, in "Design of steel structures", Unit III; plastic Theory - Theorem of plastic Analysis, plastic moment" are removed.

g) In Semester VI, in "Soil mechanics lab", experiment no. 1 has been modified to "Determination of Specific gravity of soil by pychometer".

h) In GIS lab (Geographic information system lab), 9 experiments were added in addition 5 experiments of R20 syllabus.

i) In Semester VII, in "Ground water Development and Management" (PE IV), in Unit IV, Aerial photogrammetry - Applications is removed.

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j) In Semester VII, in Environmental Engineering lab", Exp 16: "introduction to Bacteriological Analysis" is removed.

k) In Semester VIII, in "construction project planning Management", Unit V, occupational & safety hazard assessment" Topic is removed

Members present:

1. Dr. G.V. Narasimha Reddy - (University Nominee)
2. V. Sai Vikas - Chairman - V. Sai Vikas
3. K.V.R. Satya Sai - HOD/civil - "
4. Dr. CSV Subramanya Kumar - (Ext. Member)
5. Dr. Hari prasad - (Ext. Member)
6. M. Mallareddy - Ext. Member (from Industry)
7. B. Praveen - Member -
8. Md. Burhan Ahmed - Member -

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