Dr.D.NAGESHWAR RAO
M.TECH., Ph.D. MISTE.

Prof. and HOD,

Controller of Examinations

Electronics & Communication Engineering.

Areas of interest:

1. VLSI, SOC
2. Image Processing
3. Embedded system

1.Educational Qualifications:

S.No	Course of Study	Year of passing	Board/University	Class Obtained
1	Ph.D	10th Jan 2014	Gitam Univ. Vishakapatnam.	---------
2	M.Tech(DSCE)	2004	JNTU College of Engg.Hyd.	Ist class with Distiction.(75%)
3	B.E(Electronics)	1999	S.R.T.M.U Nanded (M.H)	Ist class with Distiction.(80%)

2.Employment Record : 13+ years Experience

S.No	College	Designation	Period
1	Vijaya Rural Engg., CollegeNizamabad.	Asst.Prof	1999-2003
2	KITS,Huzurabad	Asst.Prof	2003-2004
3	BIET, Hyd	Sr.Asst.Prof	2004-2005
4	NizamInst.OfEngg. & Tech.	Assoc.Prof	2005-2013
5	TKR College of Engg. & Tech.	Professor	July 2013- Till date

3. SoftwareKnown: MATLAB, SPICE, VHDL

4. Labs Established: 1. DSP Lab established at NIET in 2005.
Processor: TMS 320C6713, **Software:** CCS.

2. Cadence Lab established for M.Tech(VLSI) in 2011.

Conferences:

[1]. D.NageshwarRao, Dr.V.MalleswaraRao, Dr.S.VenkataChalam, presented a paper on **Low Voltage Low Power CMOS Operational Amplifier Input/Output Circuit Design** in International Conference on MEMS and Opto Electronics Technologies (ICMOT-2010) Organized by Swarnadhra College of Engg. and Tech., from 22-23 Jan,2010.

[2]. D.NageshwarRao, Dr.V.MalleswaraRao, Dr.S.VenkataChalam, presented a paper on **Various Design Techniques for Low Voltage Analog Circuits** at Shastipurthi National Conference Organized by ATRI, from 23-24 Oct, 2009.

[3]. M.A.Muqeet, D.NageshwarRao, M.A.Toefeeq Bilal published a paper on**Design of CMOS AnalogTelescopic OTA** In National Conference on Advances in Communication Technologies 2012, GITAM University . Page No.868-871.

[4]. D. NageshwarRao, Dr. V. MalleswaraRao, presented a paper on **Low Power Supply Voltage Using Bulk Driven Input Transistors for Biomedical Applications** at a National Conference in VLSI & Image Processing Organized by Velammal Engineering College, Chennai on 26 Sept, 2009.

6. SHORT TERM PROGRAMS/ WORKSHOP ATTENDED:

[1] Attended Workshop on "**EnterpreneurshipDevelepment**" organized by Nizam Institute ofEngg.and Tech., Deshmukhi,with NSIC LTD. on 22th March, 2012.

[2] Attended one day Training Program on "**Procurement Management Support System**"at JNTUH conducted by SPFU-Andhra Pradesh on 26 March 2012.

[3] Attended two day Training Program on "**e-FMR and Financial Management**" at Osmania University College of Engg. Hyd.,conducted by NPIU-New Delhi on 16th and 17th Feb 2012.

[4] Attended Workshop on "**New Criterion for NBA Accreditation**" organized by GNEC & GNIT on 16th and 17th at Guru Nanak Institutions Technical Campus, Ibrahimpatnam, HYD.

[5] Attended Workshop on "**EnterpreneurshipDevelepment**" organized by Nizam Institute ofEngg.and Tech., Deshmukhi,with NSIC LTD. on 22th March, 2012.

[6] Attended Workshop on "**Microwave Applications in R&D**" organized by Nizam Institute ofEngg.and Tech., Deshmukhi, on 26th Feb, 2010.

[7] Attended Workshop on "**Multi Layer PCB Design**" organized by ACE Engg. College, Department of ECE on 18th& 19th December, 2009.

[8] Attended Workshop on "**Analog & Mixed Signal Design**" organized by JNTU,HYD& Cadence Design Systems, Bangalore on 19th -21st August – 2009.

[9] Attended Workshop on "**Machine Learning & Soft Computing**" Organized byNIT, Warangal during 18th -30th May 2009.

[10] Attended Workshop on "**National Level Workshop on VLSI System Design**"Organized by CVSR College of Engineering, Hyderabad during May 2nd -3rd, 2008.

[11] Attended Short Term Course on "**Technology CAD for VLSI Design**" Organizedby IIT, Khargpur during June 4th to 7thJuly of 2007.

[12] Attended Short Term Course on "**DSP Architectures & Algorithms**" organized by NIT, Warangal during April, 2004.

7. Award: I have been awarded "Certificate of Merit" in NIET, 2007&2008.

8. Administrative Responsibilities:

1. Presently working as ECE HOD & Controller of Examinations
2. Incharge for Technical Exhibition at NIET in 2007 & 2008.
3. JNTUH Spot Valuation coordinator for the academic year 2010-2011.
4. TEQIP Coordinator for purchase committee in the college.
5. NBA ECE department Coordinator.
6. Guiding the B.Tech and M.Tech projects.
7. Work shop conducted on PCB Design and MATLAB for Image Processing in TKR CET.

9. Subjects Taught for B.Tech and M.Tech:

1. EDC, VLSI, DICA, DSP, EMWTL, AWP, STLD.
2. VLSI Design, Analog VLSI Design, Low Power VLSI.

10. ISTE MEMBERSHIP --------**LM68553.**

11. **Workshops Organized& Guest lecturers:**

1. 3-Day workshop on "PCB Design" in TKRCET, 5th -7th September, 2013.
2. 2-Day workshop on "Image Processing using MATLAB" in TKRCET, 27th-28th December, 2013.
3. Guest lecture delivered on "Low Power VLSI Design" at Anurag Group of Instutions, HYD.

D Nageshwarrao

TKR College of Engineering & Technology
vlsi
Image Processing

	All	Since 2014
Citations	21	16
h-index	2	2
i10-index	2	1

TITLE	CITED BY	YEAR
Implementation and simulation of CMOS two stage operational amplifier D Nageshwarrao, KS Kumar, YR Rao, G Jyothi International Journal of Advances in Engineering & Technology 5 (2), 162	10	2013
Gain boosted telescopic ota with 110db gain and 1.8 ghz. ugf D Nageshwarrao, D Chalam, VM Rao International Journal of Electronic Engineering Research 2 (2), 159-166	10	2010
A Comparative Study of Various Noise Removal Techniques using Filters DNRKS Rani Jounal of Engineering and Technology 7 (2), 88-93	1	2018
Design of FPGA based Cyber Secured Encoder for IOT DDN Rao Journal of Emerging Technologies and Innovative Research 4 (12), 564-567		2017
VLSI based Signal Processing Solution for Calculationof Sidelobe Amplitude in Pulse Compression DDNR Thudimilla Sadhana , P.Kalyani International Journal of Engineering Trends and Applications 4 (6), 33-38		2017
Improved Feature Extraction for Vehicle Number Plate Recognition KADNRD Ramakrishna Reddy International Journal of Emerging Technology and Advanced Engineering 7 (10 …		2017
Optimal Implementation of IP based Router with Shortest path Algorithm using VLSI Technology MSVRRDDN Rao International Journal of Electronics and Communication Engineering 10 (2), 63-70		2017
Area Delay Efficient FM0/Manchester Encoding Using SOLS Technique for Communication Applications DDN Thriveni Kunta, A Vikas International Journal of Eminent Engineering Technologies 4 (5), 279-286		2017
IMPLIMENTATION OF ENCODING SCHEME FOR POWER REDUCTION IN NETWORK ON CHIP LINKS K Gayathri, K Sukanya, DRD Nageshwarrao International Journal of Research in Advanced Engineering Technologies 5 (4 …		2016
High Speed Low Power MTCMOS D-Latch based 32 Bit Carry select adder using 10-T full adder DDNR S.Sneha, P.Kalyani International Journal of VLSI System Design and Communication Systems 4 (10 …		2016

TITLE	CITED BY	YEAR
FPGA Implementation of ALU using Fault Tolerant Reversible Logic DRDNR Rathin Kumar, P.Kalyani International Journal of Advanced Technology and Innovative Research 8 (12 …		2016
An optimized implementation of Pre-Encoded Multipliers Based on NR4SD Encoding technique for DSP/Multimedia applications B Mounika, DDN Rao International Journal of Research in Advanced Engineering Technologies 5 (4 …		2016
Design of 16-Bit Succesive Approximation A/ D Converter in 180nm CMOS Technology DN Rao Indian Technology Congress 2015, Bangalore.		2015
Design and Implementation of 64 set of Instruction set High performance Digital Signal Processor RR D.Nageshwar Rao International Journal & Magazine of Engineering, Technology, Management and …		2015
Design and Implementation of Serial port communication by using I2C Master Controller BK D.Nageshwar Rao International Journal & Magazine of Engineering, Technology, Management and …		2015
RADAR Scan Pattern synthesis and implementation on FPGA SPDRDN Rao International Journal of Scientific & Engineering Research 6 (6), 734-743		2015
Design of 10 Bit R/2R Digital to Analog Converter in 180nm CMOS Technology KRKR D.Nageshwar Rao International Journal of Applied Engineering Research 10, 26447-26453		2015
Design of 16-Bit Succesive Approximation A/ D Converter in 180nm CMOS Technology DN Rao Indian Technology Congress 2015, Bangalore.		2015
Application of Delta Sigma A/D Converter in 180nm CMOS Technology DN Rao Indian Technology Congress 2015, Bangalore.		2015
Low power high speed fully dynamic CMOS Latched Comparator MDNZB D.Nageshwar Rao, M.S.Sameera International Journal of Engineering Research and Development 10 (4), 01-06		2014