Dr. GIRISH KUMAR MEKALA

B. Tech, M. Tech, Ph.D. (NIT Hamirpur), MIEEE
Associate Professor
Department of ECE, TKRCET, Hyderabad.

Area of Interest:

- VLSI Interconnects
- 3D IC Packaging System
- Modeling of Carbon nanotubes and Graphene Nanoribbons
- Device Modeling

Academic Credentials

Course	Institution	Board/University	Year of Passed out
Ph.D.	NIT Hamirpur	NIT Hamirpur	2018
M.Tech	NIT Hamirpur	NIT Hamirpur	2011
B.Tech	Sai Spurthi Institute of Technology	JNTU Hyderabad	2008
Intermediate	Nalanda Residential Junior College	Board of Intermediate, A.P.	2004
10^{th}	Samatha Convent	Board of Secondary Education, A.P.	2002

Professional Experience

2017 (Oct.)- 2020 (Jul.) | **Associate Professor**
Worked as an Assoc. Professor in ECE Dept., VJIT, Hyderabad (Telangana).

2011 (Dec.)-2013 (Nov.) | **Assistant Professor**
Worked as an Asst. Professor in ECE Dept., AKGEC, Ghaziabad (UP).

List of Publications

- ***International Journals* (SCI and Scopus)**

1. **M. G. Kumar**, R. Chandel, and Y. Agrawal, "An Efficient Crosstalk Model for Coupled Multi-Walled Carbon Nanotube Interconnects," ***IEEE Transactions on Electromagnetic Compatibility***, vol. 60, no. 2, pp. 487-496, Apr. 2018. DOI: 10.1109/TEMC.2017.2719052 (Impact factor:1.882)

2. **M. G. Kumar**, Y. Agrawal, and R. Chandel, "Modelling and Performance Analysis of Dielectric Inserted Side Contact Multilayer Graphene Nanoribbon Interconnects," ***IET Circuits, Devices and Systems***, vol. 11, no. 3, pp. 232-240, May 2017. DOI: 10.1049/iet-cds.2016.0376 (Impact factor:1.290)
3. Y. Agrawal, **M. G. Kumar**, and R. Chandel, "Comprehensive Model for High-Speed Current-Mode Signaling in Next Generation MWCNT Bundle Interconnect Using FDTD Technique," ***IEEE Transactions on Nanotechnology***, vol. 15, no. 4, pp. 590-598, Apr. 2016. DOI: 10.1109/TNANO.2016.2558475 (Impact factor: 2.196)
4. Y. Agrawal, **M. G. Kumar**, and R. Chandel, "A Novel Unified Model for Copper and MLGNR Interconnects Using Voltage- and Current-Mode Signaling Schemes," ***IEEE Transactions on Electromagnetic Compatibility***, vol. 59, no. 1, pp. 217-227, Jul. 2016. DOI: 10.1109/TEMC.2016.2587821 (Impact factor:1.882)
5. **M. G. Kumar**, Y. Agrawal, and R. Chandel, "Carbon nanotube Interconnects- A promising solution for VLSI circuits," ***IETE Journal of Education* (*Taylor & Francis*)**, vol. 57, no. 2, pp. 46-64, Apr. 2016. DOI: 10.1080/09747338.2016.1158129
6. Y. Agrawal, **M. G. Kumar**, and R. Chandel, "A Unified Delay, Power and Crosstalk Model for Current Mode Signaling Multiwall Carbon Nanotube Interconnects," ***Circuits Systems and Signal Processing***, vol.37, no. 4, pp. 1359-1382, Apr. 2018. DOI: 10.1007/s00034-017-0614-6 (Impact factor:1.681)
7. Y. Agrawal, **M. Girish**, and R. Chandel, "An efficient and novel FDTD method based performance investigation in high-speed current-mode signaling SWCNT bundle interconnect," ***Sadhana***, vol.43, no. 11, Nov. 2018. DOI: 10.1007/s12046-018-0957 (Impact factor:0.849)

- ***Book Chapters***

1. **M. G. Kumar**, Y. Agrawal, and R. Chandel, "Stability Analysis of Carbon Nanotube Interconnects," in *Proc. 2nd ICICA* (*Book Chapter, Springer*), KCG College of Technology, Chennai, vol. 467, pp. 11-19, 2017.
2. Y. Agrawal, **M. G. Kumar**, and R. Chandel, "Time-domain analytical modeling of current-mode signaling bundled single-wall carbon nanotube interconnects," in *Proc. 2nd ICICA* (*Book Chapter, Springer*), KCG College of Technology, Chennai, vol. 467, pp. 1-9, 2017.
3. **M. G. Kumar**, R. Dhiman, Y. Agrawal, and A. K. Chandel, "Prospective Graphene based Through Silicon Vias in Three Dimensional Integrated Circuits," in *VLSI and Post-CMOS*

Electronics. Volume 2: Devices, circuits and interconnects, IET book chapter, chapter 11, Page 223-246, Oct 2019.

4. Y. Agrawal, R. Chandel, **M. G. Kumar**, and R. Parekh, "Prospective Current Mode Logic for On-chip Interconnects in Integrated Circuit Designs," in *VLSI and Post-CMOS Electronics. Volume 2: Devices, circuits and interconnects, IET book chapter*, Chapter 9, Page 173-200, Oct 2019.
5. **M. G. Kumar**, Y. Agrawal, and R. Chandel, "Performance Analysis of Mixed-Wall Carbon Nanotube Bundle Interconnects using Colliding Bodies Optimization Technique," in *Major Applications of Carbon Nanotube Field-Effect Transistors (CNTFET), IGI global*, Chapter 9, Page 189-211, Jan 2020.
6. Y. Agrawal, E. Maheshwari, **M. G. Kumar**, R. Chandel, "Emerging Graphene FETs for Next-Generation Integrated Circuit Design," *Nanoscale VLSI*, pp. 225-237, Oct. 2020.
7. T Pathade, Y Agrawal, R Parekh, and **M.G. Kumar**, "Prospective Incorporation of Booster in Carbon Interconnects for High-Speed Integrated Circuits," Advances in VLSI and Embedded Systems (Springer), pp. 273-278, Jan. 2021.

- ***International Conferences/National Conferences*** **(Scopus)**

1. **M. G. Kumar**, R. Chandel, and Y. Agrawal "Timing and Stability Analysis of Carbon Nanotube Interconnects," *in Proc. IEEE International Symposium Nanoelectronics Information Systems (INIS)*, pp. 308-313, Indore, MP, 21-23 Dec. 2015. DOI: 10.1109/iNIS.2015.43
2. Y. Agrawal, R. Chandel, and **M. Girish**, "Performance analysis of multilayer graphene nano-ribbon in current mode signaling interconnect system," *in Proc. IEEE International Symposium Nanoelectronics Information Systems (INIS)*, pp. 297-302, Indore, MP, 21-23 Dec. 2015. DOI: 10.1109/iNIS.2015.44
3. **M. G. Kumar**, Y. Agrawal, and R. Chandel, "CNT and GNR based VLSI interconnects," *in Proc. Int. Conf. on Emerging Paradigms & Practices in Global Technology, Management & Business Issues; and Review of Business & Technology Research*, vo1. 11, no. 1, NIT Hamirpur, HP, 22-24, Dec. 2014.
4. Y. Haritha, **M. G. Kumar**, Y. Agrawal, and R. Chandel, "Transient and Crosstalk Analysis of Dielectric Inserted MLGNR interconnects," *in Int. Conf. on IEEE Electrical Design of Advanced Packaging and Systems Symposium*, 2018 held at Chandigarh.
5. N Patel, Y Agrawal, R Parekh, **M. G. Kumar**, "Variability Analysis of On-chip Graphene Interconnects at Subthreshold Regime," *IEEE International Students' Conference on Electrical, Electronics and Computer Science* (SCEECS), 2020 held at Bhopal.

Personal Achievement

- Received amount of Rs. 1,00,000/- from **DST-NIMAT** to conduct Entrepreneurship Awareness Camp (EAC**)** 2018-19, Sanction order: **EDII/DST-NIMAT/18-19/EAC-63**.
- **GATE-2009** qualified in Electronics and Communication Engineering discipline.
- Attended several workshops, international and national conferences.

Membership of Professional Bodies

- IEEE member since year 2015 (Member ID 93852256).
- Member of IEEE Electronic Device (ED) society since year 2015.
- IEEE student branch counselor since August 2018 (branch code STB14421).

Reviewing Activities

Reviewing paper for the following internationally referred journals:

- IEEE Transactions on Nanotechnology
- IEEE Transactions on VLSI systems
- IEEE Transactions on Electromagnetic Compatibility
- Journal of Nanoelectronics and Optoelectronics
- Journal of Nuclear Science and Techniques
- IET Circuit, Devices and Systems
- International Journal of Circuit Theory and Applications

Workshop and Short Term Courses Conducted

- As a program coordinator, conducted 3 days program on "**Entrepreneurship Awareness Camp (EAC)**" held at VJIT, Hyderabad under **DST-NIMAT 2018-19**.

Workshop and Short Term Courses Attended

- Short term course under TEQIP-II (6 days) on "***Advances in Design Techniques for Low Power VLSI & MEMS Systems***" held at National Institute of Technology Hamirpur, Himachal Pradesh, India.

- INUP familiarization workshop (2days) on "***Nanofabrication Technologies***" held at National Institute of Technology Hamirpur, Himachal Pradesh, India.

- IEEE CAS workshop (2 days) on "***Advanced Topics in VLSI Circuit design***" held at Indian Institute of Technology Roorkee, Uttarakhand, India.

- International seminar (3 days) on "***Design Techniques for Low Power Integrated Systems***" held at National Institute of Technology Hamirpur, Himachal Pradesh, India.