K. PADMAJA DEVI,
B.TECH. M.TECH., (Ph.D.)
Assoc. Professor, TKRCET, Hyderabad
MIETE, MISTE
Electronics & Communication Engineering

Areas of Interest:

1. Digital Image processing
2. Digital Design Through Verilog
3. Microwave Engineering
4. Digital System Design
5. Design of Fault Tolerant systems

- Educational & Professional

- **Academic Qualifications**
- Pursuing Ph.D. in Digital Image Processing, SSSUTMS, BHOPAL (2015-2019)
- M.Tech. In Digital Systems & Computer Electronics, JNTUCEH, Kukatpally, Hyderabad
(2002-2004)
- B. Tech. in ECE, JNTU, Anantpur (1995-1999)

Professional Experience

- **At TKRCET**
- Associate Professor, TKR college Of Engineering, Hyderabad (2010-2019)
- Assistant Professor, TKR college Of Engineering, Hyderabad (2006-2010)
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- **At JNTUH**
- Lecturer/Teaching Assistant, JNTU College of Engg. Hyderabad (2005 - 2006)

- **Publications**

National Journals

Study on Automatic extraction of water bodies from LANDSAT Imagery
K. Padmaja Devi, R. Mohan Kumar
International Journal OF Multi disciplinary, e-ISSN 2455-3085, volume 4, Issue-05 2019

Automatic extraction and characterization of vegetation structures for agriculture and food processing using image processing algorithms
K. Padmaja Devi, R. Mohan Kumar
International Journal of Scientific Research and Review ISSN NO: 2279-543X 2019

Smart campus project design and implementation on IoT platform using raspberry pi by python approach
V. Suresh Gopi, V. Bilhani, S. Hemanth Sai, K. Padmaja Devi
International Journal of Management, Technology And Engineering, ISSN NO : 2249-7455, Volume IX, Issue IV, APRIL/2019 2019

Application of Digital Image Processing Algorithms in agriculture & food processing Techniques
K. Padmaja Devi, IJERMCA, ISSN 2319-7471, volume- 6, Issue-11 2017

Image Processing In Food Industry/Processing
K. Padmaja Devi, IJATIR 9 (02), 0401-0402 2017

Novel VLSI Architecture For Sorting W Max/Min Values
AR Humera, K. Padmaja Devi , IJPRES 5 (1), 90-96 2015

Design and VLSI Implementation of Arithmetic Operation using Quaternary Signed Digit Number System
K. Padmaja Devi, J. Uma Maheshwar
International journal for vlsi system design and communication systems 3 (04 …

Design Of Area Efficient FM0/Manchester Encoding Technique Using SOLs
K. Padmaja Devi, Mukkera Gouthami
INTERNATIONAL JOURNAL OF RESEARCH 4 (2), 18-27 2015

Design and Implementation of High Speed Double Precision floating point multiplier
K. Padmaja Devi, S. Vijay, IJOEET 1 (4), 20-23 2014

Development of Verification Environment for SPI using OVM
K. Padmaja Devi, K. Nagarjuna, IJSETR 3 (29), 5891-5895 2014

Designing of BISR technique for Multiblock Memory Along Resource Sharing Algorithm
K. Padmaja Devi, R. Srinu, IJVDCS 2 (06), 436-439 2014

Multi bit error detection and Correction architecture for motion estimation in video coding systems
DKY S. Surekha, K. Padmaja Devi, IJSTER 3 (8), 505-510 2014

Design and Implementation of Online BIST for Different Word Sizes of Memories
Muneera Jamal, K. Padmaja Devi 2014

FPGA implementations of Humming bird Cryptographic Algorithm
Jella Sandhya, K. Padmaja Devi
IJSETR 2 (11), 1127-1132 2013

High Speed Signed Multiplier for DSP Application
K. Padmaja Devi, T. Ganga Bhavani
International journal for scientific engineering technology research 2 (07 …
2013

National Conference

K. Padmaja Devi, Automatic Extraction and characterization of vegetation structures for image processing algorithms, ICEAESTPHM, 2019
K. Padmaja Devi, A Survey of Image processing techniques for plant extraction and segmentation in the field, ICRTEPSTHM, 2018

Organized

- Organized a workshop on Digital Image Processing Using MATLAB (2013)

Participated workshops:

- Two day workshop on IoT based Home Automation using RASBERRY-Pi, TKRCET 2018
- Two day workshop on PCB Design. TKRCET 2017
- One day workshop on PYTHON, TKRCET 2017.
- Robo Genesis, TKRCET 2016.
- Data Networking, Routing & Switching, TKRCET 2015.
- Embedded & VLSI Design, TKRCET 2014.
- Digital Image Processing using MATLAB, TKRCET 2013
- PCB Design, TKRCET 2013
- Animation & Game Design, TKRCET 2013.

- Participated FDP:
- Teaching Pedagogy, programme "Education Objectives" TKRCET, 2018 December.
- Design of Experiments using Taguchi Approach, TKRCET, 2018 December.
- ANN for Misuse Detection, TKRCET, 2017.
- Virtual Retinal Display, TKRCET, 2016
- Research Awareness in Advanced VSI Design, TKRCET, 2015.
- Modern Teaching Trends in Scientific and Technical Education, TKRCET, 2014.
- FDP on Entrepreneurship, August-2013

- **Teaching**
- ***M.Tech.(DSCE, ECE)***
- Design of Fault Tolerant Systems
- Digital System Design
- Design for Testability

- ***B.Tech.***
- Digital IC applications using VHDL
- Digital Image Processing
- Microwave Engineering
- Antenna & Wave Propagation
- Embedded Systems
- Digital Design through Verilog
- Control Systems
- Electronic Devices & Circuits

Laboratory

- Established
  - **Cadence (VLSI)** Lab with permanent license
  - **DSP & Basic Simulation (MATLAB)** Lab with Permanent License
  - **AE/ECA (Multisim)** software Lab with Permanent License
  - **Verilog/VHDL (ECAD/VLSI Lab)** Software with Permanent License

- **Department Level Activities**
- Mini & Major Project Coordinator (2006 to Till Date)
- Active Member in NBA, NAAC & Autonomous Committees
- Coordinator for 1st year Orientation Program
- Prathibha Coordinator
- ECTA coordinator
- Coordinator For Comprehensive viva
- Coordinator for Technical Seminars
- Time-Table Coordinator

Society Level Activities

- Annual Day Coordinator
- Cultural Coordinator
- Hospitality Committee for society activities like NBA, NAAC & Autonomous committee
- **Active member in all society related activities**

Project Guidance (M.Tech. & B.Tech.)

- **Students**

Student Name	TITLE	Year
J.UMA MAHESHWAR	BIT MAC USING VEDIC MULTIPLIER	2015
AMATUR RAHMAN HUMERA	A PARALLEL RADIX SORT BASED VLSI ARCHITECTURE FOR FINDING THE FIRST W MAXIMUM/MINIMUM VALUES	2015
M.GOUTHAMI	FULLY REUSED VLSI ARCHITECTURE OF FMO/MANCHESTER ENCODING USING SOLS TECHNIQUE FOR DSRC APPLICATIONS	2015
SALIGANTI VIJAY	DESIGN AND IMPLEMENTATION OF HIGH SPEED DOUBLE PRECISION FLOATING POINT MULTIPLIER	2014
R. SRINU	GLOBAL BUILT-IN SELF REPAIR FOR 3D MEMORIES WITH REDUNDANCY SHARING AND PARALLEL TESTING	2014
BURRI NIKITHA	AN OPTIMIZED IMPLEMENTATION OF MAC UNIT USING SPST IN FPGA TECHNOLOGY	2014
K. NAGARJUNA	DEVELOPMENT OF VERIFICATION ENVIRONMENT FOR SPI MASTER INTERFACE USING SYSTEM VERILOG	2014
JAMAL MUNEERA	DESIGN & IMPLEMENTATION OF ONLINE BIST WITH DIFFERENT SIZES OF MEMORIES	2014
K. NAVEEN CHAUHAN	DESIGN & ASSERTION BASED FORMAL VERIFICATION OF A NOVEL AUTOMATED STIMULUS GENERATION METHODOLOGY FOR RTL DESIGN	2013
S. NARESH	A NOVEL APPROACH OF REPAIR IN BISR FOR SRAM'S WITH SELECTABLE REDUNDANCY	2013
T.GANGA BHAVANI	A FIXED POINT MULTIPLIER ARCHITECTURE FOR FAST MULTIPLICATION USING UT VEDIC PRINCIPLES AND PIPELINING	2013
JELLA SANDHYA	FPGA IMPLEMENTATION OF HUMBIRD	2013

S. SRAVYA REDDY SURABHI THARUNI T DEVAMANI	IRIS RECOGNITION FOR BIO-METRIC IDENTIFICATON	2014
G. VAMSHI G. PRUDHVI A. SATEESH	INDUSTRIAL MONITORING & CONTROLLING THROUGH SMS ALERT USING GSM	2016
P. RAMESH R. NAVEEN KUMAR	E-VOTING SYSTEM USING GSM MOBILE SMS	2015
M. SAI SREE S. NILAVARDHAN REDDY Y. KAMAL KAUSHIK	RANGE ESTIMATION OF NON-FLUCTUATING TARGETS USING MONO STATIC PULSE RADAR	2015
V. JEEVAN KUMAR	WIDE BAND WAVERORM GENERATION ON SDR PLATFORM	2015

Guided & still guiding around 150 UG students in major and mini projects in various fields

Contact :

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Alternate Email:
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