

Dr.B SWAPNA RANI
Ph.D,
Professor, ECE Department.

Areas of interest:

**VLSI** 

#### Academic Qualification:

- Ph.D. in VLSI, SSSUTMS, Sehore, Madhya Pradesh (2019).
- M.tech in DSCE (ECE), JNTUA, Anantapur (2010).
- B.E. in EIE, GITAMS, Visakhapatnam.(2005)

#### Professional Experience:

- Professor TKR College of Engineering & Technology (2019November –till date)
- Associate Professor, TKR College of Engineering & Technology (2010-2019 October)
- Assistant Professor, TKR College of Engineering & Technology (2006-2010)
- Assistant Professor, Indur Institute of Engineering & Technology (2005-2006)

# Paper publications:

- A Research paper entitled "Integration of Benes switching and Cell Scheduling algorithm for Fabric using VLSI" is selected for publishing in "International Journal of Advanced Research Foundation (IJARF)" Volume 3, Issue 8, August 2016 ISSN: 2394-3394.
- A Research paper entitled "Estimation and Analysis of switching activities in VLSI circuits" is selected for publishing in "International Journal of Enhanced Research in Management and Computer Applications (IJERMCA)" Volume 6, Issue 11, NOV 2017 ISSN: 2319-7471.
- A Research paper entitled "Study on Scheduling algorithm for Fabric using VLSI" is selected for publishing in "Research Review on International Journal(RRIJ)" Volume 4, Issue 5, May 2019 ISSN: 2455-3085.
- A Research paper entitled "Design & characterization of Combination & Integration of Benes switching and Cell Scheduling algorithm for Switching Fabric using VLSI" is selected for publishing in "International Journal of Scientific Research and review(IJSRR)" Volume 3, Issue 8, May 2019 ISSN: 2279-543X.
- A Research paper entitled "An Area Delay Efficient Design Of Fam Using Modified Booth Recoder", JUOEET, July 2015
- A Research paper entitled "*Design and Development of AFDX Transmitter Schedular*, IJMETR". June 2015.

#### Conferences:

- Presented paper entitled "Reliability study and Analysis of Nanoscale Circuits and Systems" in "International Conference on Advance Studies in Engineering and Sciences" held on Dec 2<sup>nd</sup> 2017.
- Presented paper entitled " Combination & Integration of Benes switching and Cell Scheduling algorithm for Switching Fabric using VLSI" "in "ICRTEPSTHM 2018" held on 30th SEP 2018 organized by IJAMSR.
- Presented paper entitled "Comparative study of Benes switching and Cell Scheduling algorithm for Switching Fabric using VLSI" in "ICRTEPSTHM 2019" held on 27th Jan 2019 organized by IJAMSR.
- Participated FDP:
- Teaching Pedagogy, programme "Education Objectives" TKRCET, 2018 December.
- Design of Experiments using Taguchi Approach, TKRCET, 2018 December.
- ANN for Misuse Detection, TKRCET, 2017.
- Virtual Retinal Display, TKRCET, 2016
- Research Awareness in Advanced VSI Design, TKRCET, 2015.
- Modern Teaching Trends in Scientific and Technical Education, TKRCET, 2014.
- Electro Magnetic Theory & Transmission Lines with Emphasis on MATLAB & ANSYS, Geethanjali College of Engg. & Tech. ,2014.
- Research Methodology, Gitam, 2013.
- ARM CortexM3 Architecture, SNIST, 2013

### Participated workshops:

- Two day workshop on IoT based Home Automation using RASBERRY-Pi, TKRCET 2018
- Digital System Design using FPGA & Simulink, CVRCoE, 2017.
- Two day workshop on PCB Design. TKRCET 2017
- One day workshop on PYTHON, TKRCET 2017.
- Robo Genesis, TKRCET 2016.
- Data Networking, Routing & Switching, TKRCET 2015.
- Embedded & VLSI Design, TKRCET 2014.
- Digital Image Processing using MATLAB, TKRCET 2013
- PCB Design, TKRCET 2013
- Aniamtion & Game Design, TKRCET 2013.

### Organized:

- Organized and attended workshop on "ARM based Embedded Processing" in August, 2015.
- Organized ECTA in October, 2016 & 2017.

# Teaching:

Electronic Devices and Circuits, Analog Electronics, Microprocessors and Microcontrollers, LDIC, DICA, LICA, EMI, MPI,.

## Positions held at TKRCET:

- Annual day coordinator since 2012.
- Bathukamma coordinator since 2017.
- BoS member since 2017.
- UG Project coordinator since 2012.

# Projects guided:-

- 30+ projects were guided under UG level
- 5+ projects were guided under PG level

## Contact:

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Electronics and Communication Engineering,

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