



R18 Regulation

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A' Grade)

Subject code: 2P3FC

B.Tech III Semester Regular/Supplementary Examinations, February 2021

DIGITAL LOGIC DESIGN
(Information Technology)

Maximum Marks: 70

Date: 22.02.2021 Duration: 3 hours

- Note:**
1. This question paper contains two parts A and B.
 2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
 3. Part B consists of 5 Units. Answer any one full question from each unit which carries 10M.
 4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks (10x2M=20 Marks)

- 1 Convert following hexadecimal to decimal numbers.
(i) $F28_{16}$ (ii) $BC2_{16}$.
- 2 State and prove the distributive property of Boolean algebra.
- 3 Implement OR gate using NAND gates only
- 4 Define sum of products and product of sum.
- 5 Draw the logic circuit of a full adder and give its truth table.
- 6 Define a combinational circuit, give its block diagram.
- 7 Differentiate between a latch and a flip flop.
- 8 Show the excitation table and truth table of JK flip flop.
- 9 Explain the concept of bidirectional shift register
- 10 Explain ROM? What are the types of ROMs?

Part-B

Answer All the following questions. (10MX 5=50Marks)

- 11 A. Convert the following to the corresponding bases (5M)
(i) $(9BCD)_{16} = ()_8$
(ii) $(323)_4 = ()_5$
B. What are the various logic gates, give the representation along with the truth table. (5M)
- OR
- 12 A. Simplify the following Boolean expressions using the Boolean theorems.
(i) $(A+B+C)(B'+C)+(A+D)(A'+C)$
(ii) $(A+B)(A+B')(A'+B)$ (5M)
B. The Hamming code 010110110 is received at the receiving end. Correct the received data if there is any error. (5M)
- 13 Simplify the following Boolean functions, using a four variable Karnaugh map method and implement the simplified function using NAND gates. (10M)
 $F(A,B,C,D) = \Sigma(0,2,4,5,6,7,8,10,13,15)$

OR

- 14 Why a NAND and NOR gates are known as universal gates? Simulate all the basic Gates. (10M)
- 15 A. What is a decoder? Construct a 4×16 decoder with two 3×8 decoders. (5M)
B. Design 2 bit Magnitude Comparator and explain in detail. (5M)
- OR
- 16 A. Design a full binary adder with two half adders and a OR gate. (5M)
B. Draw the logic diagram of 8:1 MUX using 2:1 MUX. (5M)
- 17 A. Explain the operation of SR Flip – Flop using Truth table? (5M)
B. What is a shift register? Explain about the following modes of operations in a four bit shift register. (5M)
(i) Shift right (ii) Shift left (iii) Bidirectional.
- OR
- 18 A. What is a master slave flip flop? Design a clocked master slave JK flip flop (5M)
B. Draw the circuit diagram of a 3-bit binary synchronous up counter. (5M)
- 19 A. Draw and explain the block diagram of PLA. (5M)
B. What are sequential programmable devices?. (5M)
- OR
- 20 A. Compare PLA with PAL with examples? (5M)
B. What do you mean by register transfer? Explain in detail. (5M)