

UNIT - I: DIODE CHARACTERISTICS & APPLICATIONS

PN junction diode - $V-I$ characteristics

Diode resistance and capacitance

Diode models - ideal, simplified, piecewise linear

Rectifiers - half wave, full wave [center-tap & bridge]

Capacitor filter for Rectifiers

clippers and clampers

Zener diode - $V-I$ characteristics and V/g regulation

Introduction:

Electronics: It controls the flow of e^- s using semiconductor materials.
→ signal controls → control - devices (Diode, transistor)
Electrical: It is a power handling → power → machines (Generator, transformer)

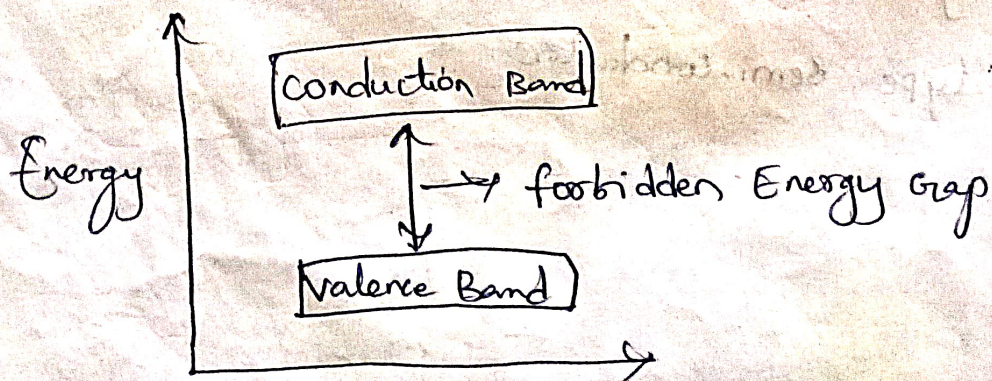
Energy Bands:

→ Energy Bands are the ranges of energy levels that e^- s may occupy in a solid materials.
→ 3 types: ① valence Band ② conduction Band ③ forbidden energy gap

① valence Band: It is associated with the valence e^- s.
→ where e^- s stay normally & cannot move easily.
→ valence Band e^- s are bound e^- s & it has low energy.
→ It can not participate in flow of current

② conduction Band: conduction band associated with the free e^- s. & it can participate in flow of current.
→ where e^- s can move freely. [free e^-] & higher energy

③ forbidden Energy Gap: it is the gap b/w the valence & conduction Band is forbidden energy gap



* Semi-conductor:-

→ A Semiconductor is a material whose electrical conductivity lies between a conductor and insulator.
↓ allow current ↓ Blocks current

→ Semi-conductor is of 2 types. i.e.,

① Intrinsic semi-conductor

② Extrinsic semi-conductor

* Intrinsic semi-conductor:- pure form of semi-conductor

* Extrinsic semi-conductor:- Adding of impurities to the intrinsic semi-conductor.

→ The Impurities are holes and electrons.

→ Extrinsic semi-conductors are divided into 2 types

① p-type semi-conductors:

② n-type semi-conductors:

* p-type semi-conductors:-

→ The majority charge carriers are the holes and minority charge carriers are electrons.

→ Trivalent impurities are added to the p-type semi-conductor

eg:- Boron (B), Aluminium (Al), Gallium (Ga), Indium (In)

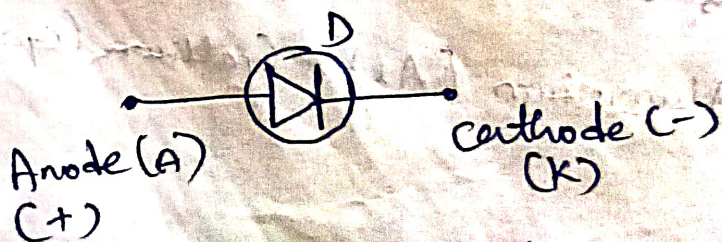
* N-type Semi-conductors :-

- The majority charge carriers are the electrons and minority charge carriers are holes.
- pentavalent impurities are added to the n-type Semi-conductor.

eg:- Phosphorus (P), Arsenic (As), Antimony (Sb), Bismuth (Bi)

* Diode :-

- It is a two-terminal semi-conductor device and it allows the current only in one direction.
- One terminal is anode (+) and one terminal is cathode (-).
- The direction of the current is decided by the polarity of the applied voltage.
- when we apply positive voltage at that time the current will flow.
- when we apply negative voltage it will not allow the flow of current.



Diode symbol

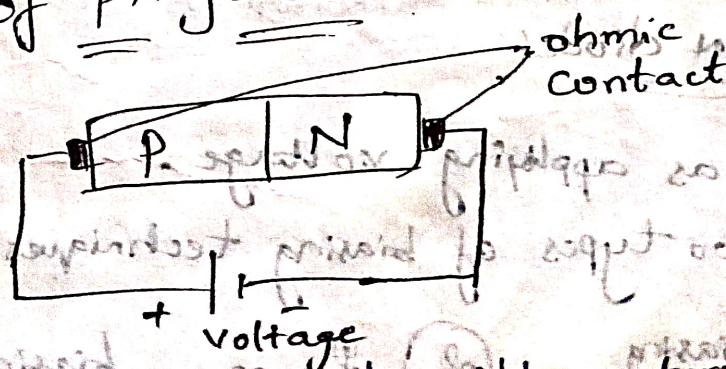
* Applications of a diode:

- Rectifier
- Amplifier
- Switch
- Voltage Regulator
- Oscillator

* P-N-junction diode:

- In a p-type material holes are the majority charge carriers and electrons are the minority charge carriers.
- In a n-type material electrons are the majority charge carriers and holes are the minority charge carriers.
- P-type materials are combined with n-type materials at that time one junction is formed at $x=0$ (equilibrium state) that junction is called PN-junction.
- The interface between two regions is called Metallurgical region (or) PN junction.

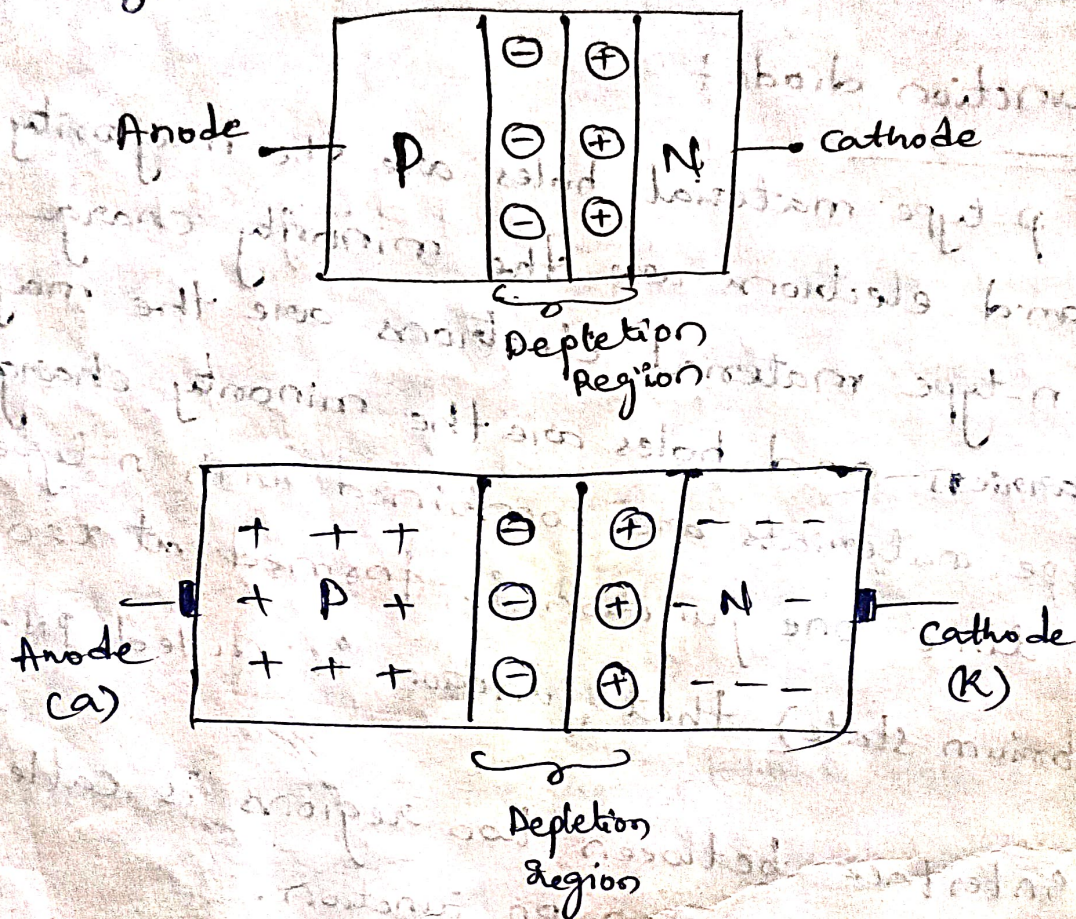
* Schematic of PN junction:



ohmic contact :- To connect with external devices.

Formation of a depletion layer or region / Depletion Region

Due to the force of attraction holes are moving into n-region and electrons are moved into p-region, at this time due to the recombination of majority carriers ions are produced nearer the junction this is known as depletion region.

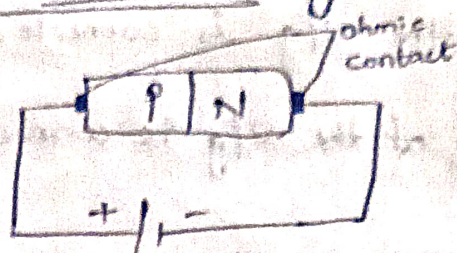


Formation of PN junction and Depletion Region

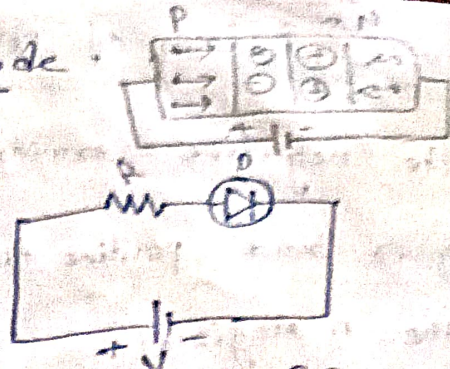
* Biasing in PN Diode

- It is known as applying voltage.
- There are two types of biasing techniques, they are
 - ① forward biasing
 - ② Reverse biasing

① forward biasing of PN diode



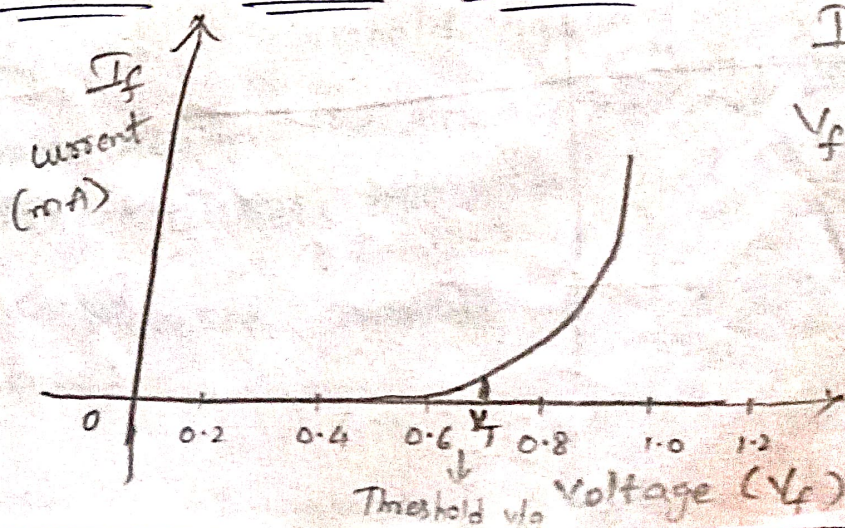
Schematic F.B



Symbolic F.B

- Positive terminal of the V/g is connected to the P-region & negative terminal of the V/g is connected to n-region.
- The forward V/g increases at the holes in a p-region is repelled with positive terminal of the voltage and moved to n-region.
- The electrons in n-region is repelled with -ve terminal of the voltage and moved into p-region thus, the depletion region decreases.
- when applied V/g is less than threshold voltage (V/g) [cut-in voltage] there is no current conduction
- when applied V/g is greater than threshold V/g at that time only current conduction is possible.

V-I characteristics of forward biasing :-



$I_f \rightarrow$ forward current
 $V_f \rightarrow$ forward voltage

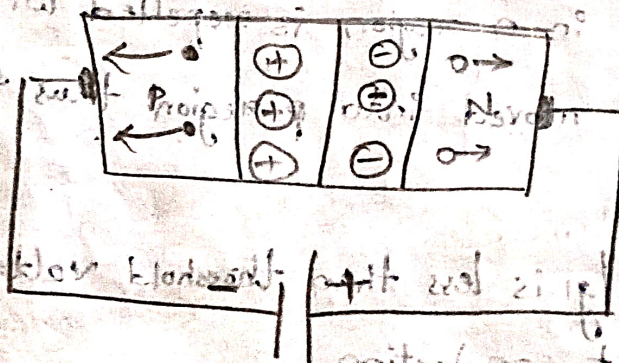
② Reverse Biasing of PN Diode

→ The negative terminal of the V/g is connected to the P-region and positive terminal of the V/g is connected to the n-region.

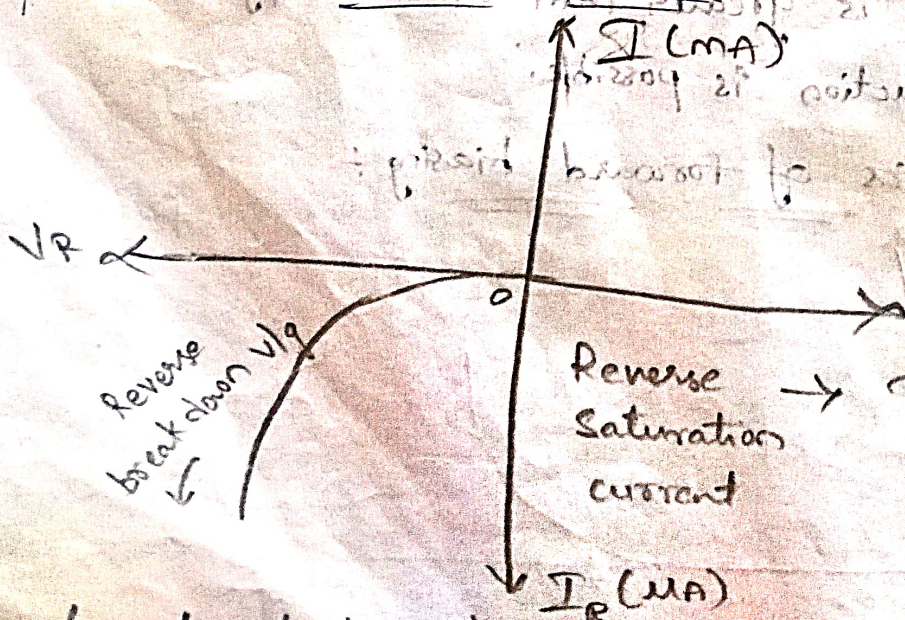
→ The holes in a p-region attracted with -ve terminal of the V/g then holes are moved away from the junction.

→ The e^- s in a n-region with +ve terminal of the voltage attracted then e^- s are moved away from the junction.

Thus depletion layer increases.



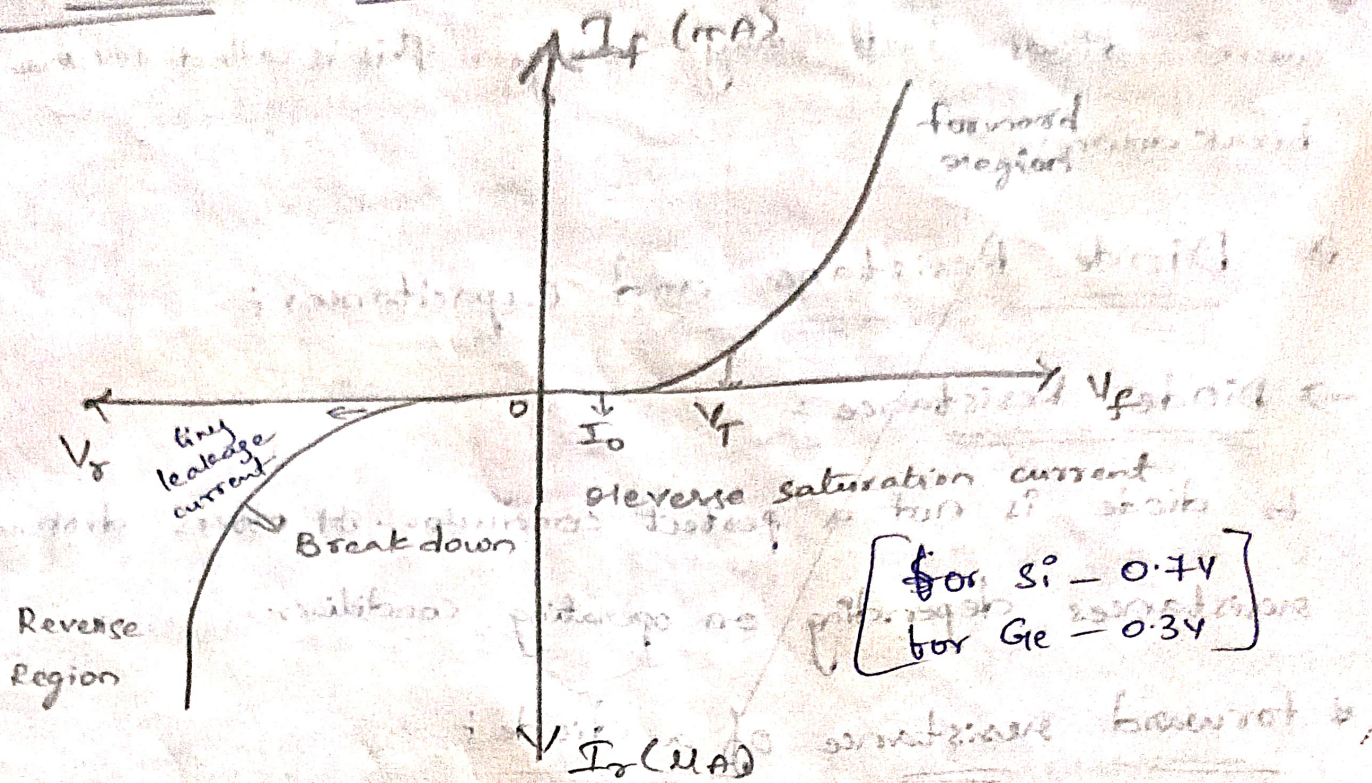
V-I characteristics of Reverse bias



Reverse Saturation current → The current flowing a Reverse bias condition.

The V/g at which sudden increases in current takes place

V-I characteristics of a diode [PN diode]



- I_f → forward current
 - I_r → Reverse current
 - V_T → Threshold v/g
 - V_f → Forward v/g
 - V_r → Reverse v/g
 - In a forward region applied v/g is less than threshold v/g there is no flow of current through the diode.
 - Applied v/g is greater than the threshold v/g there is flow of current through the diode. Then current increases exponentially after threshold v/g only.
 - In a Reverse region the reverse current flows due to the minority charge carriers which are used in very small number then the reverse current is also small.
- [Notes we have to explain about F.B & R.B]

→ If we increase the v/g beyond the limit, current flows diode may damage. This is called reverse break down.

* Diode Resistance and Capacitance :-

→ Diode Resistance :-

A diode is not a perfect conductor, it offers different resistances depending on operating condition.

→ It is of 3 types of resistance :-

① Static or DC resistances

② Dynamic or AC resistances

③ Reverse resistance

① Static or DC Resistance :-

It is the opposition to DC current, calculated by the ratio of DC voltage to DC current through the diode.

It is denoted with R_{dc} .

$$R_{dc} = \frac{V_{dc}}{I_{dc}}$$

② Dynamic or AC resistance :-
It is the opposition to AC current, determined by the change in voltage over the change in current through the diode.

$$R_{ac} = \frac{\Delta V_{ac}}{\Delta I_{ac}} = \frac{dv}{di}$$

In forward bias (above cut-in v/g), this resistance is very small (a few ohms).

③ Reverse Resistance (R_r) :-

→ when the diode is reverse biased, the resistance offered is very high (in mega ohms), since only a very tiny leakage current flows.

$$R_r = \frac{V_r}{I_r}$$

$R \rightarrow$ Resistance

$V \rightarrow$ voltage

$I \rightarrow$ current

$R_r \rightarrow$ Reverse resistance

$V_r \rightarrow$ reverse v/g

$I_r \rightarrow$ reverse current

$dv \rightarrow$ change in v/g
 $di \rightarrow$ change in current.

* Diode capacitance *

Diode equation:

$$* I = I_0 \left[e^{\frac{V}{\eta V_T}} - 1 \right] *$$

$I_0 \rightarrow$ Reverse saturation current

$V_T \rightarrow$ Threshold v/g

$\eta \rightarrow$ ~~1 or 2~~

$T \rightarrow$ Temperature in $^{\circ}K$ [$\therefore T = 273 + ^{\circ}C$]

$\eta = 1$ for silicon

$\eta = 2$ for germanium

V_T for silicon is 0.6

V_T for Ge is 0.3

$$I = I_0 \left[e^{\frac{V}{\eta V_T}} - 1 \right] \rightarrow \text{Diode equation}$$

Diode Capacitances:

→ A diode is not just a switch, it also behaves like a capacitor because of the charge storage at the PN junction.

→ There are two types of diode capacitances.

① Transition or Junction capacitances (C_T):

② Diffusion or Storage capacitances (C_D):

* ① Transition or Junction Capacitances (C_T):

→ In the transition capacitances the diode is in reverse biased condition, here the depletion region acts like dielectric and the P & N regions acts like the capacitor plates.

→ we have two conducting plates, p-type is plate-1 and n-type is plate-2 are two conducting materials b/w them.

→ More charges in a depletion region then capacitances also increases. Depletion region increases.

→ In depletion region, the electric charges (+ve & -ve regions) do not move from one place to another place. However, they exert electric field.

→ we know that capacitances means the ability to store electric charge.

→ In a Note we have to explain about Reverse biasing]

→ In a forward biased ~~bi~~ diode, the transition capacitance exist.

→ The transition capacitance is very small compared to the diffusion capacitances.

→ Hence transition capacitances is neglected in forward biased diode.

→ * The change of capacitances at the,

* Defination of Transition Capacitances

* The change in electric charge to the change in applied voltage.

$$C_T = \frac{dq}{dv} \Rightarrow \frac{\text{change in electric charge}}{\text{change in applied } v/g}$$

where,

C_T = Transition capacitances

dq = change in electric charge

dv = change in applied v/g

The transition capacitances can be mathematically written as

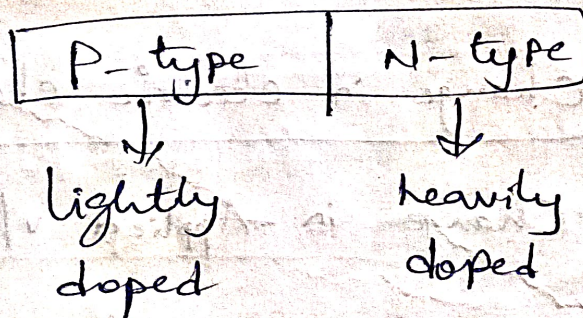
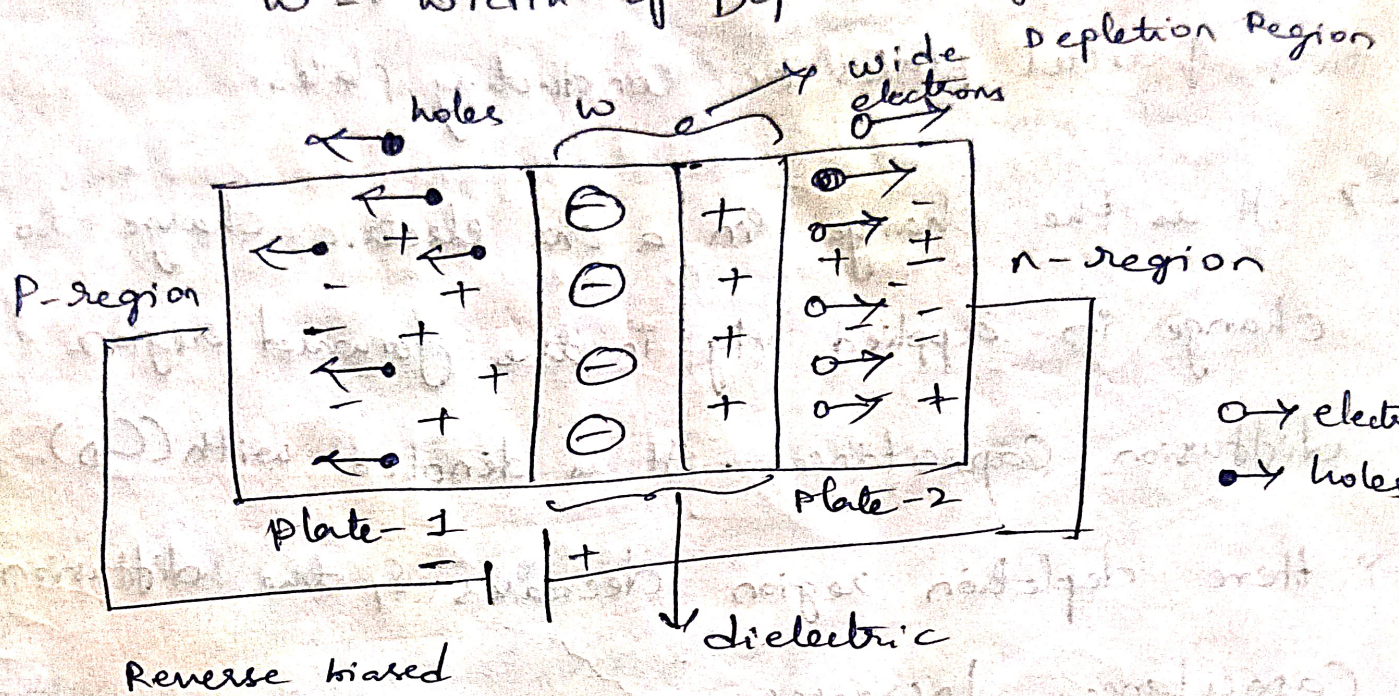
$$C_T = \frac{dq}{dv} = \frac{\epsilon A}{w}$$

$$C_T = \frac{dq}{dv} = \frac{\epsilon A}{w}$$

where, ϵ = Permittivity of free space

A = Area of plates

w = width of Depletion region



C_T = Transition Capacitances

$dq \rightarrow$ change in electric charge

$dv \rightarrow$ " " applied v/g

② Diffusion Capacitances (C_D)

→ In this diffusion capacitance (C_D), diode is in a forward biased condition, here also depletion region acts like dielectric and P & N regions acts like two parallel plates or conducting plates.

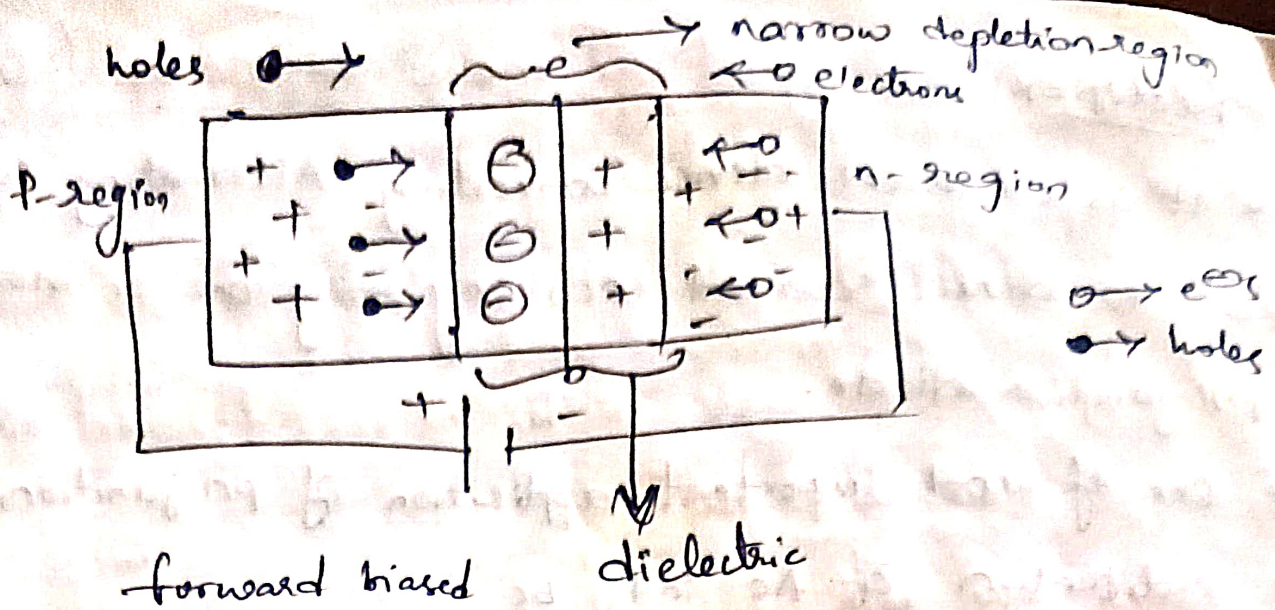
* → It is the change in a ch^a electric charge to the change in applied v/g in the forward region is called diffusion capacitance. It is denoted with (C_D)

→ Here depletion region decreases & the diffusion capacitance increases.

$$C_D = \frac{dq}{dv} = \frac{\text{Change in electric charge}}{\text{Change in Applied v/g}}$$

$$C_D = \frac{dq}{dv} = \frac{\gamma I}{\eta V_T}$$

[Note :- we have to explain about forward biased]



→ Diffusion Capacitance is much larger than the transition capacitance.

$$C_D = \frac{dQ}{dV} = \frac{\tau I}{\eta V_T}$$

C_D = diffusion capacitance

dQ → change in electric charge

dV → " " applied V/g

τ → life time of charge carriers

I → current through the diode

η → ideality constant

V_T → Thermal V/g

* Diode Models / Diode Equivalent Circuits :-

- It is a simplified representation of a diode's behavior in a circuit, used for analysis & calculations.
- It is of three types.

- ① Ideal diode
- ② Simplified or practical model diode
- ③ piecewise-linear model diode

* ① Ideal diode :-

- When we apply positive V_g to the diode it acts like a forward bias.
- When we apply negative V_g to the diode it acts like a Reverse bias.

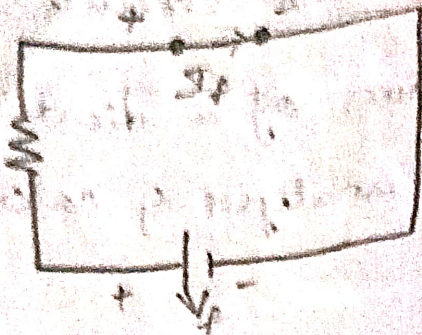
- The diode is in a forward bias condition it acts like a closed switch.

Symbol :-

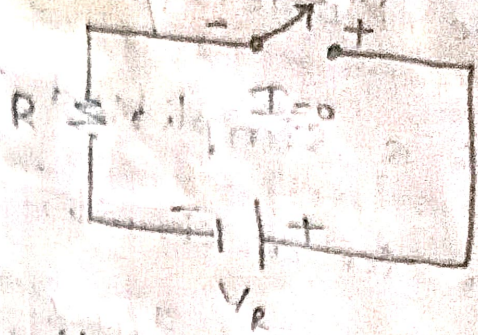


F.B

- The diode is in a Reverse bias condition it acts like a open switch.



(a) forward bias

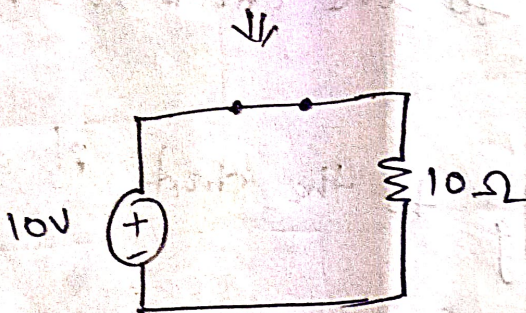
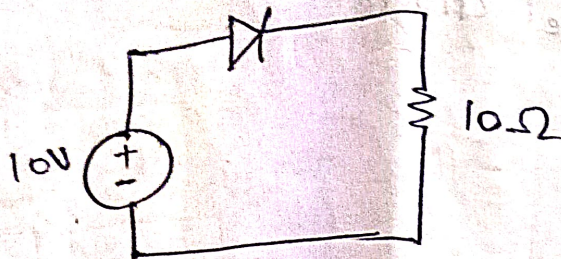


(b) reverse bias

Eg:

Q. find the current flowing through the given circuit

A. F.B



$$I = \frac{V}{R}$$

$$I = \frac{10}{10}$$

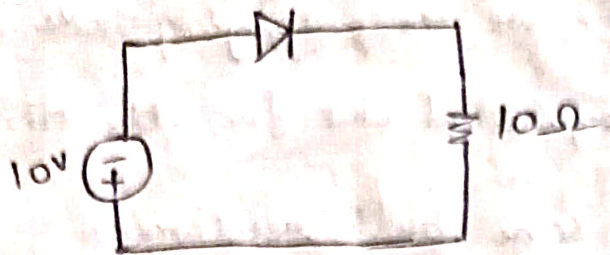
$$V = 10, R = 10\Omega$$

$$I = \frac{V}{R}$$

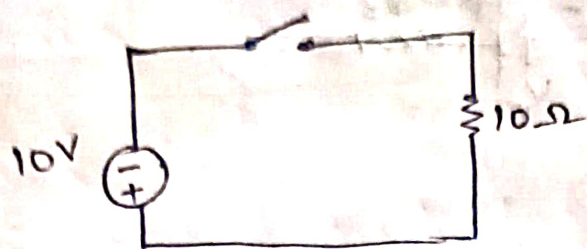
$$I = \frac{10}{10}$$

$$I = 1A$$

Q:-



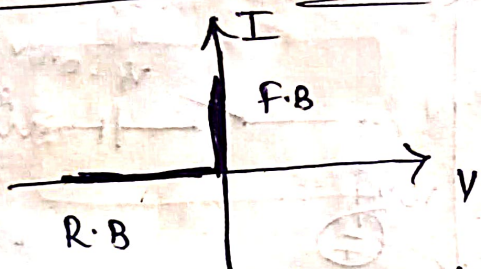
A:-



There is no flow of current in open ckt condition.

$$\therefore I = 0$$

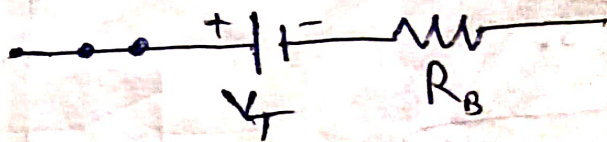
V-I characteristics of a diode:-



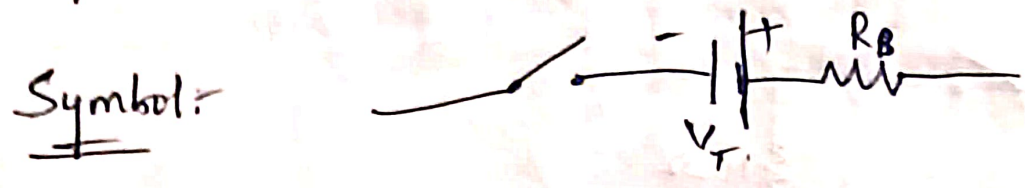
② Simplified or Piecewise-linear model of a diode:-

→ In a F.B condition we are applying +ve V/g to the diode then the equivalent circuit for the diode is closed switch with threshold voltage and the some bulk resistance

Symbol:-

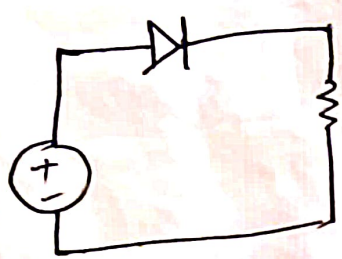


→ In a reverse bias condition we are applying -ve voltage to the diode then equivalent ckt for the diode is open switch with V_T and some bulk resistance.

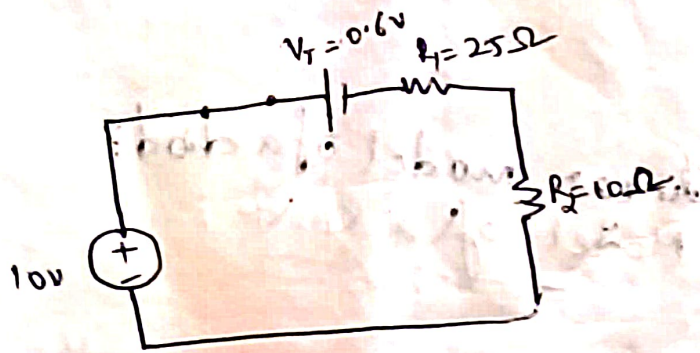


Example:-

Q. Forward Bias (F.B)



Ans.



$$I = \frac{V}{R}$$

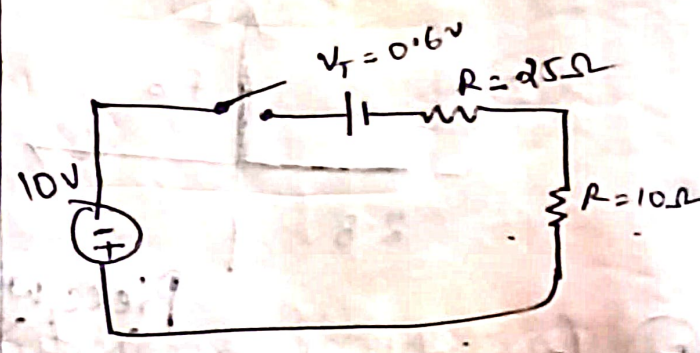
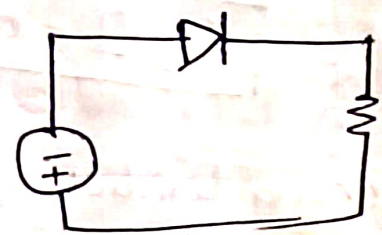
$$I = \frac{10 - 0.6}{25 + 10}$$

[∵ Resistance are in series]

$$I = \frac{9.4}{35}$$

$$I = 0.268A$$

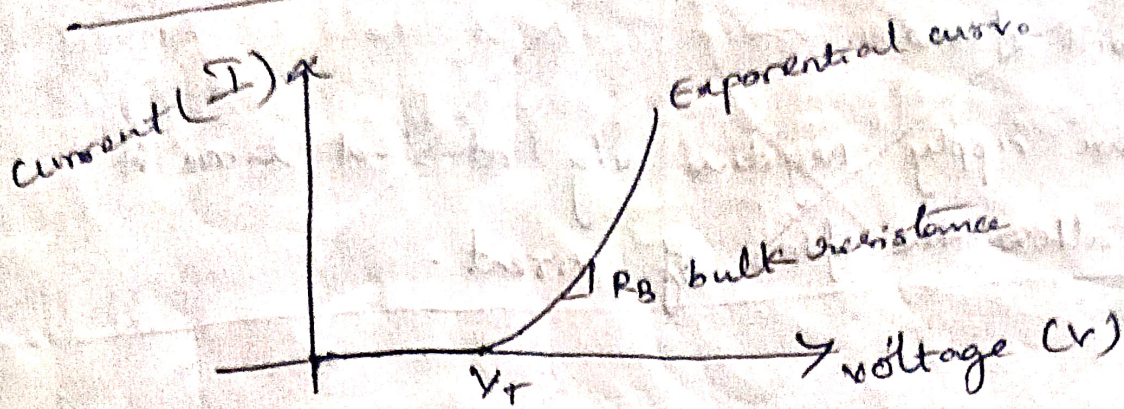
Reverse bias



$$I = 0$$

because the switch is open.

V-I characteristics of Simplified or practical diode



(3) Simplified or practical Piecewise-linear Model diode:

→ In a forward bias condition we are applying positive voltage to the diode then the equivalent ckt for the diode is closed switch along with some threshold voltage (V_T)

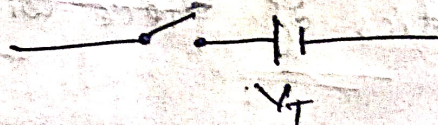
Symbol:



Threshold V_g (or) cut-in V_g for silicon is 0.6V & for Germanium is 0.3V.

→ In a Reverse bias condition we are applying negative V_g to the diode then the equivalent ckt for the diode is open switch along with some V_T

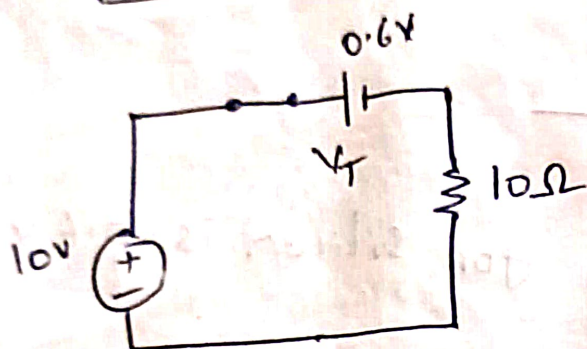
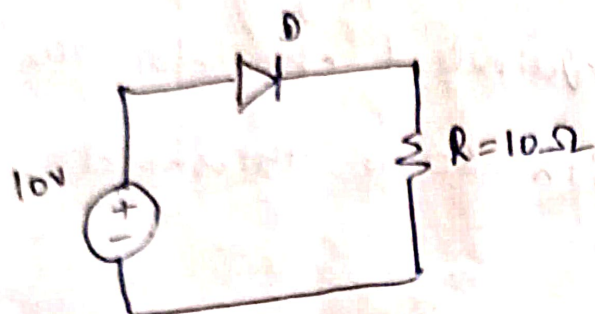
Symbol:



→ when
→ when we are

Example

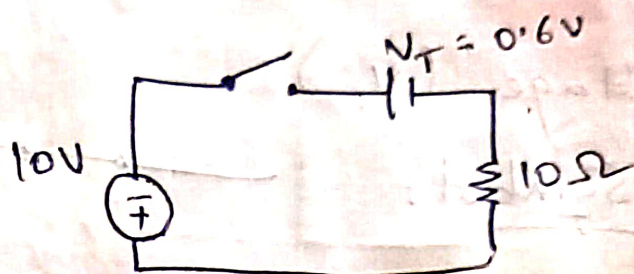
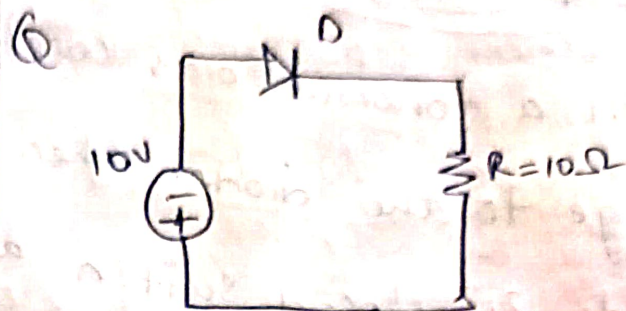
Q. forward bias



$$I = \frac{V}{R} = \frac{10 - 0.6}{10} = \frac{9.4}{10}$$

$$I = 0.94 \text{ A}$$

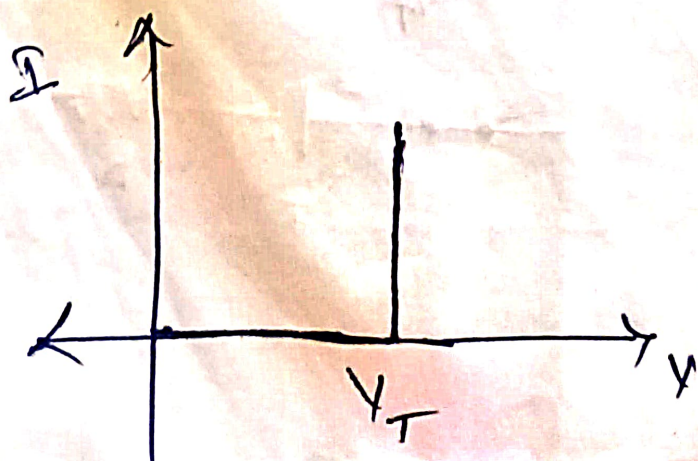
Reverse bias



$$I = 0$$

because the switch is open.

V-I characteristics of ~~Piece-wise~~ ^{simplified} linear model



* Rectifiers :

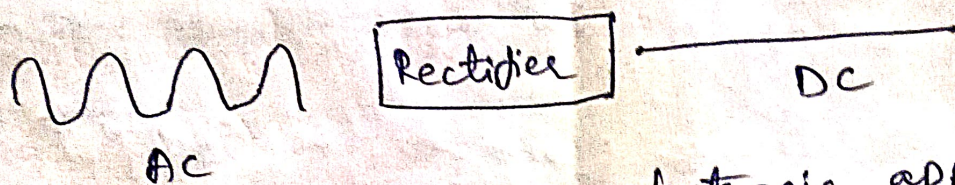
→ It is electrical device converting Alternating current (AC) to Direct current (DC) by using one or more

PN junction diode.

→ One of the most important application of PN junction diode is Rectification of AC to DC.

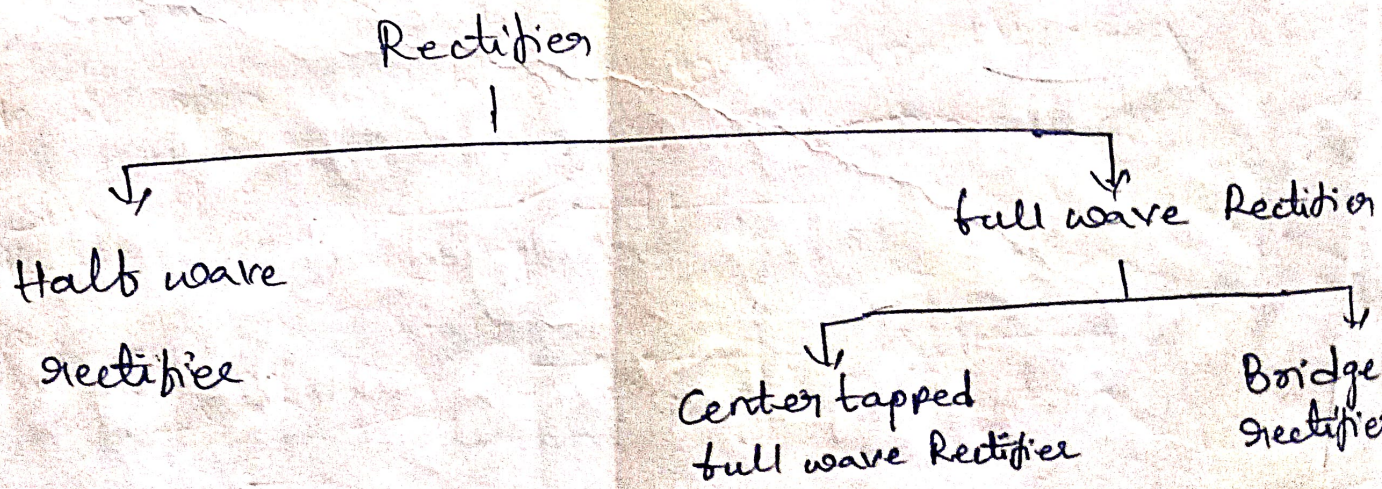
→ PN diode allow current in only forward bias condition blocks electric current in reverse bias condition.

(This property of diode allow it to act like rectifier.)



→ In our house almost all electronic appliances use AC current. Some electronic appliances such as laptops, computers convert AC into DC before they consume power.

→ Rectifier is of two types ① Half wave Rectifier
② Full wave Rectifier

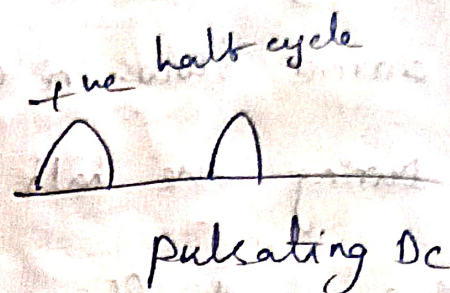
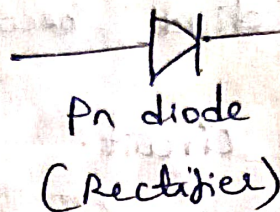
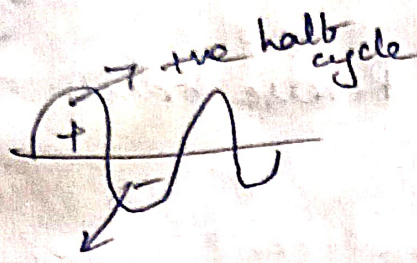


* Types of Rectifiers

① Half wave Rectifier:- (HWR)

→ It is type of rectifier which converts half of AC i/p signal (+ve half cycle) into pulsating DC o/p signal and remaining half cycle (-ve half cycle) is blocked

→ In HWR we use single diode

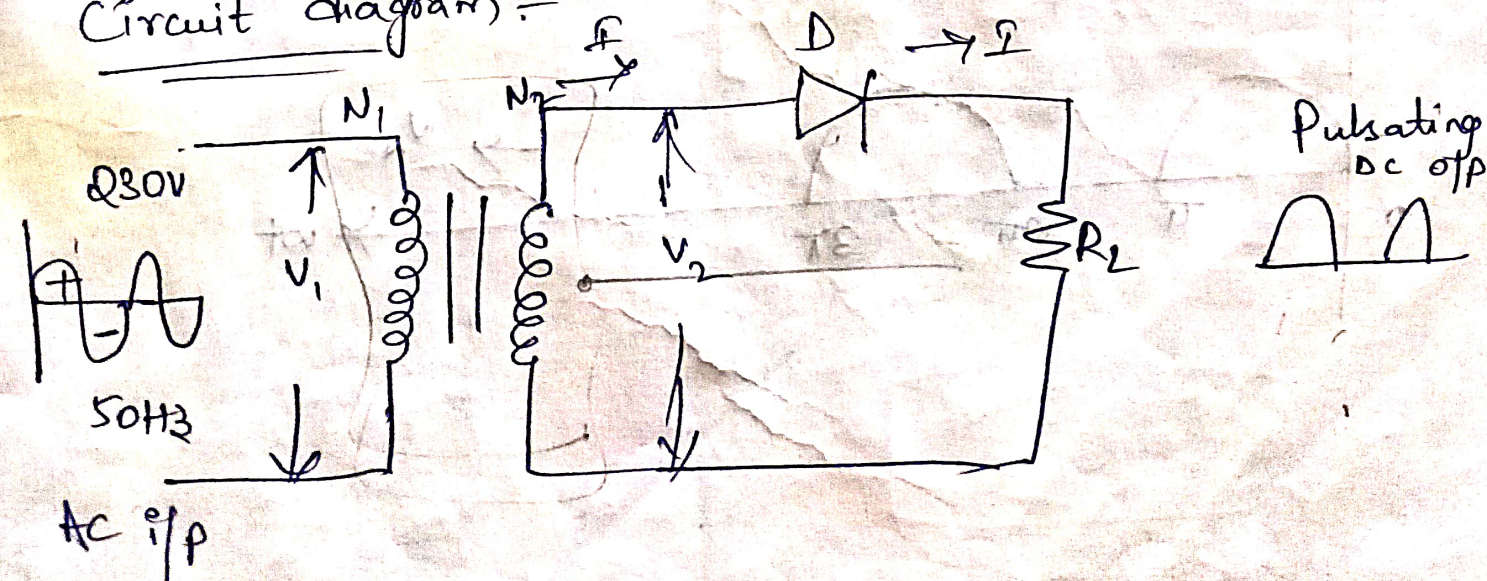


→ Here if positive half cycle allowed then negative half cycle blocked.

→ Similarly if negative half cycle allowed then positive half cycle blocked.

→ In HWR doesn't allow both +ve & -ve half cycle at same time [either in +ve or -ve only].

Circuit diagram:-



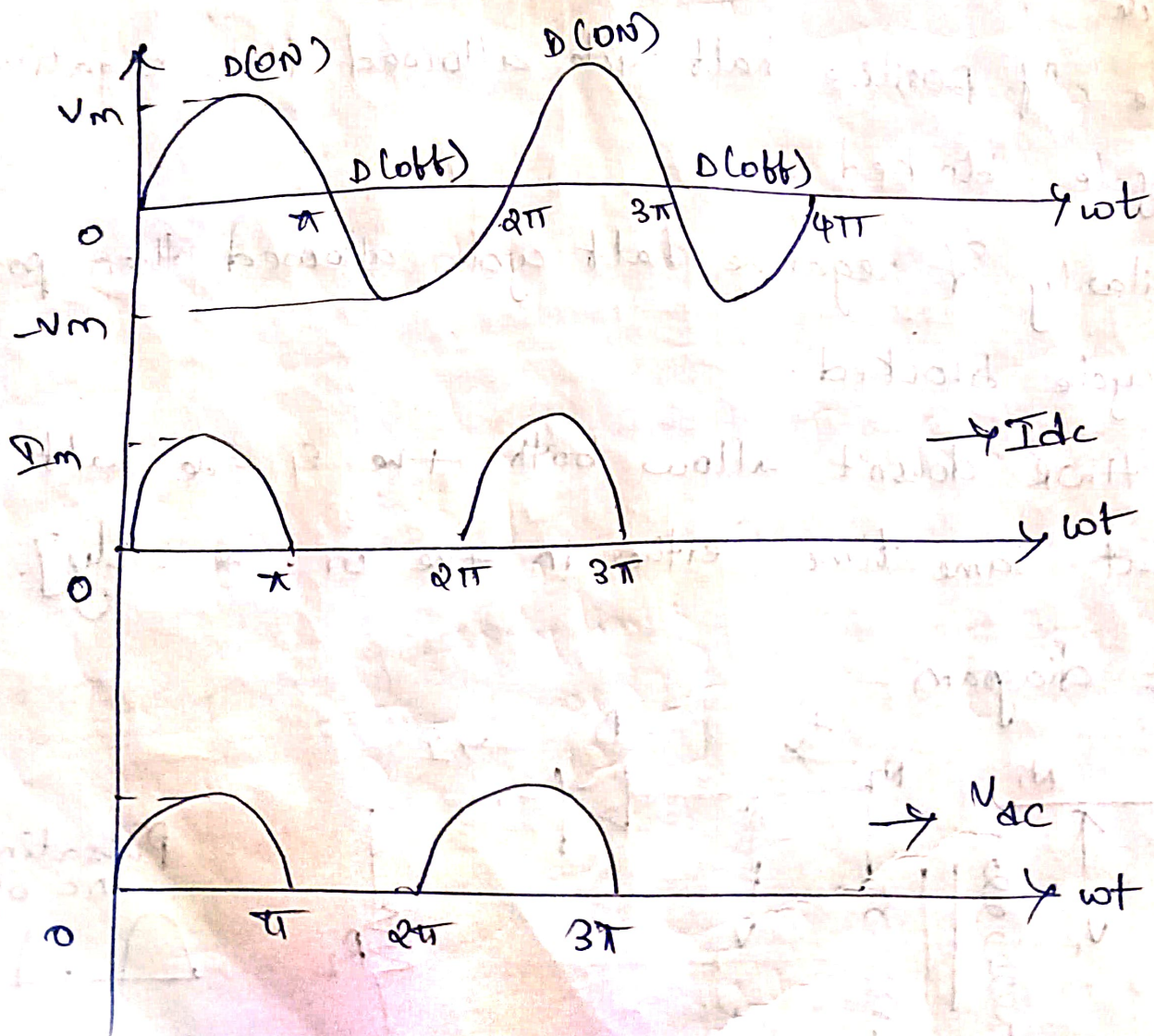
→ HWR is made up of AC source, transformer (step-down)

Diode & resistor (load)

→ Diode place b/w transformer & load.

→ During +ve half cycle diode becomes forward biased
& current flows in circuit.

→ During -ve half cycle diode becomes Reverse biased
& no current flows through circuit.



Characteristics:-

- ① Average DC current (I_{DC}) & DC voltage (V_{DC})
- ② I_{RMS}
- ③ V_{RMS}
- ④ efficiency
- ⑤ DC power output P_{DC}
- ⑥ AC Power i/p P_{AC}
- ⑦ Ripple factor
- ⑧ Transformer utilisation factor (TUF)
- ⑨ Peak Inverse V/g (PIV)
- ⑩ voltage Regulation

① Average DC current (I_{DC}):-

$$i_L = I_m \sin \omega t$$

$$\begin{aligned} 0 < \omega t < \pi & \rightarrow \text{+ve half cycle} \\ \pi < \omega t < 2\pi & \rightarrow \text{-ve half cycle} \end{aligned}$$

[here $\pi < \omega t < 2\pi$ is zero '0' due to -ve half cycle current doesn't flow.]

$I_m \Rightarrow$ peak value of load current.

$$I_{DC} = \frac{1}{T} \int_0^T i_L d\omega t$$

$$T = 2\pi, \quad i_L = I_m \sin \omega t$$

$$I_{DC} = \frac{1}{T} \int_0^T I_L dt$$

$$\Rightarrow \frac{1}{2\pi} \int_0^{2\pi} I_m \sin \omega t \cdot d\omega t$$

$$\Rightarrow \text{from } 0 \text{ to } 2\pi \text{ is } \underbrace{0 < \omega t < \pi}_{(1)} \text{ \& } \underbrace{\pi < \omega t < 2\pi}_{(2)}$$

$$\Rightarrow \frac{1}{2\pi} \int_0^{\pi} I_m \sin \omega t \cdot d\omega t + \int_{\pi}^{2\pi} I_m \sin \omega t \cdot d\omega t$$

'0' due to one half cycle

$$\Rightarrow \frac{I_m}{2\pi} \int_0^{\pi} \sin \omega t \cdot d\omega t + 0$$

$$\Rightarrow \frac{I_m}{2\pi} \left[-\cos \omega t \right]_0^{\pi} \quad [\because \int \sin \omega t = -\cos \omega t]$$

$$\Rightarrow \frac{I_m}{2\pi} \left[\begin{matrix} \text{Apply limits} \\ -\cos \pi - (-\cos 0) \\ (-1) \quad (1) \end{matrix} \right] \quad \left[\begin{matrix} \cos \pi = -1 \\ \cos 0 = 1 \end{matrix} \right]$$

$$\Rightarrow \frac{I_m}{2\pi} [-(-1) - (-1)] \Rightarrow \frac{I_m}{2\pi} \cdot 2$$

$$\boxed{I_{DC} = \frac{I_m}{\pi}}$$

$$\text{Similarly } V_{DC} = \frac{V_m}{\pi}$$

② Avg Dc load V_g

$$V_{DC} = I_{DC} \cdot R_L$$

$$V_{DC} = \frac{I_m}{\pi} \cdot R_L$$

$$\Rightarrow \frac{V_m}{\pi (R_f + R_L)} R_L$$

R_f is small compared to R_L .

$$V_{DC} = \frac{V_m}{\pi} \cdot \frac{R_L}{R_L}$$

$$\boxed{V_{DC} = \frac{V_m}{\pi}}$$

(or)

$$V_{DC} = \frac{1}{T} \int_0^T V_L \cdot dt$$

$$V_L = V_m \sin \omega t, T = 2\pi$$

$$V_{DC} = \frac{1}{2\pi} \int_0^{2\pi} V_m \sin \omega t \cdot dt$$

$[\pi < \omega t < 2\pi \text{ is '0'}]$

$$V_{DC} = \frac{1}{2\pi} \int_0^{\pi} V_m \sin \omega t \cdot dt$$

Apply limits

$$V_{DC} = \frac{V_m}{2\pi} \left[-\cos \omega t \right]_0^{\pi} \Rightarrow \frac{V_m}{2\pi} \left[-\cos(\pi) - (-\cos 0) \right]$$

$$V_{DC} = \frac{V_m}{2\pi} (2)$$

$$\boxed{V_{DC} = \frac{V_m}{\pi}}$$

② Avg Dc load V_{dc}

$$V_{dc} = I_{dc} \cdot R_L$$

$$V_{dc} = \frac{I_m}{\pi} \cdot R_L$$

$$\Rightarrow \frac{V_m}{\pi (R_f + R_L)} R_L$$

R_f is small compared to R_L

$$V_{dc} = \frac{V_m}{\pi} \cdot \frac{R_L}{R_L}$$

$$\boxed{V_{dc} = \frac{V_m}{\pi}}$$

(or)

$$V_{dc} = \frac{1}{T} \int_0^T V_o \cdot dt$$

$$V_o = V_m \sin \omega t$$

$$V_o = V_m \sin \omega t, T = 2\pi$$

$$V_{dc} = \frac{1}{2\pi} \int_0^{2\pi} V_m \sin \omega t \cdot dt$$

$[\pi < \omega t < 2\pi \text{ is '0'}]$

$$V_{dc} = \frac{1}{2\pi} \int_0^{\pi} V_m \sin \omega t \cdot dt$$

Apply limits

$$V_{dc} = \frac{V_m}{2\pi} \left[-\cos \omega t \right]_0^{\pi} \Rightarrow \frac{V_m}{2\pi} \left[-\cos(\pi) - (-\cos 0) \right]$$

$$V_{dc} = \frac{V_m}{2\pi} (2)$$

$$\boxed{V_{dc} = \frac{V_m}{\pi}}$$

③ I_{RMS} : RMS value of load current

$$I_{RMS} = \sqrt{\frac{1}{T} \int_0^T i_L^2 dt}$$

$$T = 2\pi, i_L = I_m \sin \omega t$$

$$I_{RMS} = \sqrt{\frac{1}{2\pi} \int_0^{2\pi} (I_m \sin \omega t)^2 dt}$$

$$\Rightarrow \sqrt{\frac{1}{2\pi} \int_0^{2\pi} I_m^2 \sin^2 \omega t dt}$$

$$0 < \omega t < \pi \quad \& \quad \underbrace{\pi < \omega t < 2\pi}_0$$

$$\sqrt{\frac{1}{2\pi} \int_0^{\pi} I_m^2 \sin^2 \omega t dt}$$

$$\because \sin^2 \theta = \frac{1 - \cos 2\theta}{2}$$

$$\sqrt{\frac{I_m^2}{2\pi} \int_0^{\pi} \left(\frac{1 - \cos 2\omega t}{2} \right) dt}$$

$$\sqrt{\frac{I_m^2}{2\pi} \left[\frac{\omega t}{2} - \frac{\sin 2\omega t}{2 \cdot 2} \right]_0^{\pi}}$$

$$\left\{ \begin{array}{l} \because \int 1 \cdot \omega t = \omega t \\ \int \cos 2\omega t = \frac{\sin 2\omega t}{2} \end{array} \right.$$

Apply limits

$$\Rightarrow \sqrt{\frac{I_m^2}{2\pi} \left[\frac{\pi}{2} - 0 \right] - \left[\frac{\sin 2(\pi) - \sin 2(0)}{4} \right]}$$

$$\Rightarrow \sqrt{\frac{I_m^2}{2\pi} \left[\frac{\pi}{2} \right] - 0} \quad \left[\because \sin \pi - 0 \right]$$

$$\left[\because \sin 0 - 0 \right]$$

$$\Rightarrow \sqrt{\frac{I_m^2}{2\pi} \left[\frac{\pi}{2} \right]}$$

$$\Rightarrow \sqrt{\frac{I_m^2}{4}}$$

$$I_{RMS} = \sqrt{\frac{I_m^2}{4}}$$

$$I_{RMS} = \frac{I_m}{2}$$

Similarly $V_{RMS} = \frac{V_m}{2}$

$$V_{RMS} = \frac{V_m}{2}$$

[No V_{RMS} derivation it is same as like I_{RMS}]

④ DC power output P_{DC} :

$$P_{DC} = V_{DC} \cdot I_{DC}$$

$$(I_{DC} \cdot R_L) \cdot I_{DC}$$

$$\Rightarrow I_{DC}^2 \cdot R_L$$

$$\left[\because I_{DC} = \frac{I_m}{\pi} \right]$$

$$P_{DC} \Rightarrow \frac{I_m^2}{\pi^2} \cdot R_L$$

⑤ AC power input P_{AC} :-

$$P_{AC} = V_{RMS} I_{RMS}$$

$$\Rightarrow (I_{RMS} \cdot R_L) I_{RMS}$$

$$\Rightarrow I_{RMS}^2 \cdot R_L$$

$$P_{AC} \Rightarrow \frac{I_m^2}{4} \cdot R_L$$

$$\left[\because V_{RMS} = I_{RMS} \times R_L \right]$$

$$\left[\because I_{RMS} = \frac{I_m}{2} \right]$$

* Efficiency (or) Rectifier efficiency $:(\eta)$:-

$\rightarrow$ It is ratio of o/p DC power to i/p AC power

$$\eta = \frac{\text{DC o/p power}}{\text{AC i/p power}} = \frac{P_{DC}}{P_{AC}}$$

$$\eta = \frac{\frac{I_m^2}{\pi^2} \cdot R_L}{\frac{I_m^2}{4} \cdot R_L} \Rightarrow \frac{4}{\pi^2}$$

$$\eta = 0.406$$

$$\therefore \eta = 0.406 \times 100 = 40.6\%$$

$$\therefore \eta = 40.6\%$$

* Ripple factor (γ):

$$\gamma = \frac{\text{Rms value of AC component of o/p}}{\text{Avg or DC component of o/p}}$$

$$\gamma = \frac{I_{ac}}{I_{dc}} \quad \therefore I_{ac} = \sqrt{I_{rms}^2 - I_{dc}^2}$$

$$\gamma = \frac{\sqrt{I_{rms}^2 - I_{dc}^2}}{I_{dc}}$$

$$\gamma = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$$

$$\left[\because I_{rms} = \frac{I_m}{\sqrt{2}} \right]$$

$$\left[\because I_{dc} = \frac{I_m}{\pi} \right]$$

$$\gamma = \sqrt{\left(\frac{\frac{I_m}{\sqrt{2}}}{\frac{I_m}{\pi}}\right)^2 - 1} \Rightarrow \sqrt{\frac{\pi^2}{4} - 1}$$

$$\boxed{\gamma = 1.211}$$

* Transformer utilization factor (TUF) of HWR :

$$TUF = \frac{\text{dc power delivered to load}}{\text{Ac power rating of transformer secondary}}$$

$$TUF = \frac{P_{dc}}{P_{ac, \text{ rated}}} = \frac{P_{dc}}{P_{rms}}$$

$$TUF = \frac{P_{dc}}{P_{rms}}$$

$$\therefore P = V \cdot I$$

$$\therefore P_{dc} = V_{dc} \cdot I_{dc}$$

$$\therefore P_{rms} = V_{rms} \cdot I_{rms}$$

$$\therefore V = IR \Rightarrow I = \frac{V}{R}$$

$$\therefore I_{dc} = \frac{V_{dc}}{R_L}$$

$$TUF = \frac{V_{dc} I_{dc}}{V_{rms} \cdot I_{rms}}$$

$$\Rightarrow \frac{V_{dc} \cdot \frac{V_{dc}}{R_L}}{V_{rms} \cdot \frac{V_{rms}}{R_L}} \Rightarrow \frac{\frac{V_{dc}^2}{R_L}}{\frac{V_{rms}^2}{R_L}} \Rightarrow \left(\frac{V_{dc}}{V_{rms}} \right)^2$$

$$TUF = \frac{\frac{V_m}{\pi^2}}{\frac{V_m}{2^2}} \Rightarrow \frac{4}{\pi^2} = 0.406.$$

$$\therefore V_{dc} = \frac{V_m}{\pi}$$

$$\therefore V_{rms} = \frac{V_m}{2}$$

$$TUF = 0.406 \rightarrow \text{Same as efficiency}$$

But do it half $\div$ by '2'

$$TUF = \frac{0.406}{2} = 0.203$$

$$TUF = 0.203$$

approximate & actual value of TUF is 28.6 %

* form factor:-

$$\text{form factor} = \frac{\text{rms value}}{\text{Avg value}} \Rightarrow \frac{\frac{V_m}{2}}{\frac{V_m}{\pi}} = \frac{\pi}{2} = 1.57$$

$$\boxed{\text{form factor} = 1.57}$$

* Peak factor:

$$\text{Peak factor} = \frac{\text{Peak value}}{\text{rms value}}$$

$$\frac{V_m}{\frac{V_m}{2}}$$

$$\text{Peak factor} = 2$$

* Advantage

* Peak inverse voltage: it is the peak v/g across diode in reverse bias hence maximum value of v/g that exist across diode i.e., V_m

$$\boxed{PIV = V_m}$$

* voltage Regulation:-

The v/g regulation is the factor which tells about the change in dc o/p v/g as load changes from no load to full load condition

$$(V_{dc})_{NL} = \text{DC v/g on no load}$$

$$(V_{dc})_{FL} = \text{D.C v/g on full load}$$

Then the v/g Regulation is

$$V.R = \frac{(V_{dc})_{NL} - (V_{dc})_{FL}}{(V_{dc})_{FL}}$$

* Advantages of HWR:-

- Simple & easy to design
- low cost circuit

* Disadvantages of HWR:-

- low efficiency i.e., 40.6%.
- High ripple factor (1.21)
- low TUF (0.287), TUF is not fully utilized

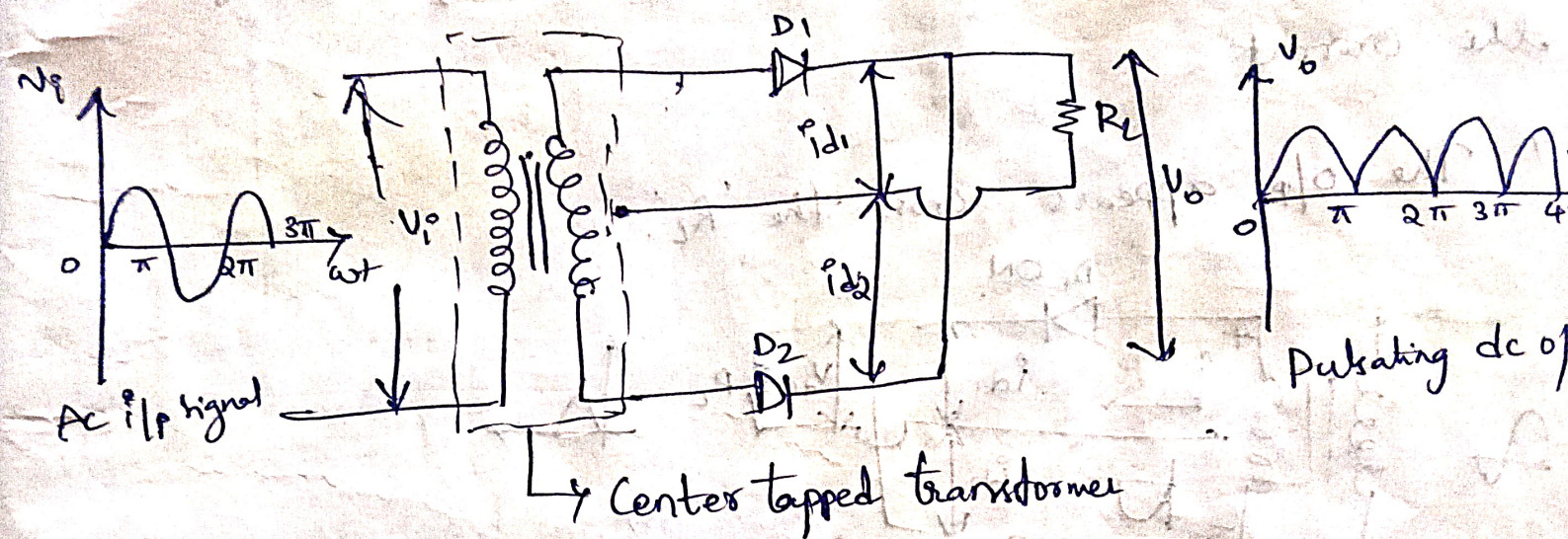
* Full-wave Rectifier:

→ Full-wave Center tapped Rectifier

→ FWR is a circuit which converts bi-directional AC i/p signal into a pulsating dc v/g using two pn junction diodes.

→ It conducts during both the positive & negative half cycles of ac i/p signal.

→ It is also called center tapped transformer.



* Operation:

→ The center-tap transformer is used to provide the equal v/g's above and below the center-tapped for both the half-cycles.

* During +ve half cycle

→ During +ve half cycle of the i/p signal, the diode D_1 is forward biased and D_2 is Reverse biased.

→ Hence D_1 conducts & D_2 does not conduct

* During -ve half cycle:

→ During -ve half cycle of the i/p signal, the diode D_1 is reverse biased & D_2 is forward biased.

→ Hence D_1 does not conduct and D_2 conducts the current

→ The o/p. appears across the ' R_L '.

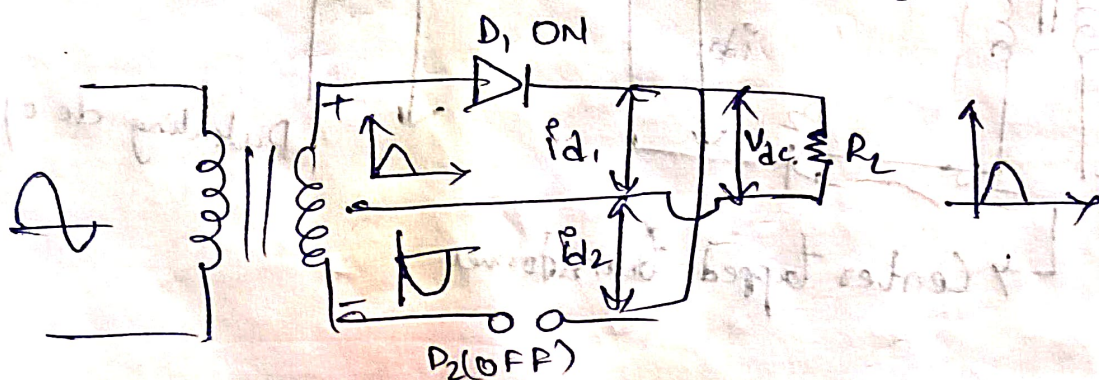


Fig: +ve half cycle

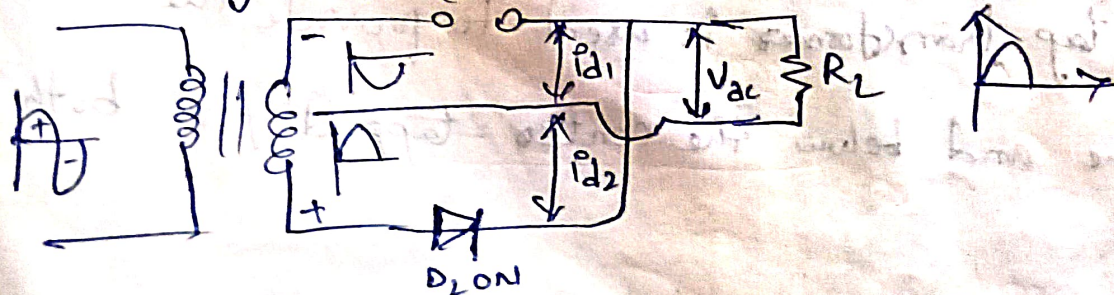
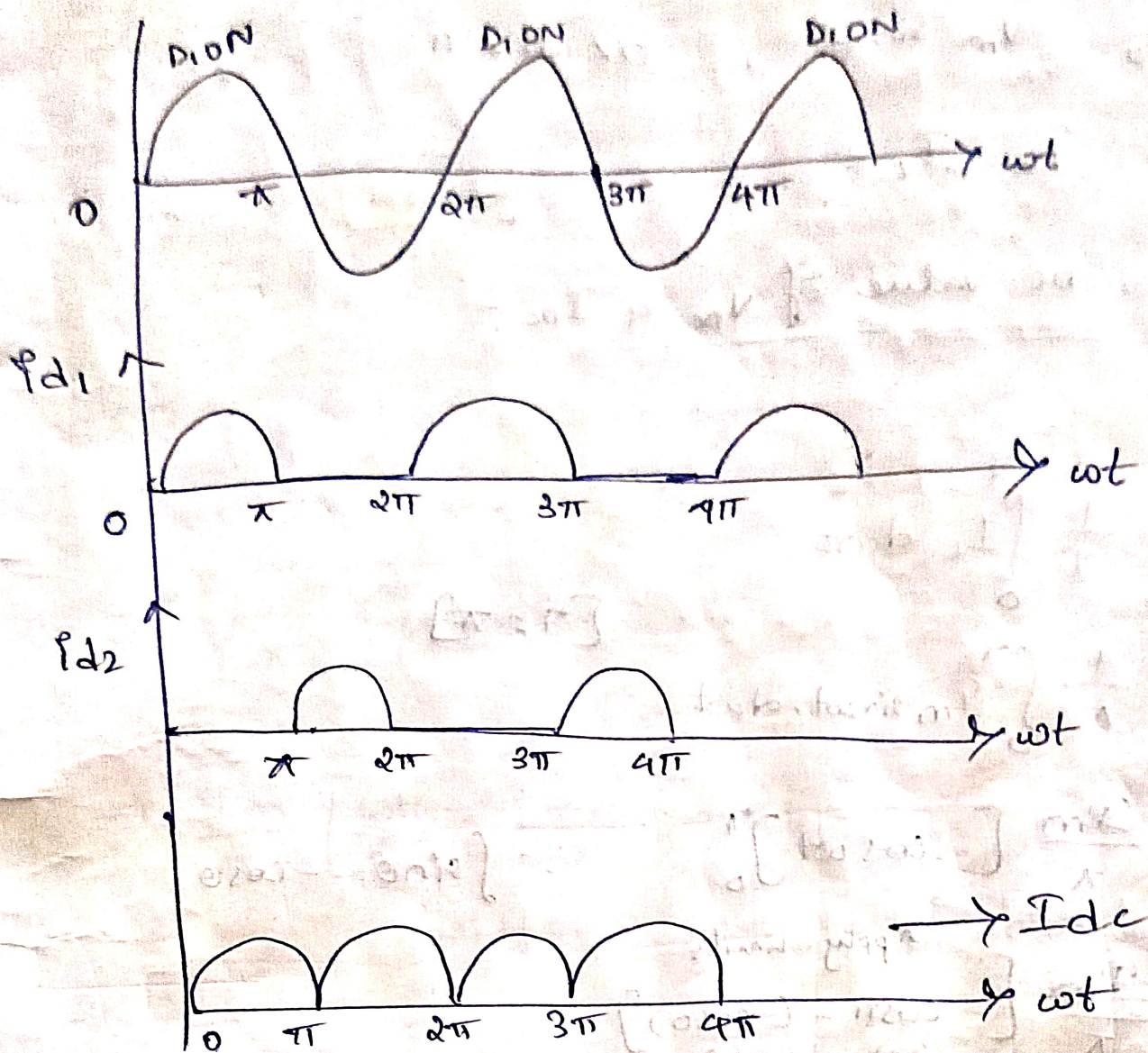


Fig: -ve half cycle

Waveforms:



Characteristics:

- ① Average dc load current : (I_{dc}) & V_{dc}
- ② I_{rms} & V_{rms}
- ③ P_{dc} (DC power o/p)
- ④ AC power i/p (P_{ac})
- ⑤ Rectifier efficiency (η)
- ⑥ Ripple factor (γ)
- ⑦ PIV
- ⑧ TUF
- ⑨ V/g Regulation

$$I_o = I_m \sin \omega t, \quad 0 < \omega t < \pi$$

$$V_o = V_m \sin \omega t, \quad 0 < \omega t < \pi$$

$$I_o = I_L$$

① Avg or DC value of V_{DC} & I_{DC} :-

$$\underline{I_{DC}}$$

$$I_{DC} = \frac{1}{T} \int_0^T I_L \cdot d\omega t$$

$$[T = \pi]$$

$$I_{DC} = \frac{1}{\pi} \int_0^{\pi} I_m \sin \omega t \cdot d\omega t$$

$$\Rightarrow \frac{I_m}{\pi} [-\cos \omega t]_0^{\pi} \quad \because \int \sin \theta = -\cos \theta$$

$$\Rightarrow \frac{I_m}{\pi} \left[\begin{array}{c} \text{Apply limits} \\ -\cos \pi - (-\cos 0) \end{array} \right]$$

$$\Rightarrow \frac{I_m}{\pi} (2)$$

$$\boxed{I_{DC} = \frac{2I_m}{\pi}}$$

Similarly

$$\boxed{V_{DC} = \frac{2V_m}{\pi}}$$

②

$\left[I_{DC} = \frac{I_m}{\pi} \text{ in HWR} \right] \rightarrow$ Here for FWR twice the rectification (HWR)

* Rms values of V & I :-

$$\underline{I_{RMS}} \quad \& \quad \underline{V_{RMS}}$$

$$\underline{I_{RMS}}$$

$$I_{RMS} = \sqrt{\frac{1}{T} \int_0^T I^2 dt}$$

$$I = I_m \sin \omega t$$

$$[T = \pi]$$

$$I_{RMS} = \sqrt{\frac{1}{\pi} \int_0^{\pi} I_m^2 \sin^2 \omega t \cdot d\omega t}$$

$$\Rightarrow \sqrt{\frac{I_m^2}{\pi} \int_0^{\pi} \left(\frac{1 - \cos 2\omega t}{2} \right) d\omega t}$$

$$[\because \sin^2 \theta = \frac{1 - \cos 2\theta}{2}]$$

$$\int 1 \cdot d\omega t = \omega t$$

$$\int \cos 2\theta \Rightarrow \frac{\sin 2\theta}{2}$$

$$\Rightarrow \sqrt{\frac{I_m^2}{\pi} \left[\frac{\omega t}{2} - \frac{\sin 2\omega t}{2 \cdot 2} \right]_0^{\pi}}$$

Apply limits

$$\Rightarrow \sqrt{\frac{I_m^2}{\pi} \left[\frac{\pi}{2} - 0 - \frac{\sin 2(\pi) - \sin 2(0)}{4} \right]}$$

$$(\because \sin \pi = 0)$$

$$(\because \sin 0 = 0)$$

$$\Rightarrow I_{RMS} = \sqrt{\frac{I_m^2}{\pi} \left[\frac{\pi}{2} \right]}$$

$$I_{RMS} = \frac{I_m}{\sqrt{2}}$$

Similarly

$$V_{RMS} = \frac{V_m}{\sqrt{2}}$$

[Note: Do V_{RMS} derivation same as like I_{RMS}
Keep V in the place of I]

* Dc power o/p P_{DC} :

$$P_{DC} = V_{DC} \cdot I_{DC}$$

$$\downarrow$$

$$(I_{DC} \cdot R_L) \cdot I_{DC}$$

$$P_{DC} = I_{DC}^2 \cdot R_L$$

$$P_{DC} = \left(\frac{\sqrt{2} I_m}{\sqrt{2}} \right)^2 \cdot R_L$$

$$P_{DC} = \frac{4 I_m^2}{\pi^2} R_L$$

$$P_{DC} = \frac{4 I_m^2 R_L}{\pi^2}$$

Ac power i/p P_{AC} :

$$P_{AC} = \frac{V_{rms} I_{rms}}{1}$$

$$P_{AC} = I_{rms}^2 \cdot R_L$$

$$\left(\frac{I_m}{\sqrt{2}} \right)^2 \cdot R_L$$

$$P_{AC} = \frac{I_m^2 R_L}{2}$$

$$P_{AC} = \frac{I_m^2 R_L}{2}$$

$$P = VI = \frac{V^2}{R}$$

$$V = IR$$

$$P = VI$$

$$V = IR$$

* Rectifier efficiency η :-

$$\eta = \frac{P_{ac}}{P_{dc}}$$

$$\eta = \frac{\frac{45\% \cdot P_L}{\pi^2}}{\frac{I_m \cdot R_L}{2}} = \frac{8}{\pi^2}$$

$$\eta = 0.812$$

$$\therefore \eta = 81.2\%$$

The maximum efficiency of FWR is 81.2%.

* Ripple factor γ :-

→ It is an unwanted AC component present in the dc o/p.

$$\gamma = \frac{\text{rms value of AC component}}{\text{dc component}} = \frac{I_{AC}}{I_{DC}}$$

$$\gamma = \sqrt{\left(\frac{I_{rms}}{I_{DC}}\right)^2 - 1} \quad \left\{ \begin{array}{l} \gamma = \frac{\sqrt{I_{rms}^2 - I_{DC}^2}}{I_{DC}} \\ I_{rms} = \frac{I_m}{\sqrt{2}} \quad \& \quad I_{DC} = \frac{2I_m}{\pi} \end{array} \right.$$

$$\gamma = \sqrt{\frac{\frac{I_m}{\sqrt{2}}}{2\left(\frac{I_m}{\pi}\right)^2} - 1} \Rightarrow \sqrt{\frac{\pi^2}{8} - 1} \Rightarrow \gamma = 0.48$$

$$\boxed{\gamma = 0.48}$$

* Peak Inverse vlg (PIV)

$$PIV = 2V_m$$

* Transformer utilization factor (TUF) of FWR

$$TUF = \frac{P_{dc}}{P_{ac, \text{rated}}} = \frac{P_{dc}}{P_{rms}}$$

$$\therefore P = V \cdot I$$

$$\therefore P_{dc} = V_{dc} \cdot I_{dc}$$

$$P_{rms} = V_{rms} \cdot I_{rms}$$

$$TUF = \frac{V_{dc} \cdot I_{dc}}{V_{rms} \cdot I_{rms}}$$

$$TUF = \frac{V_{dc} \cdot \frac{V_{dc}}{R_L}}{V_{rms} \cdot \frac{V_{rms}}{R_L}} \Rightarrow \frac{\frac{V_{dc}^2}{R_L}}{\frac{V_{rms}^2}{R_L}} \Rightarrow \frac{V_{dc}^2}{V_{rms}^2}$$

$$TUF = \frac{\frac{2V_m^2}{\pi^2}}{\frac{V_m^2}{2}} \Rightarrow TUF = \frac{8}{\pi^2} = 0.81$$

$TUF = 81.05\% \rightarrow$ for secondary

Primary :- 2 times of HWR

$$TUF = 2 \times 0.3 = 0.406$$

$$TUF = \frac{0.406 + 0.81}{2}$$

$$\boxed{TUF = 0.693}$$

* voltage Regulation:-

$$(V_{dc})_{NL} = \frac{2V_m}{\pi}$$

$$(V_{dc})_{FL} = I_{dc} R_L$$

$$\therefore R = \frac{(V_{dc})_{NL} - (V_{dc})_{FL}}{(V_{dc})_{FL}} \times 100$$

$$\therefore R = \frac{\frac{2V_m}{\pi} - I_{dc} R_L}{I_{dc} R_L} = \frac{\frac{2V_m}{\pi} - \frac{2V_m R_L}{\pi}}{\frac{2I_m R_L}{\pi}}$$

$$\Rightarrow \frac{\frac{2I_m}{\pi} (R_s + R_f + R_L) - \frac{2I_m}{\pi} R_L}{\frac{2I_m}{\pi} R_L}$$

$$\Rightarrow \frac{\cancel{\frac{2I_m}{\pi}} (R_s + R_f + \cancel{R_L} - \cancel{R_L})}{\cancel{\frac{2I_m}{\pi}} R_L}$$

$$\frac{\cancel{\frac{2I_m}{\pi}} R_L}{\cancel{\frac{2I_m}{\pi}} R_L}$$

$$\therefore R = \frac{R_s + R_L}{R_L} \times 100 \quad \text{or} \quad \therefore R = \frac{1}{R_L} \times 100$$

* Advantages of Full wave Rectifier:

→ Form factor:

$$\text{Form factor} = \frac{\text{rms value}}{\text{Avg value}}$$

$$\Rightarrow \frac{V_m / \sqrt{2}}{2V_m / \pi} \Rightarrow \frac{\pi}{2\sqrt{2}} = 1.11$$

→ Peak factor:

$$\text{Peak factor} = \frac{\text{Peak value}}{\text{rms value}}$$

$$P.f = \frac{V_m}{V_m / \sqrt{2}} \Rightarrow \sqrt{2}$$

* Advantages of PWR:

→ Efficiency is higher than $\frac{1}{2}$ WR

$$\eta = 81.2\%$$

→ lower Ripple factor ; $r = 48.2\%$

→ Higher TUF 0.693,

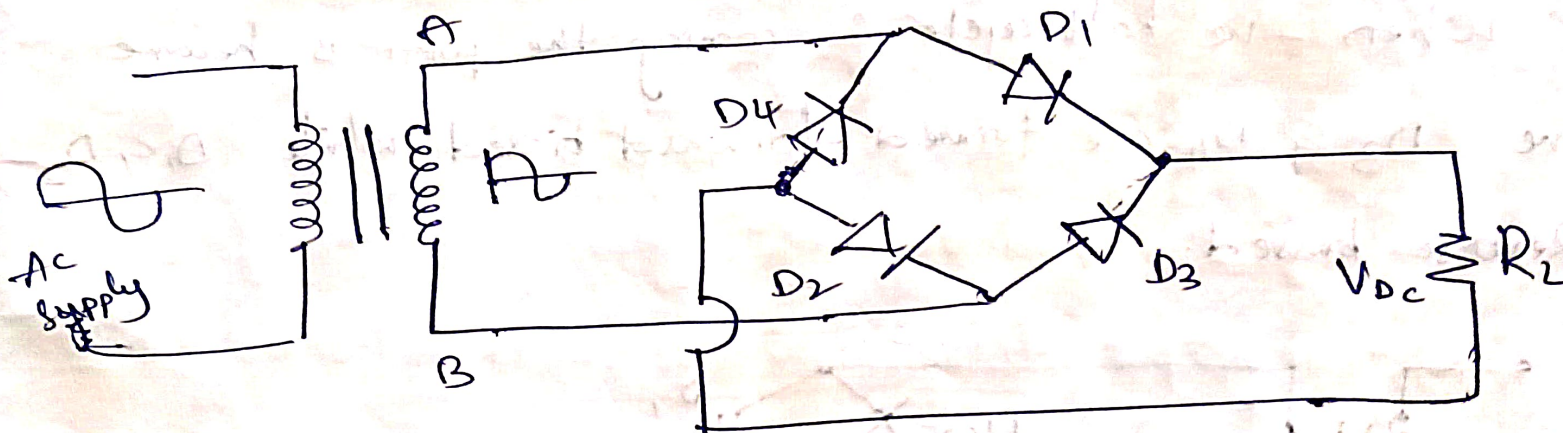
* Disadvantages:

→ Larger in size

→ costlier due to Center-tapped transformer

* Bridge Rectifier:

These circuits are mainly used as power rectifier circuit to convert AC power to DC power.

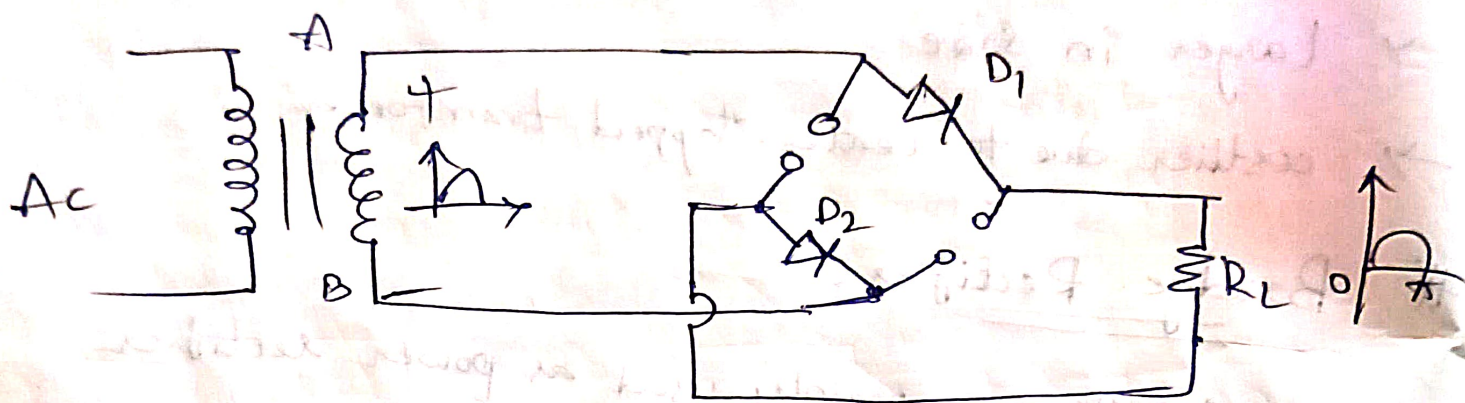


→ This is full wave rectifier ckt using four diodes forming the four arms of a bridge. AC signal applied to one diagonal of bridge & o/p taken from another diagonal.

The advantage of ckt it does not require centre tapped transformer.

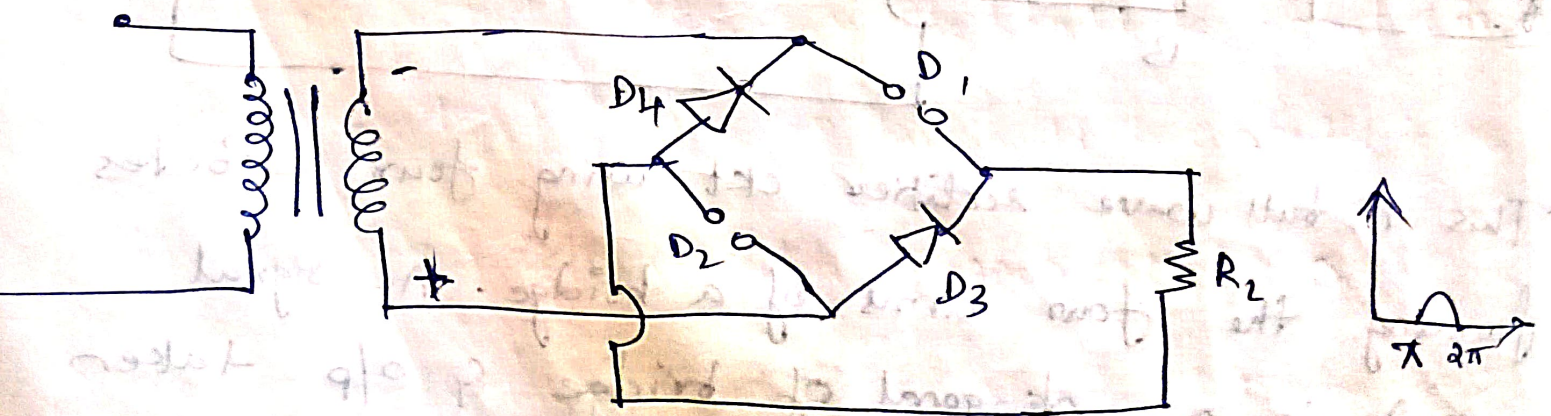
Operations:-

→ when positive half of AC i/p v/g consider point 'A' become +ve & diode D_1 & D_2 will be forward biased while D_3 & D_4 Reverse biased.



During +ve half cycle:

→ When -ve half cycle is coming the point B become +ve & D_3 & D_4 are forward biased while D_1 & D_2 Reverse biased.



* Parameters of Bridge Rectifier is same as that of full wave rectifier *

$$(1) I_{dc} = \frac{2I_m}{\pi}$$

$$(2) V_{dc} = \frac{2V_m}{\pi}$$

$$(3) I_{rms} = \frac{V_m}{\sqrt{2}}$$

$$(4) V_{rms} = \frac{V_m}{\sqrt{2}}$$

$$(5) P_{dc} = \frac{4I_m^2}{\pi^2} \cdot R_L$$

$$(6) P_{ac} = \frac{I_m^2}{2} R_L$$

* Efficiency $\eta = \frac{\frac{4I_m^2 R_L}{\pi^2}}{\frac{I_m^2 R_L}{2}} = \frac{8}{\pi^2}$

$$\eta = 0.812$$

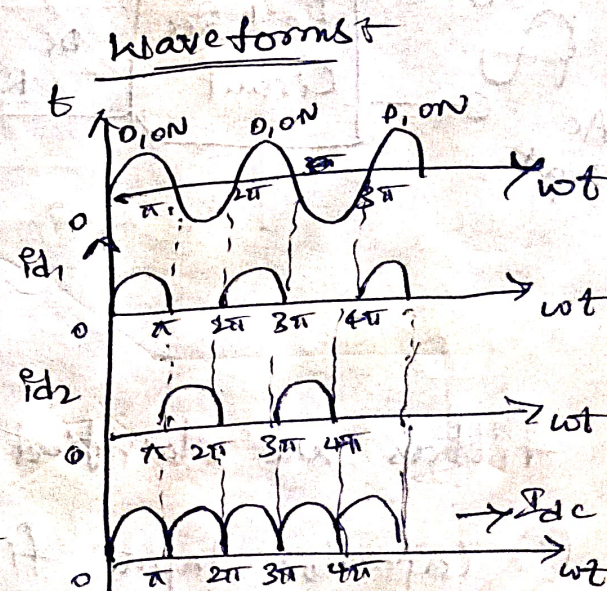
$$\therefore \eta = 81.2\%$$

* Ripple factor $r = 0.4811$

Advantages of Bridge rectifier:

(1) No centre tap transformer

(2) Current in secondary of transformer is in opposite direction in two half cycles. Hence net DC component flowing is zero which reduces the losses & danger of saturation.



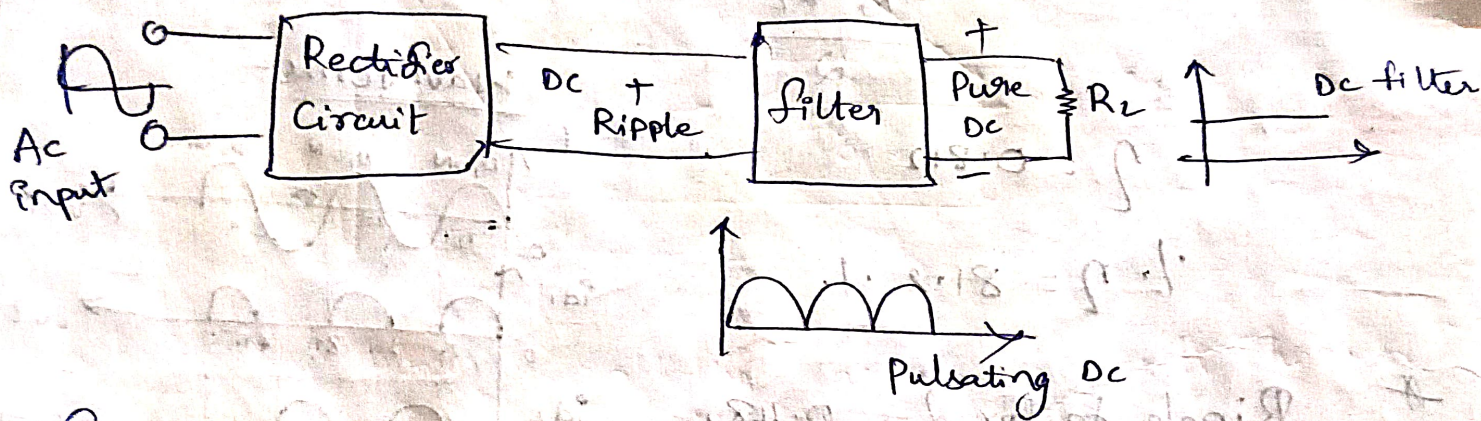
* Disadvantages

→ It uses four diodes.

* Capacitor filter for rectifiers, [HWR & FWR]

filter: The output of full wave rectifier is not pure D.C. it contains some portion of A.C. called ripples.

To minimise the ripple content in the output filter circuit are used. These circuits are used between rectifier & load.



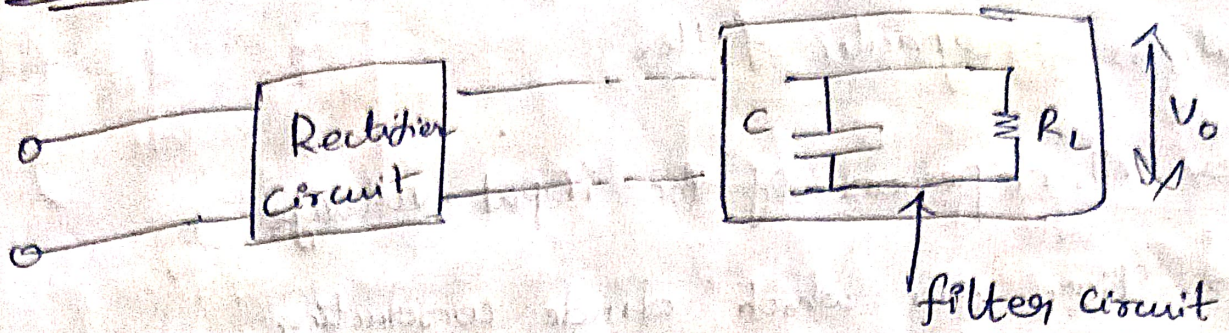
Filters are classified into two types:

- ① Capacitor Input filter → This should be connected in Parallel
- ② Inductor Input filter → This should be connected in Series

Capacitor is parallelly connected & open ckt. for D.C.

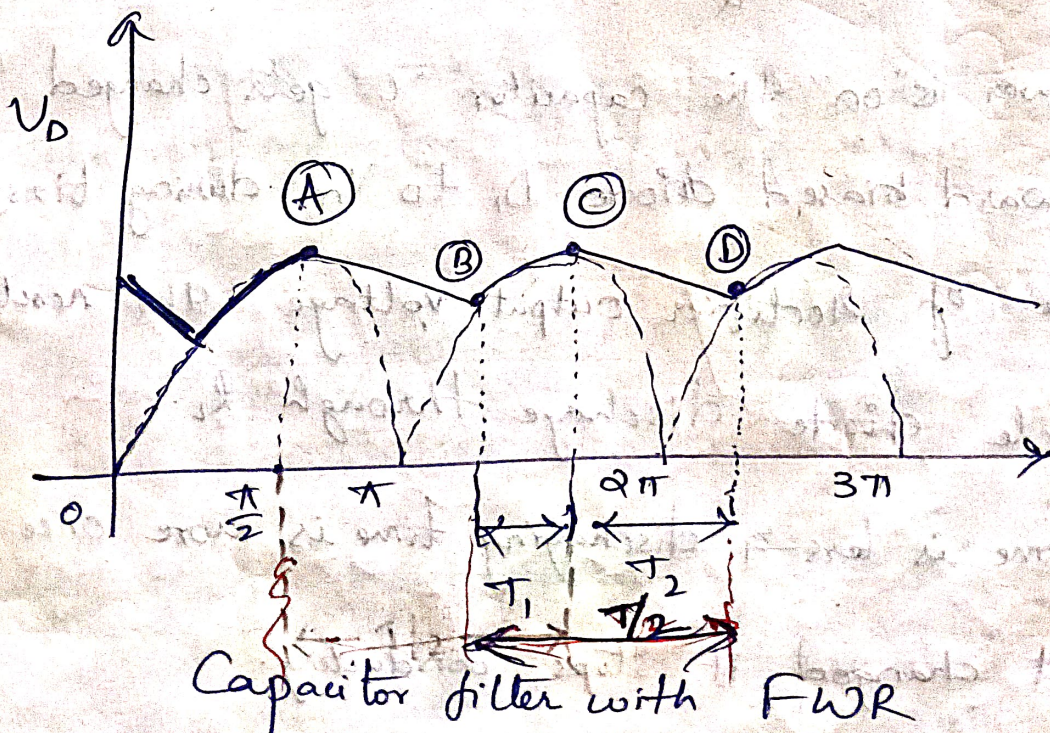
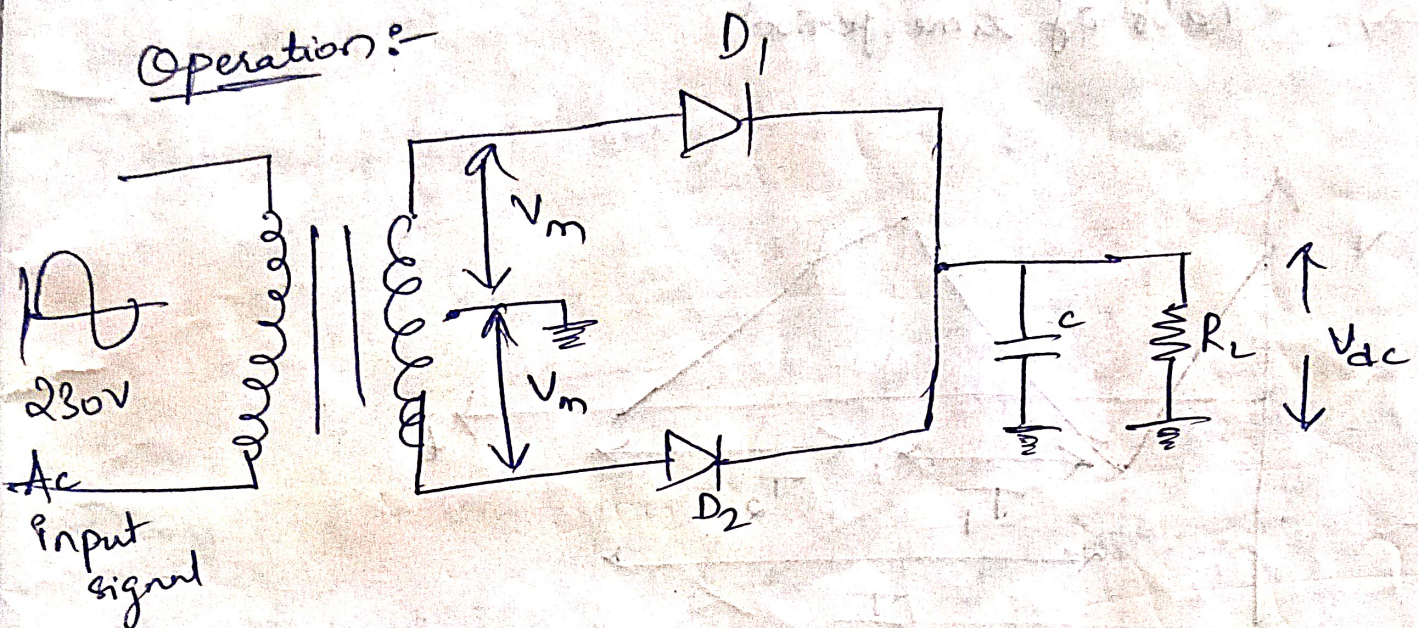
Inductor is series connected & short ckt. for D.C.

* Capacitor filter ?



Capacitor filter with full wave Rectifier (FWR):-

Operation:-



Capacitor filter with FWR

Analysis of capacitor filter

- $T \rightarrow$ Time period of AC input voltage
- $T_1 \rightarrow$ Time for which diode conducting
- $T_2 \rightarrow$ Time for which diode non-conducting
- $\frac{T}{2} \rightarrow$ half of time period

$\rightarrow$ when power is on capacitor 'C' gets charged through forward biased diode D_1 to V_m during first quarter

$\rightarrow$ Ist quarter of AC input signal

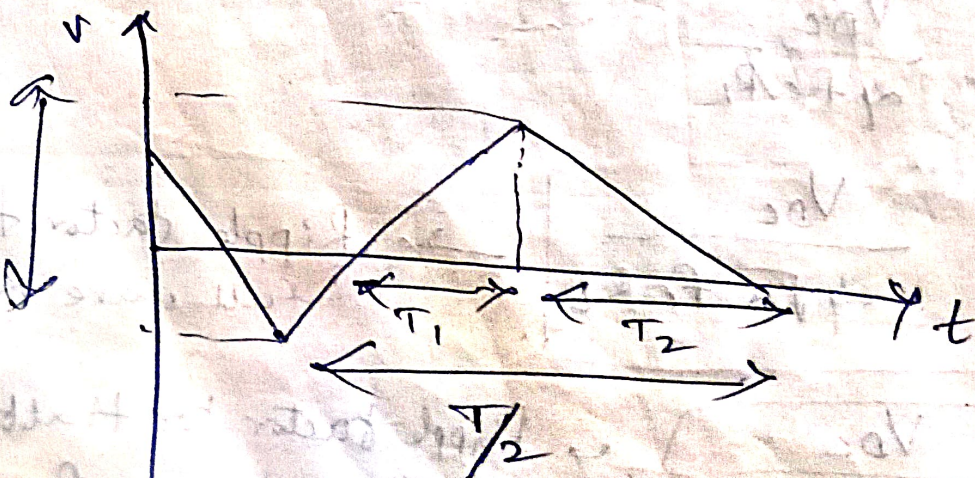
$D_1 \rightarrow$ f.B. & capacitor $\rightarrow$ charge through D_1 (diode)

$\rightarrow$ IInd quarter capacitor 'C' $\rightarrow$ discharge

$\rightarrow$ IIIrd quarter $D_2 \rightarrow$ f.B. & capacitor 'C' $\rightarrow$ charge D_2

$\rightarrow$ IVth quarter capacitor 'C' $\rightarrow$ discharge

$\rightarrow$ The O/p of FWR with capacitor filter is triangular



Here $T_2 \gg T_1$

so neglect T_1

$$T_1 + T_2 = \frac{T}{2}$$

neglect T_1

$$T_2 = \frac{T}{2}$$

Rms value of triangular wave form is

$$V_{rms} = \frac{V_p}{2\sqrt{3}}$$

here Capacitor in charge time [charge gained]

Capacitor in discharge time [charge lost]

charge gained [$Q = CV_p$] — ①

charge lost [$Q = I_{dc} T_2$] — ②

equating both charge gained & charge lost

$$\downarrow$$
$$Q = CV_p$$

$$\downarrow$$
$$Q = CV_p$$

$$\downarrow$$
$$Q = I_{dc} T_2$$

$$C V_p = I_{dc} T_2$$

$$V_p = \frac{I_{dc} T_2}{C}$$

$$\therefore T_2 = \frac{T}{2}$$

$$V_p = \frac{I_{dc} T}{2C}$$

$$[\because T = \frac{1}{f}]$$

$$V_r = \frac{I_{dc} T}{2C}$$

$$\left[T = \frac{1}{f} \right]$$

$$V_r = \frac{I_{dc}}{2fc}$$

$$\left[I = \frac{V}{R} \right]$$

$$\frac{V_{dc}}{R_L}$$

$$V_r = \frac{V_{dc}}{R_L} \frac{1}{2fc}$$

$$V_r = \frac{V_{dc}}{2fc R_L}$$

Peak to peak ripple voltage

Ripple factor $V_{rms} = \frac{V_r}{2\sqrt{3}}$

$$V_{rms} = \frac{V_{dc}}{2\sqrt{3} fc R_L}$$

$$V_{rms} = \frac{V_{dc}}{4\sqrt{3} fc R_L}$$

→ Ripple factor for Full wave Rectifier

$$V_{rms} = \frac{V_{dc}}{2\sqrt{3} fc R_L}$$

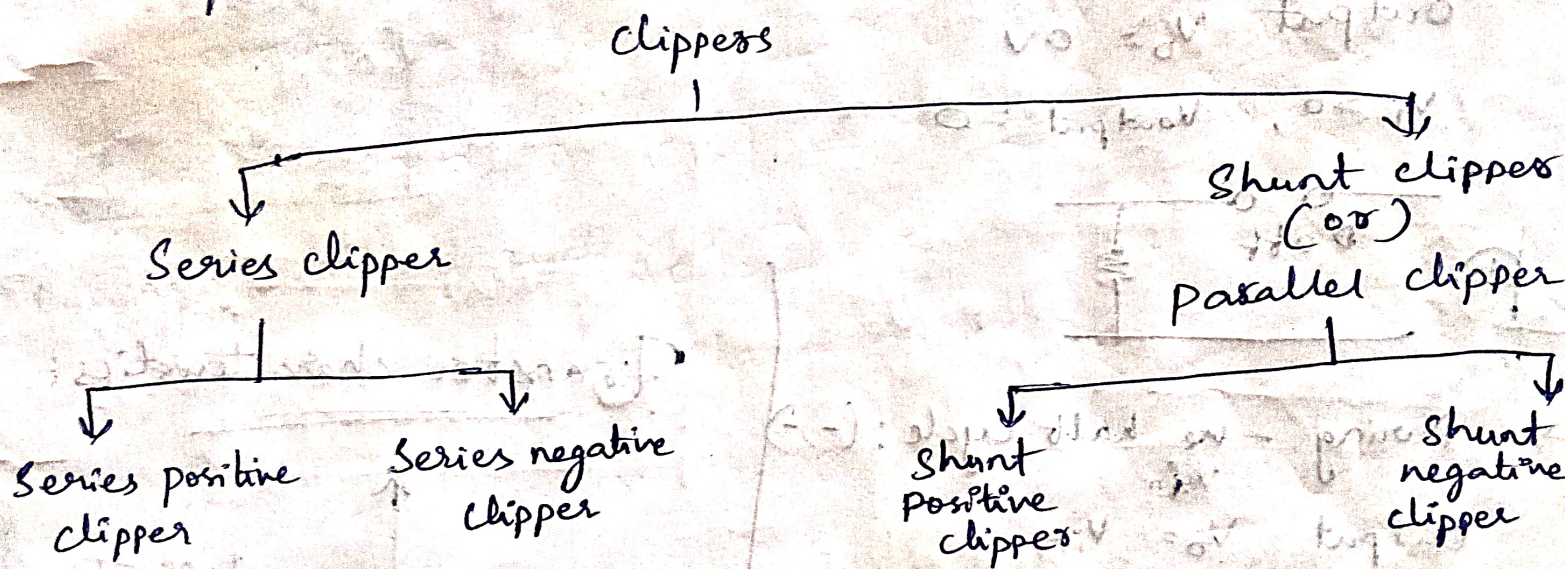
→ Ripple factor for Half wave Rectifier

* Clippers and clampers *

* Clippers :

The circuit which removes the undesired part of signal: clip wave form and transmits only desired part of signal. clipping of waveform is most common technique that applies to input signal to adopt so that they may lie with in operating range of electronic circuit.

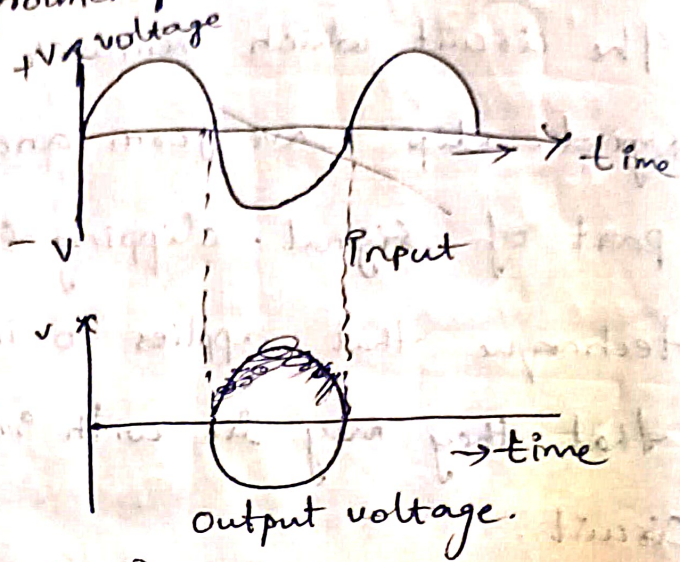
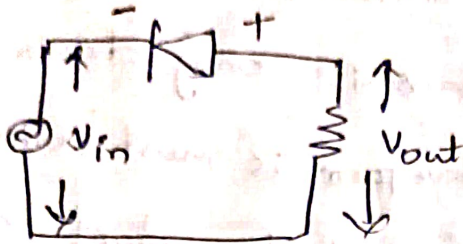
→ Clippers can be classified into two types:



(i) Series Clipper :-

In Series clippers diodes is connected in series with AC input supply.

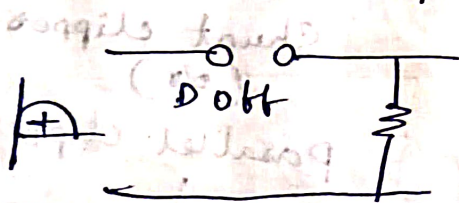
(i) Series positive clipper In this type of clipper Cathode of diode is connected to the input supply and Anode is maintained at ground potential.



→ During positive half cycle: $(-, +)$

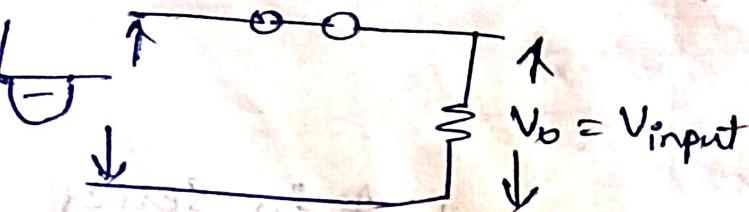
output $V_o = 0V$

$V_i > 0, V_{\text{output}} = 0$

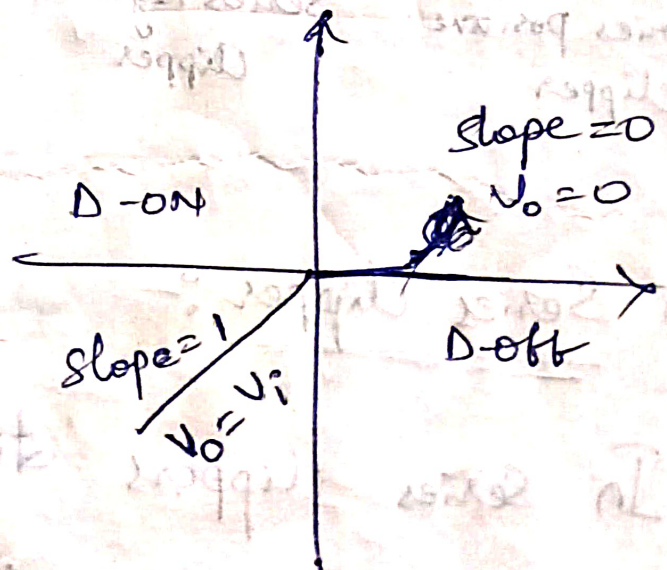


→ During -ve half cycle: $(-, -)$

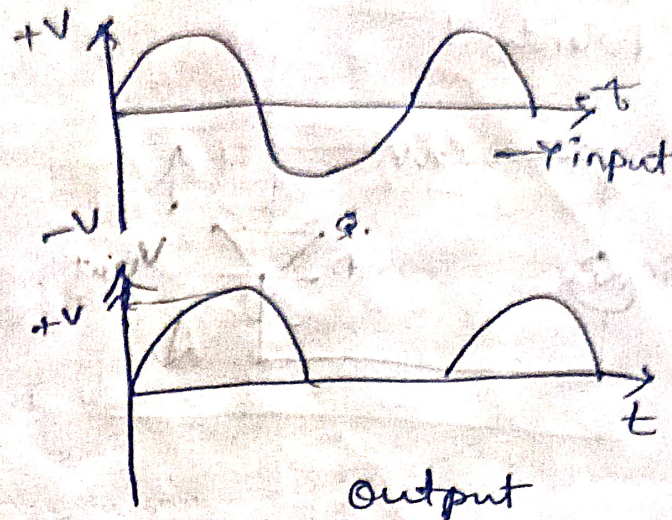
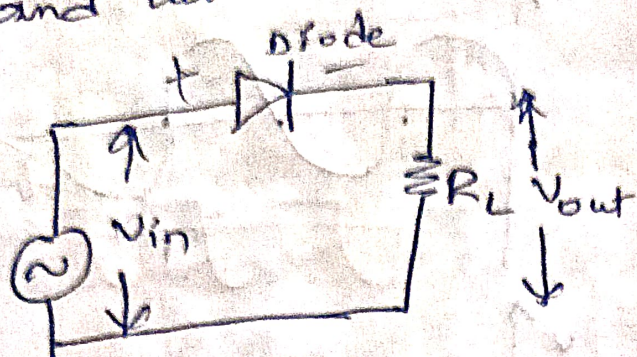
output $V_o = V_{in}$



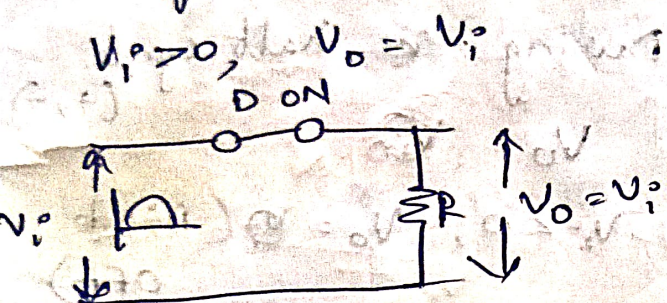
Transfer characteristics:



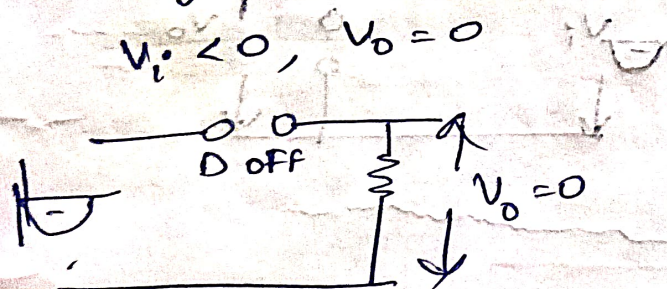
(ii) Series - ve clipper :- In this type of clipper Anode of diode is connected to the input supply and cathode connected to ground potential.



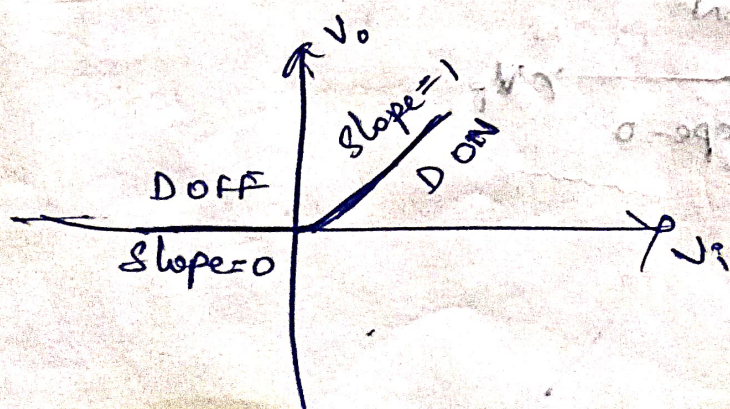
for
 → During positive half cycle: $(+, +)$



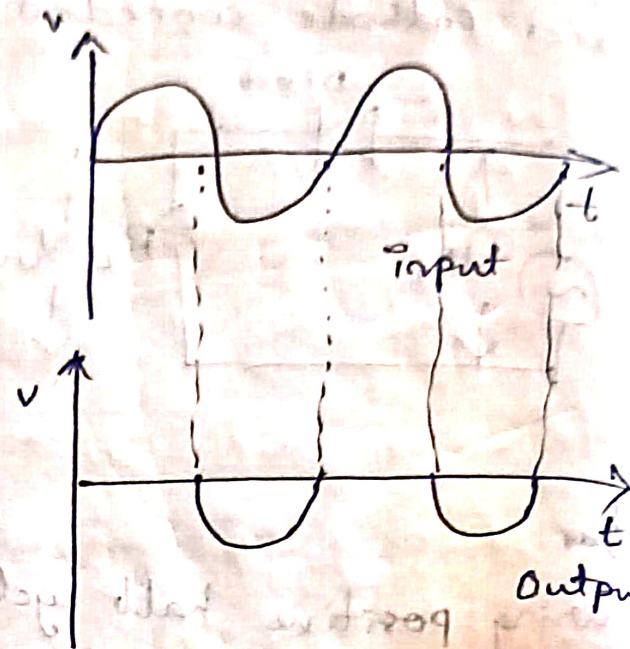
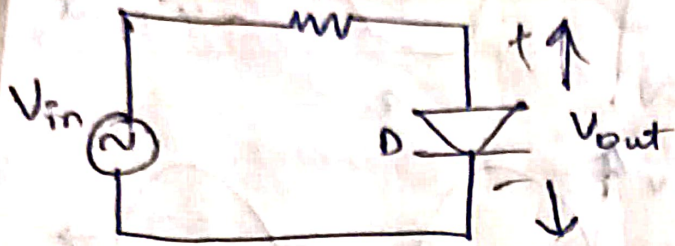
→ During -ve half cycle: $(+, -)$



Transfer characteristics



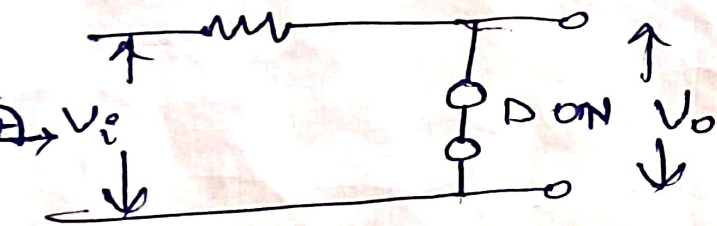
Q1) Shunt positive clipper :- Anode is connected to input through Resistor R, Cathode at ground Potential.



During positive half cycle:

$(+, +)$

$V_i > 0$ then $V_o = V_i$ (diode ON)

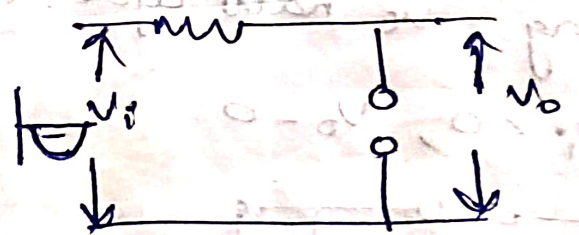


During -ve half cycle

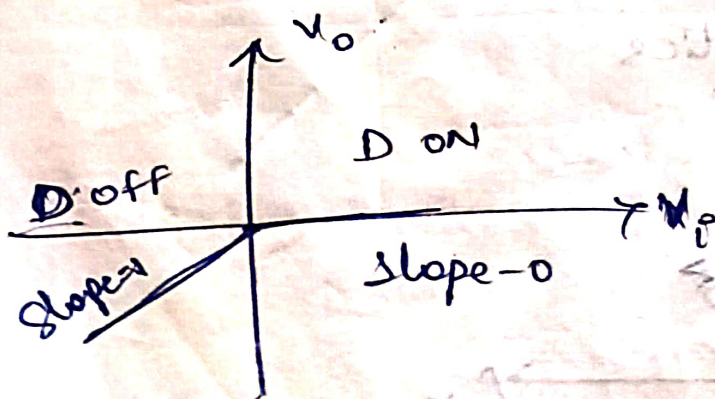
$(+, -)$

$V_o = 0$

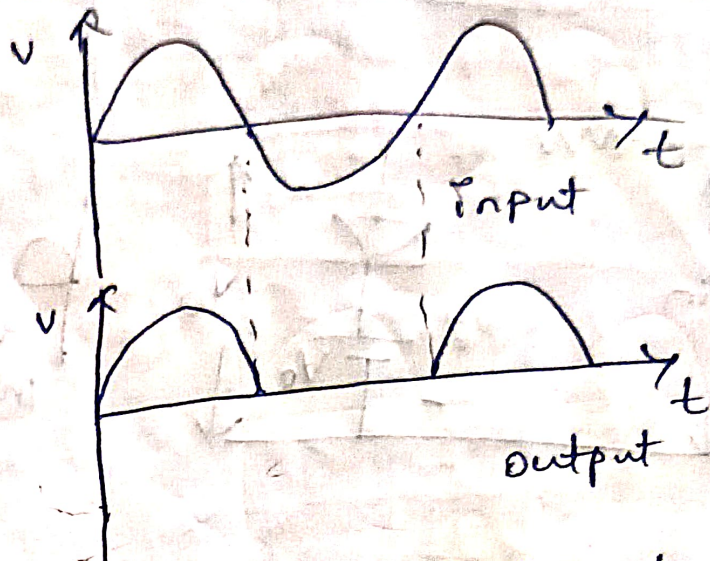
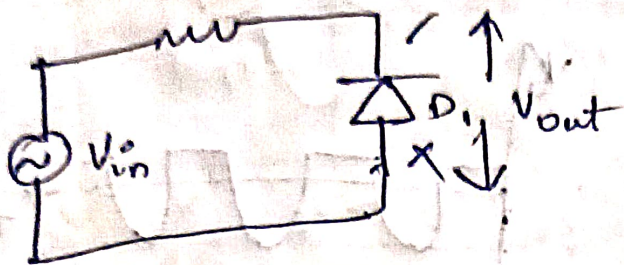
$V_i < 0$, $V_o = 0$ (Diode OFF)



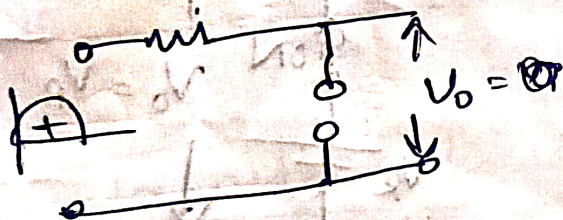
Transfer characteristics:-



(ii) Shunt negative clipper - Cathode is connected to input supply through Resistor R & anode is maintained at ground potential.

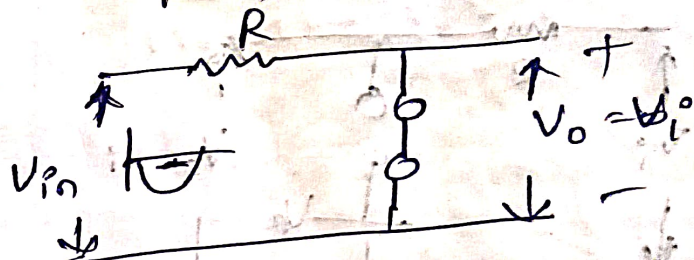


During positive half cycle: $(-, +)$
 $V_i > 0, V_o = V_i$ (Diode off)

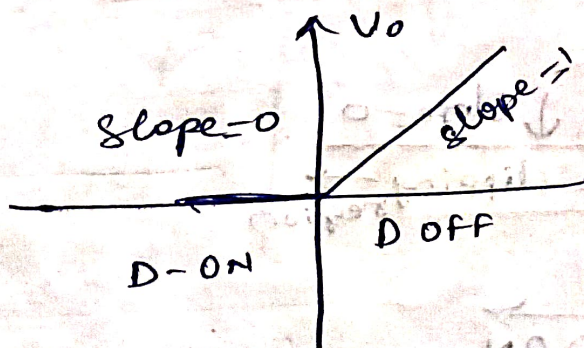


During -ve half cycle: $(+, -)$

$$V_i < 0, V_o = 0$$

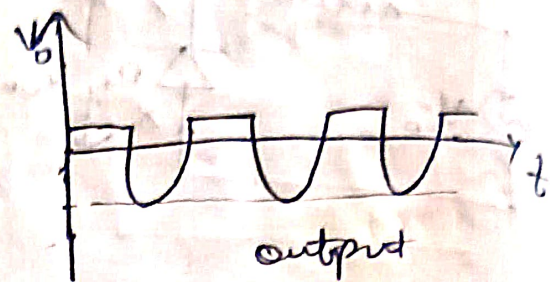
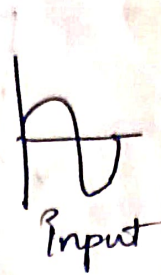
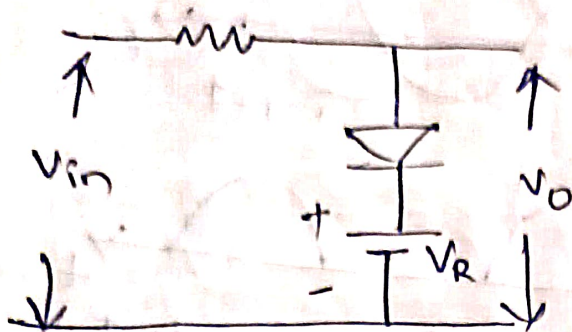


Transfer characteristics:-

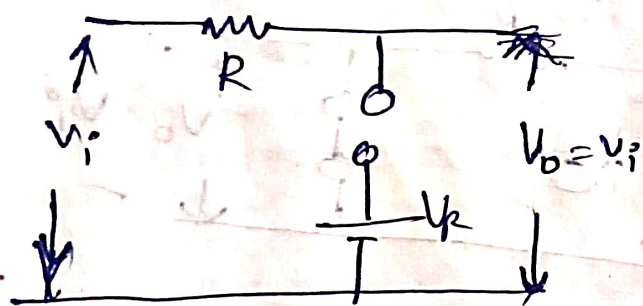


Clipper with biasings (reference voltage) +

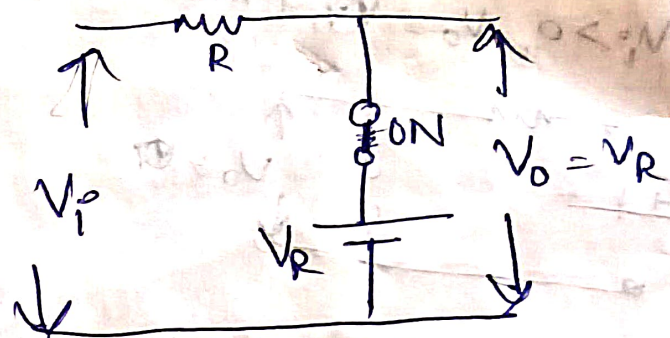
(i) +ve shunt clipper with reference voltage (above)



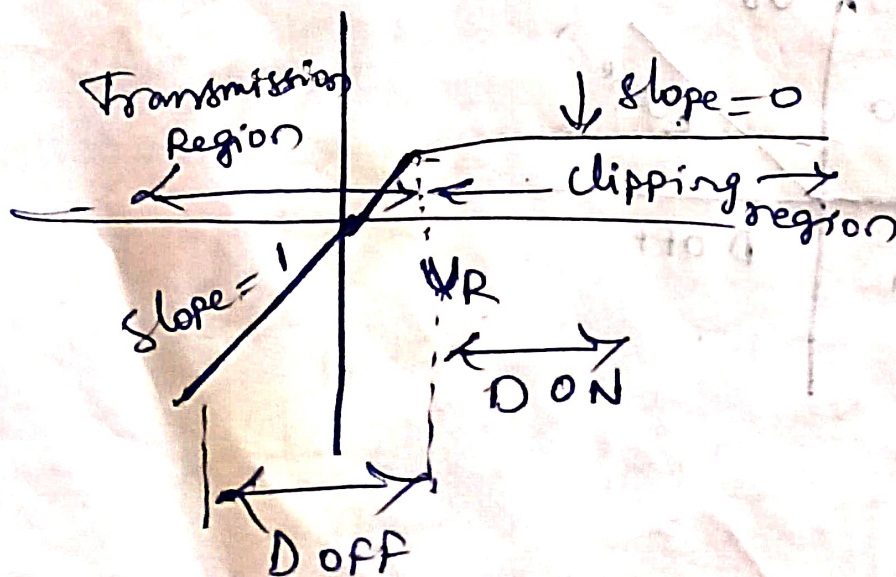
for $V_i < V_R$, $V_o = V_i$
(+ve half cycle)



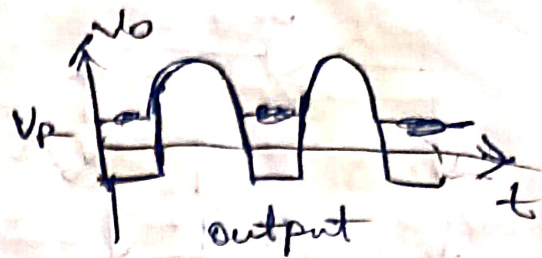
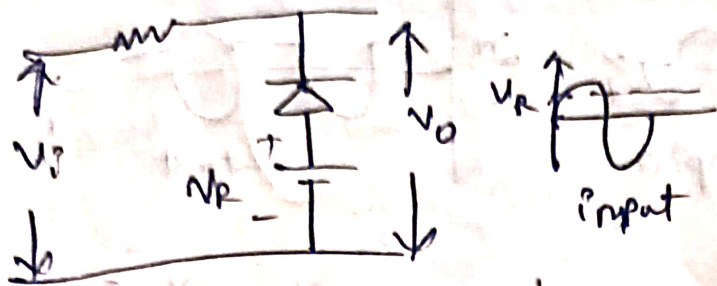
$V_i > V_R$, $V_o = V_R$
(-ve half cycle)



Transfer characteristics

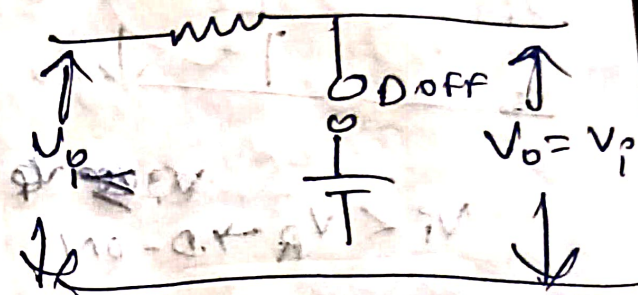
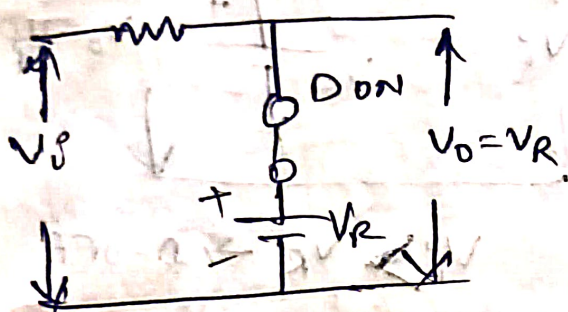


(ii) -ve shunt clipper below reference voltage

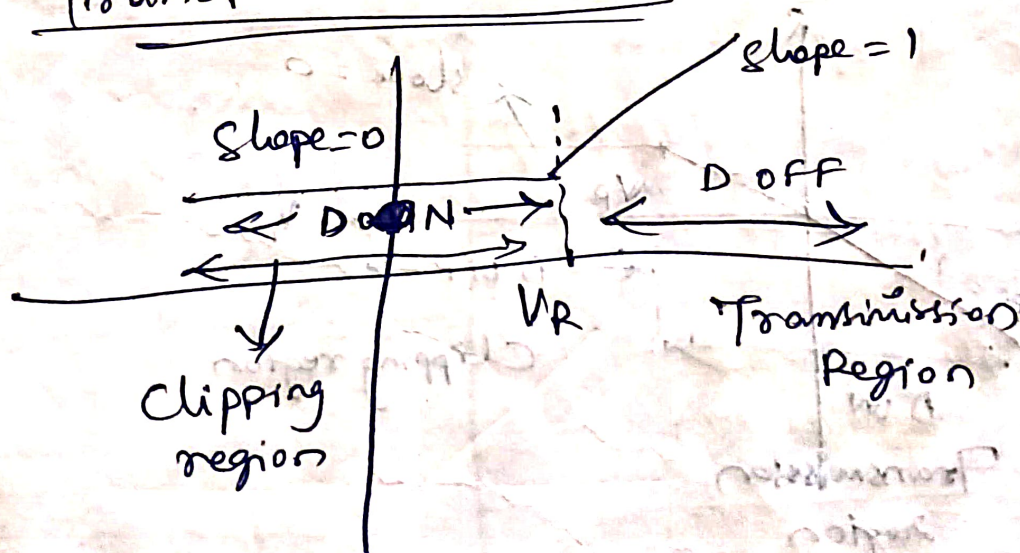


for $V_i < V_R$, $V_o = V_R$ (+ve half cycle)

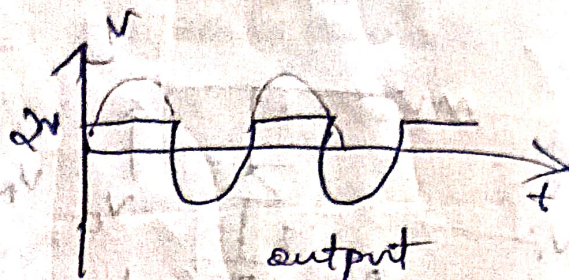
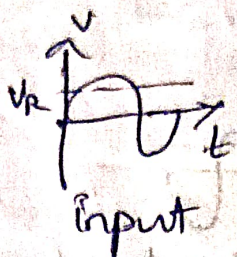
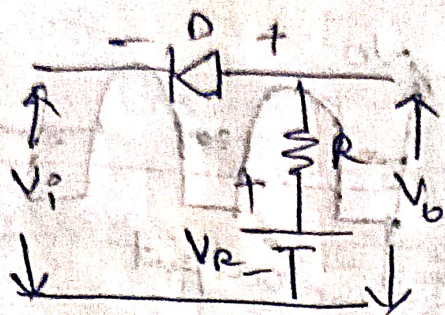
for $V_i > V_R$, $V_o = V_i$ (-ve half cycle)



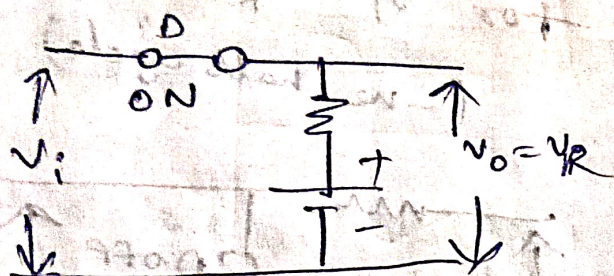
Transfer characteristics



(iii) +ve Series clipper above reference voltage:

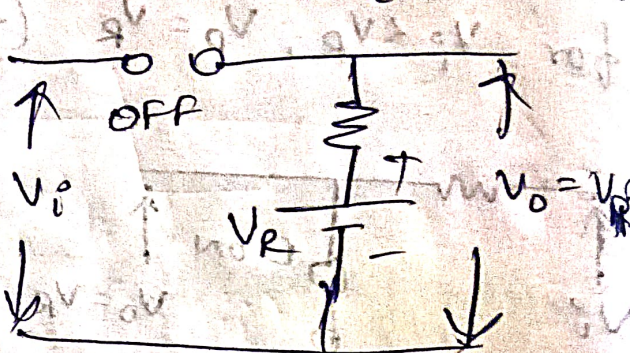


for $V_i < V_R$, $V_o = V_i$ (~~the~~ half cycle)



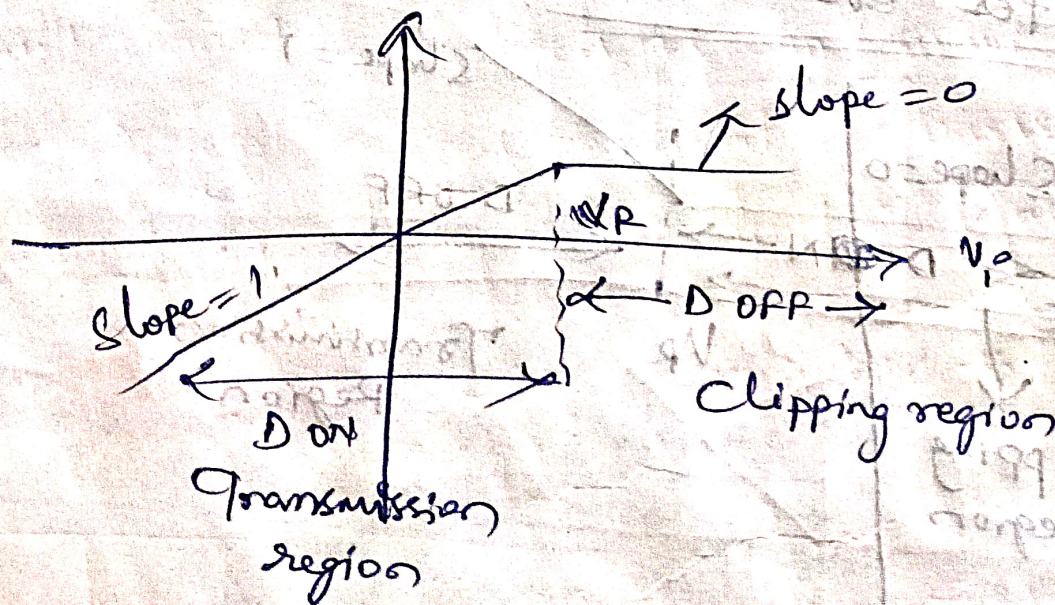
$V_i < V_R \rightarrow D - ON$

for $V_i > V_R$, $V_o = V_R$ (+ve half cycle)

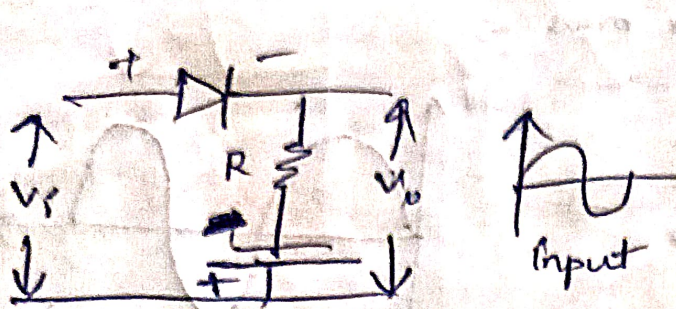


$V_i > V_R \rightarrow D - OFF$

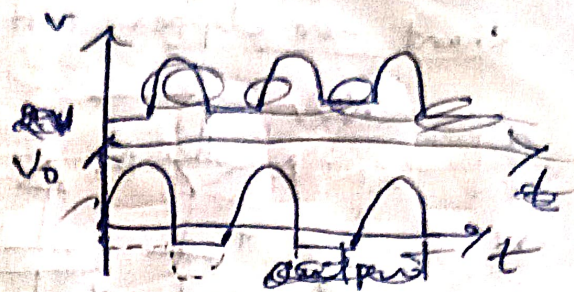
Transfer characteristics:



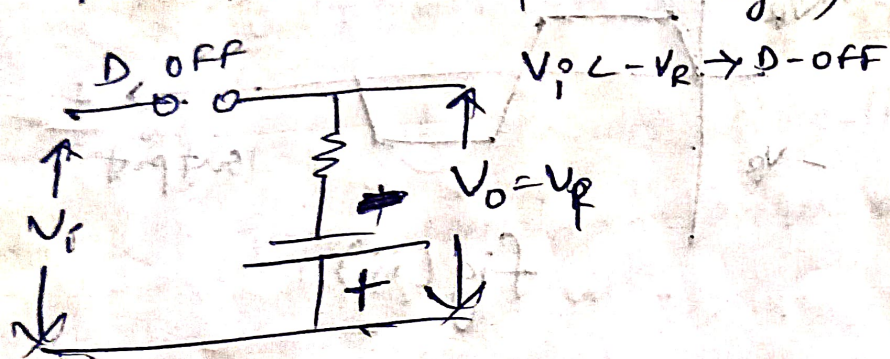
(iv) -ve Series Clipper below reference V_R



Input

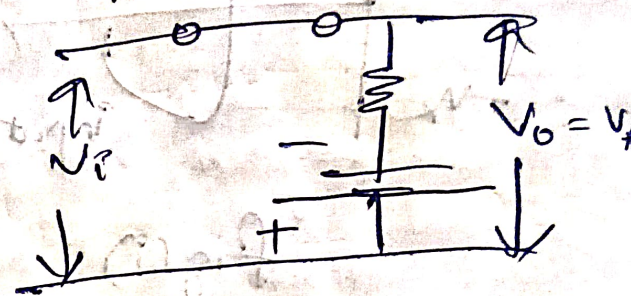


for $V_i < V_R$, $V_o = V_i$ (→ve half cycle)

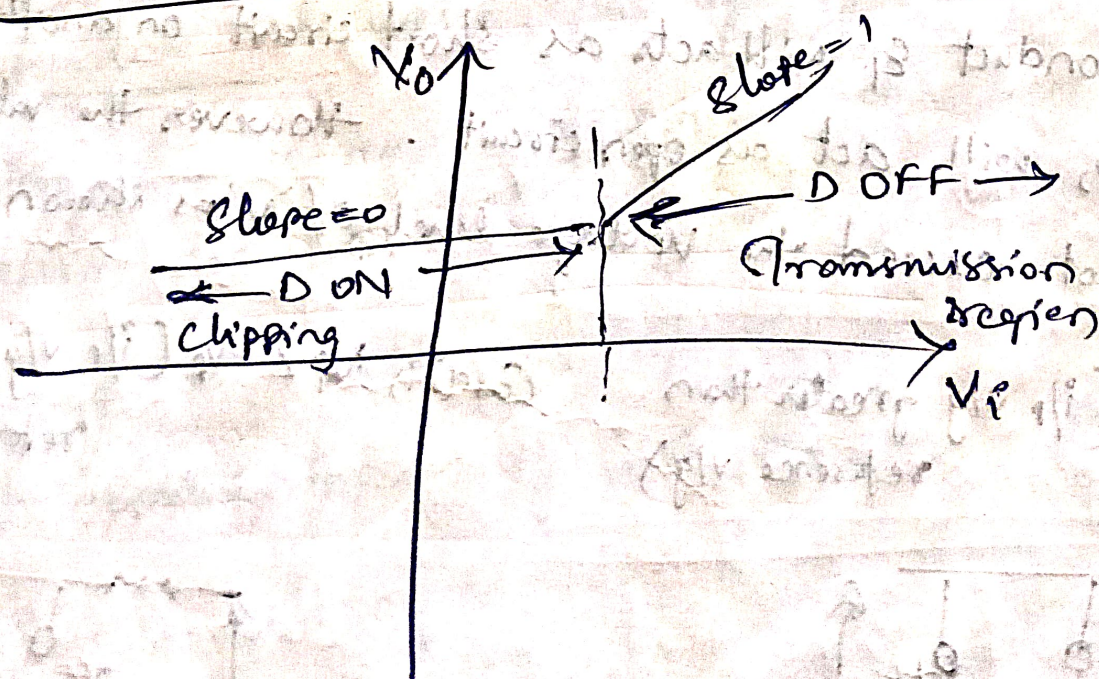


for $V_i > V_R$, $V_o = V_R$ (+ve half cycle)

$V_i > -V_R \rightarrow D$ is ON



Transfer characteristics:-



* Clippers at two Independent levels:

Shunt -ve clipper with -ve bias

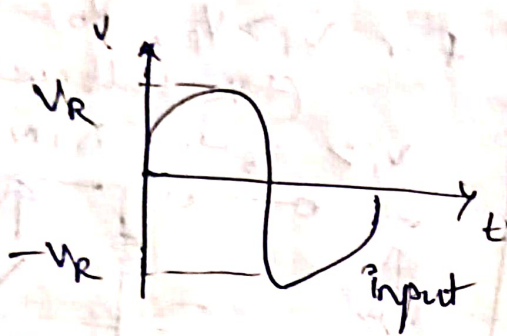
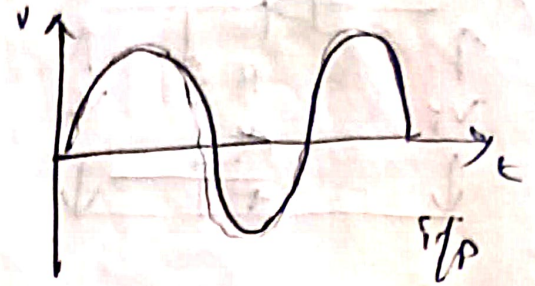
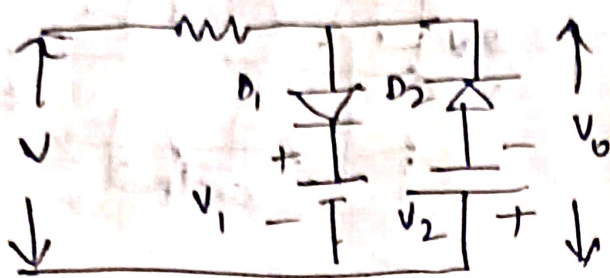


fig (i)

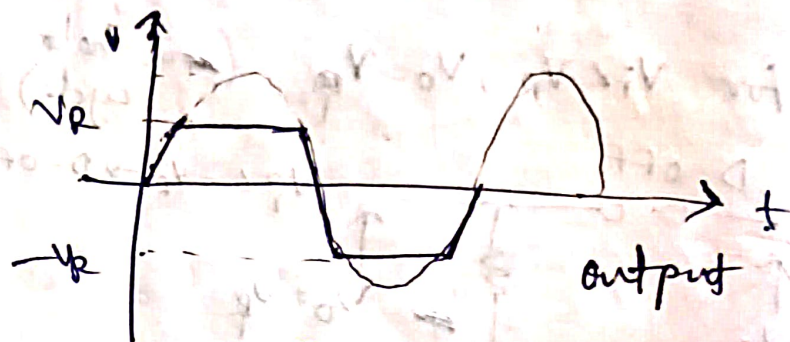
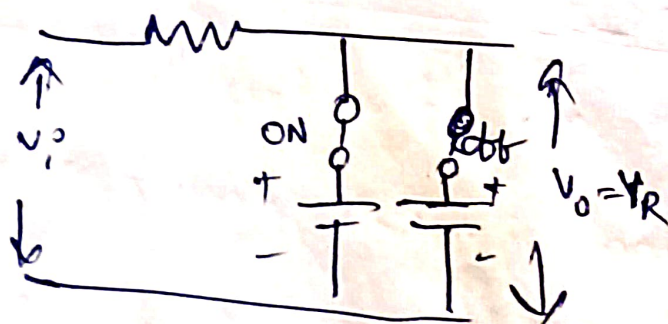


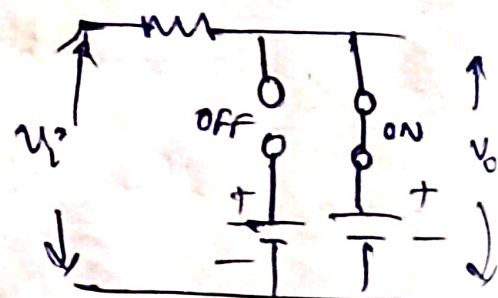
fig (ii)

→ Suppose AC v/g is applied at input terminal of circuit then during the half cycle diode D_1 is F.B. while $D_2 \rightarrow R.B$.
 $\therefore$ Diode will conduct & V_1 will act as short circuit on another hand diode D_2 will act as open circuit. However the value of o/p volts cannot exceed the voltage level of 'V' as shown.

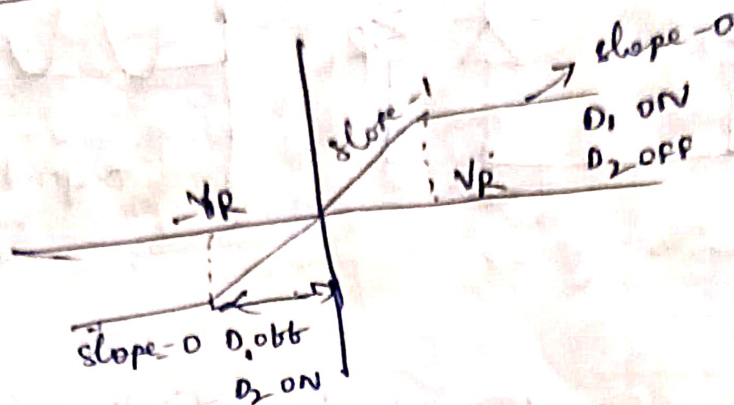
Case (i) $V_i > V_R$ (i/p v/g greater than reference v/g)



Case (ii) $V_i < -V_R$ (i/p v/g less than reference v/g)



Transfer characteristics



* Diode clippers (or) Clampers :-

→ clippers also known as 'restorers', clippers are designed to shift input waveform either above or below reference level of DC.

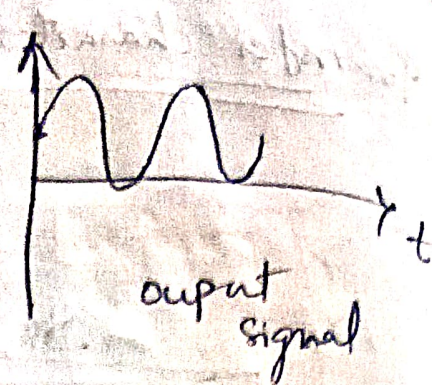
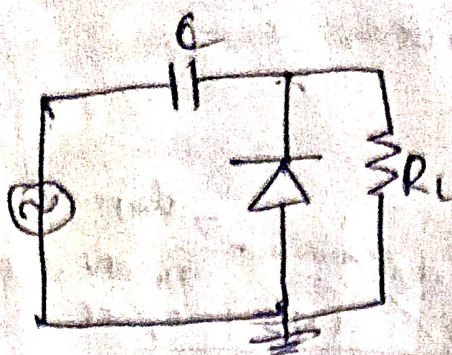
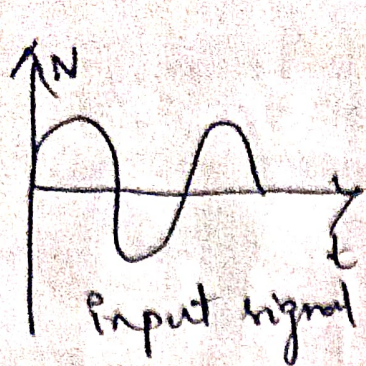
→ clippers are classified into two types :-

- (i) positive clipper
- (ii) negative clipper

(i) positive clipper :- This type of clipper circuit shifts the input waveform in a positive direction as results the waveform lie above DC reference voltage.

→ During +ve half cycle o/p V_g of circuit will be the sum of applied input V_g and the charge stored at capacitor.

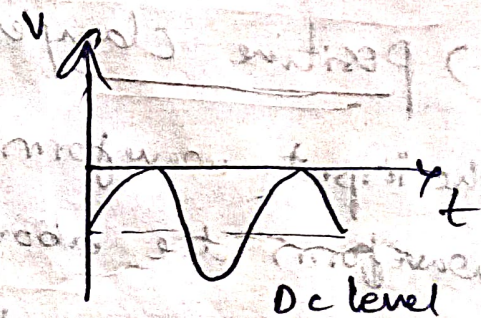
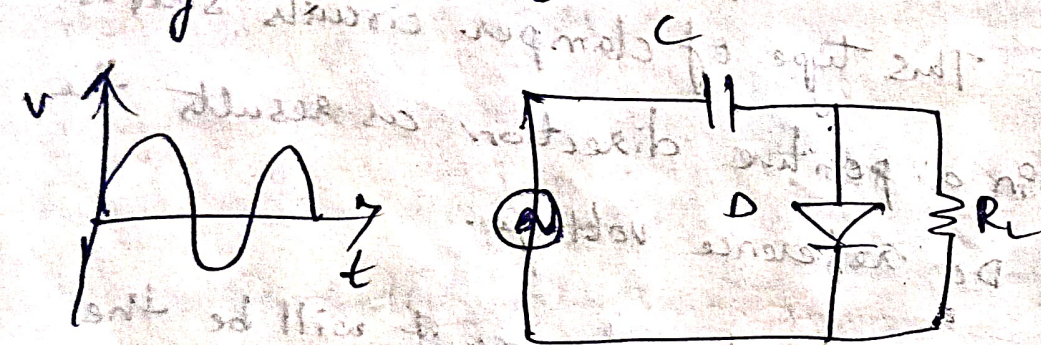
→ During -ve half cycle the diode starts to conduct & charge capacitor very quickly maximum value. the o/p waveform of the clipper shift towards positive direction.



Negative clamper:

→ During positive half cycle of input the diode is forward biased and diode conducts the capacitor charges very quickly

→ During negative half cycle of input diode will reverse bias & this diode will not conduct. The o/p v_o is equal to the sum of applied input v_i & charge stored in capacitor during reverse bias.

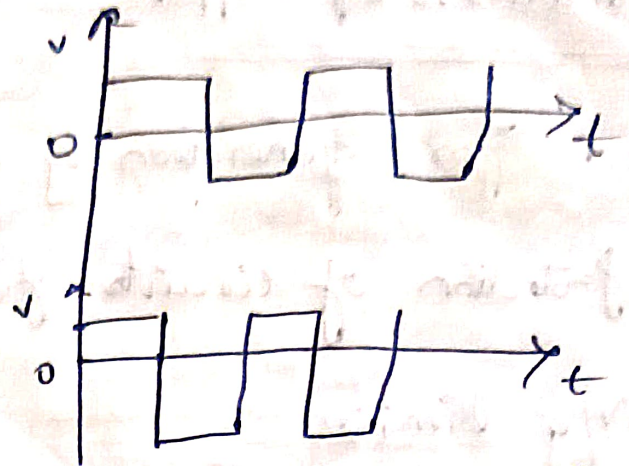
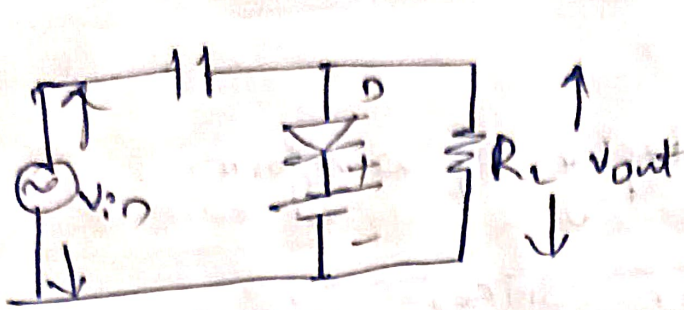


Negative clamper with reference voltage (above reference v_o)

This circuit looks same that of $-ve$ clamper circuit but DC reference supply is connected in series with diode.

The o/p waveform is similar to $-ve$ clamper circuit output waveform but it is shifted towards $+ve$ direction by

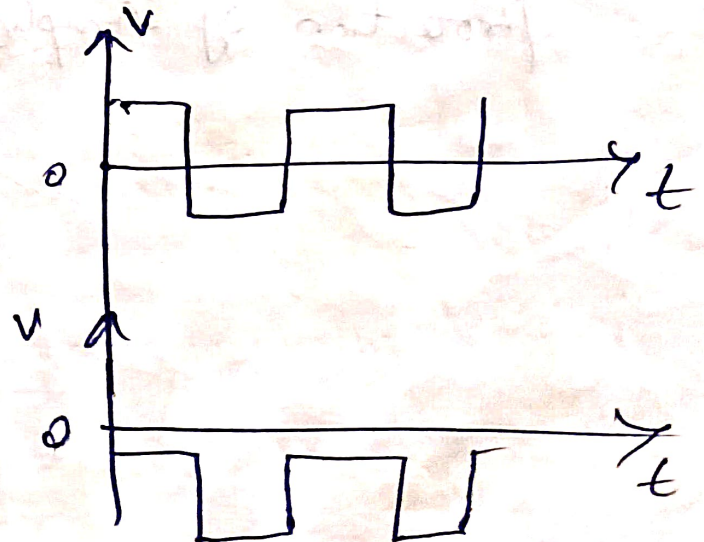
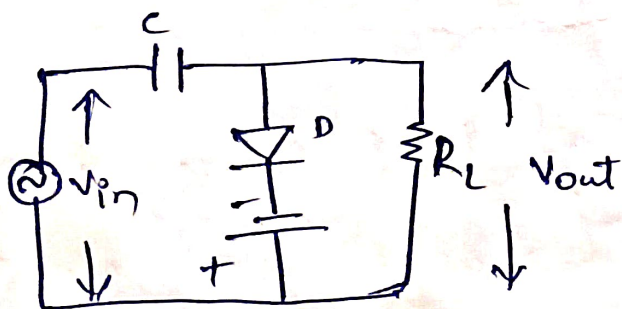
an amount equal to reference V_g at diode.



Negative clamper with reference voltage below reference:

The reference V_g are connected in Reverse (negative to diode negative terminal and positive to the ground) to the diode in series.

Then during the half cycle the diode start conducting current before applying input voltage. The waveform is shifted away from '0' volts towards negative direction an amount of reference voltage.

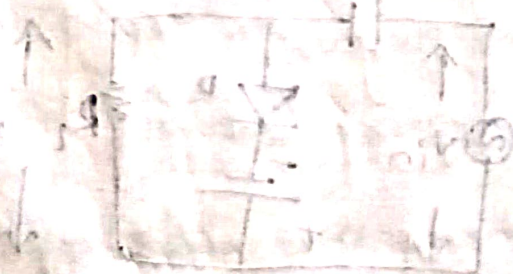


Applications of clippers:-

- 1) used for generation & shaping of waveform
- 2) protection of circuits from spikes
- 3) v/g limiter
- 4) FM transmitter, television circuits.

Applications of clampers:-

- used as direct current restorers.
- used to remove distortions
- used as v/g Multipliers.
- used as base line stabilizer
- protection of Amplifier.



Zener diode - VI characteristics and voltage

Regulation :-

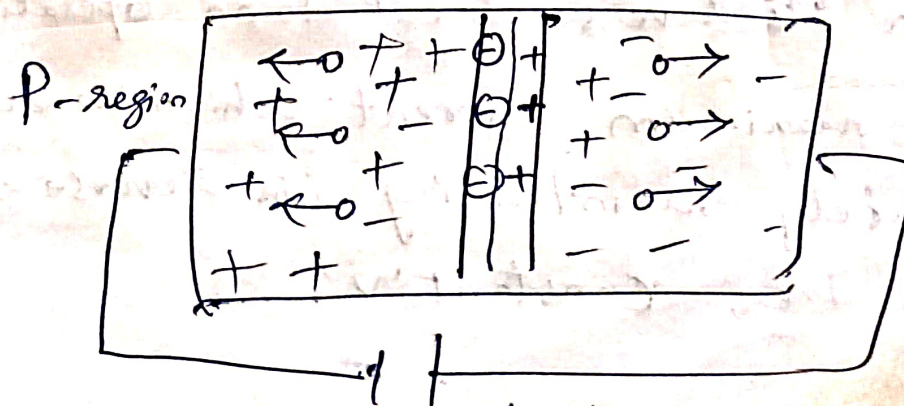
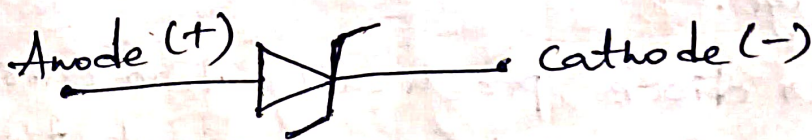
Zener Diode:- A heavily doped semiconductor diode which is designed to operate in reverse direction is known as zener diode.

→ It is a PN junction diode, & it consists of more doping concentration compared to Avalanche PN junction diode.

→ As doping concentration is higher with zener diode, the width of depletion region is narrow at pn junction with zener diode.

→ Zener diode works similarly to Avalanche pn junction diode in F.B & Zener diode works as voltage regulator in R.B.

symbol of zener diode:-

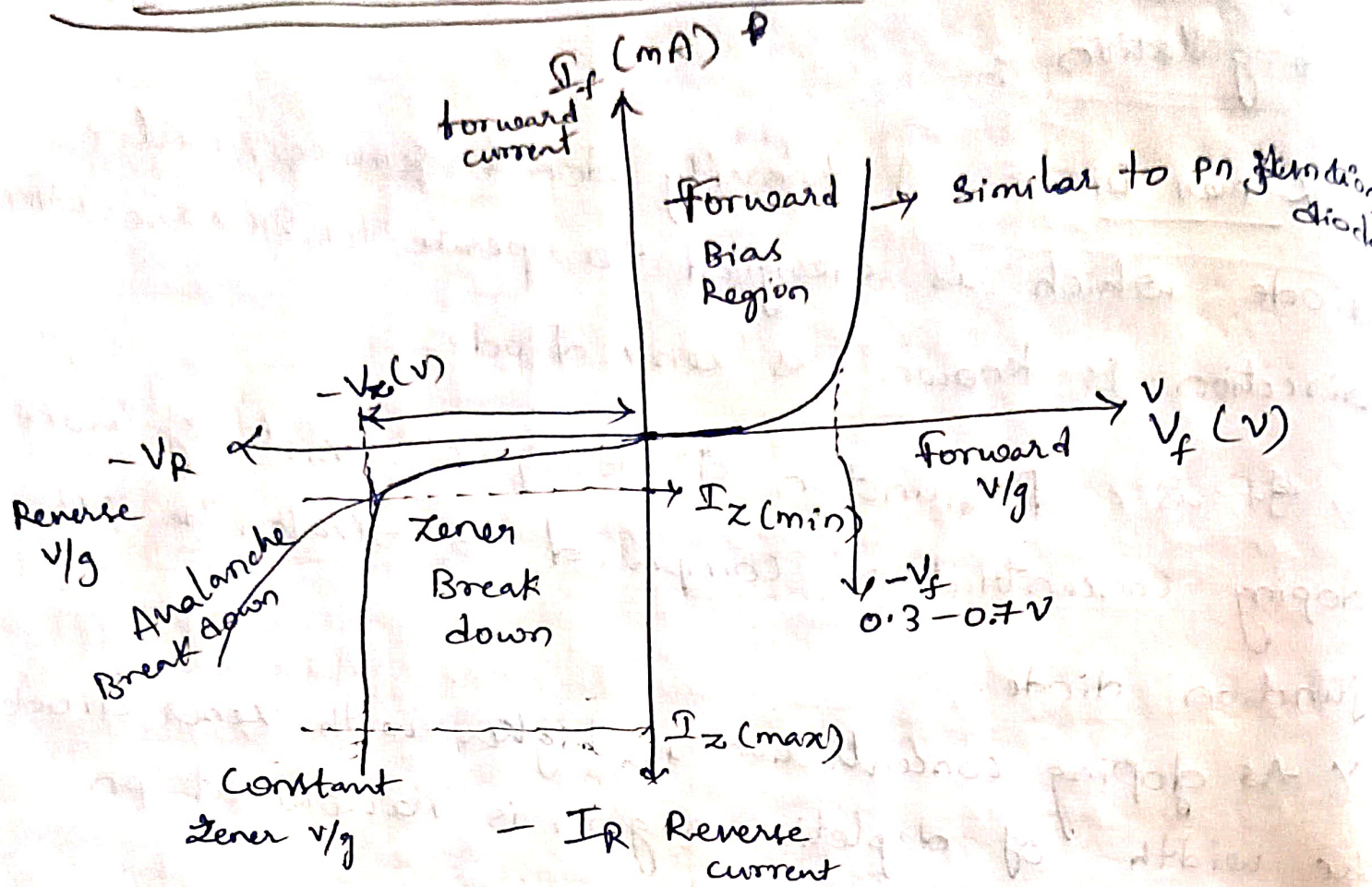


N-region

Depletion Region is narrow

Zener diode in R.B.

V-I characteristics of Zener diode:



V-I characteristics of Zener diode:

→ This works efficiently in R.B conditions. When voltage increases beyond the break down voltage current increases greatly from its normal cutoff value. This voltage is called Zener voltage (or) break down voltage.

- for Zener diode, practically two currents
- (1) $I_Z(\min)$ is minimum current through Zener diode maintain its reverse break down operation.
 - (2) $I_Z(\max)$ is maximum current which Zener diode can take safely maintaining its reverse break down operation i.e., constant 'V'.

→ Zener diode is most suitable for voltage Regulator.

Q. Zener diode as voltage Regulator:

→ It is used in Reverse biased region the current through the diode is very small of order of μA .

→ Here R_S is used to limit the current through the Zener diode.

→ A Zener diode can be used as voltage Regulator only if the o/p v/g is more than the Zener v/g without a Zener diode.

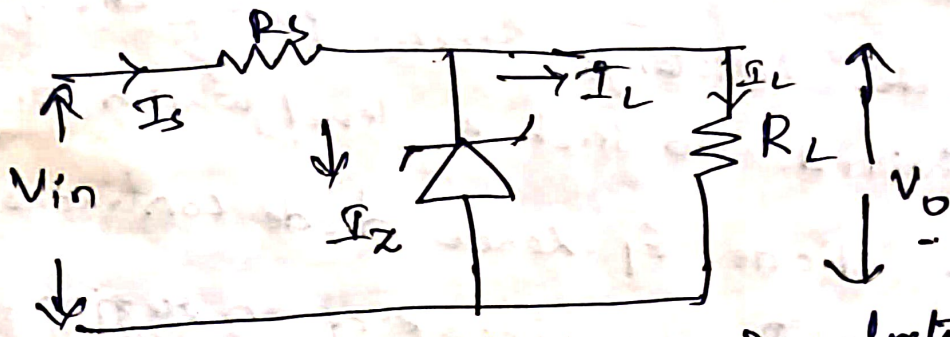


fig: Zener diode as Regulator

load current $I_L = \frac{V_Z}{R_L}$

Source current $I_S = \frac{V_S - V_Z}{R_S}$

Zener current $I_S = I_Z + I_L$

$$I_Z = I_S - I_L$$

Power across Zener

$$P_Z = V_Z \cdot I_Z$$

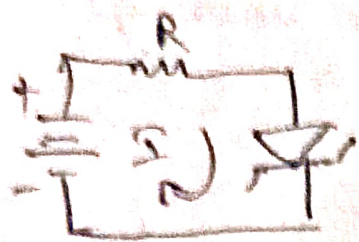


fig (1) - F.B Zener diode

→ fig (1): It represents F.B of Zener diode. It acts similar to PN diode in F.B.

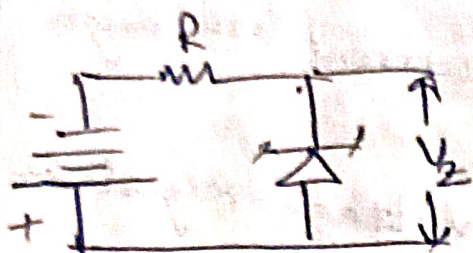


fig (2) R.B of Zener diode

→ fig (2): It represents the R.B of Zener diode, But in R.B it operates in Reverse break down Region.

→ In R.B, reverse current of ~~resistance~~ Zener diode limited using a series resistance. Then power dissipation at junction is limited to such a level which will not damage the diode. & Zener diode continues to operate safely in Reverse break down region.

UNIT - II

BIPOLAR JUNCTION TRANSISTOR (BJT)

* Bipolar junction transistor (BJT) :-

- A BJT is a three-terminal semiconductor device used for amplification & switching applications.
- It is current controlled device.
- In this three terminals are Emitter, Base, collector.
- In this concept of transfer of resistance has given the name Transfer + resistor
Transfer + resistor $\Rightarrow$ Transistor :- The signal is passing from a low Resistance region to high resistance region.

Types of BJT :-

- It is called Bipolar because both electrons & holes participate in current conduction.

Terminals :-

- ① Emitter (E) :- Heavily doped, emits charge carriers (electrons or holes).
- ② Base (B) :- Very thin and lightly doped, controls the transistor action.
- ③ Collector (C) :- Moderately doped, collects charge carriers.

Types of BJT:

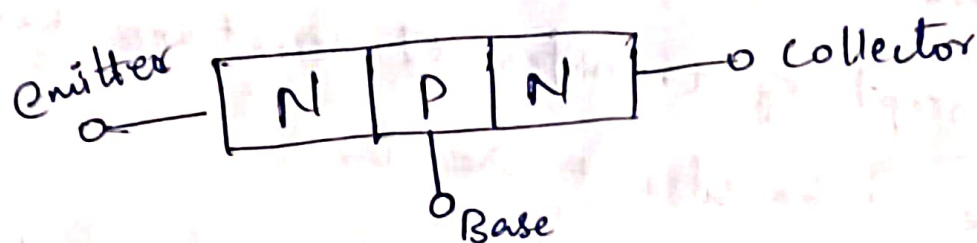
→ 2 types

① NPN type

② PNP type.

① NPN transistor construction and operation:-

Construction:-



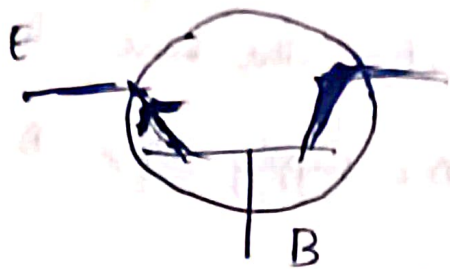
When a transistor is formed by sandwiching a single P-region between two n-regions, then it is called NPN transistor.

* → The middle region of each transistor is 'base' of transistor. This is very thin and lightly doped.

* → Remaining two regions of each transistor is 'base' of transistor. This is very thin and lightly doped.

→ Remaining two regions are called Emitter and collector. Emitter is heavily doped & collector is Moderately doped.

Symbol of NPN transistor



- A transistor has two pn junctions. One junction is between the emitter and base. This is called emitter base junction i.e., ' J_E '.
- The other junction is b/w the base & collector. This is called collector base junction i.e., ' J_C '.

Biased Transistor

- In order to operate transistor properly as an amplifier it is necessary to correctly bias two junctions with external voltages.

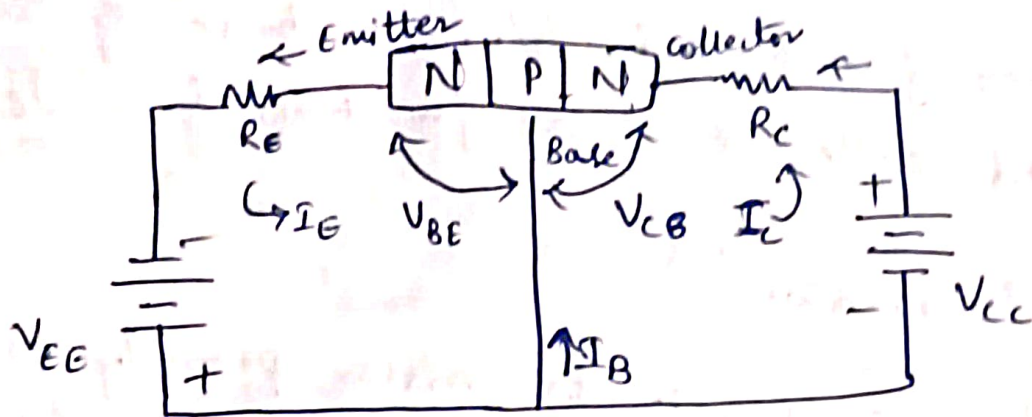
Region	EB junction (Emitter base)	CB junction (Collector Base)
Active	Forward bias	Reverse bias
cut off	Reverse bias	Reverse bias
Saturation	forward bias	forward bias

- The transistor to be in active region the EB junction should be forward biased and CB junction should be reverse biased.

Operation of NPN Transistor

Let us consider the npn transistor. The base-emitter junction is forward biased by d.c. supply V_{EE} . Depletion region width at junction (EB) decreases.

The collector to base junction is reverse biased. Increases depletion region at junction (CB).



→ The forward biased EB junction causes the electrons in the n-type emitter flow towards base.

→ This constitutes emitter current I_E . As electron flows through p-type base they tend to combine with holes in p-region.

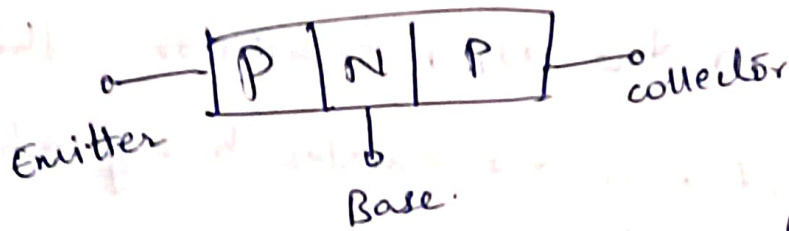
→ We know that the base region is very thin lightly doped. Very thin base region means that free e^- have only short distance to go to reach collector, very few of e^- injected into base from emitter recombine with holes to constitute base current I_B and remaining large no. of e^- cross base region and move through collector region to

Positive terminal of external DC. Thus constitutes collector current I_c . The most of e^- from emitter flow in the collector circuit and very few combine with holes in the base.

Thus collector current larger than base current.

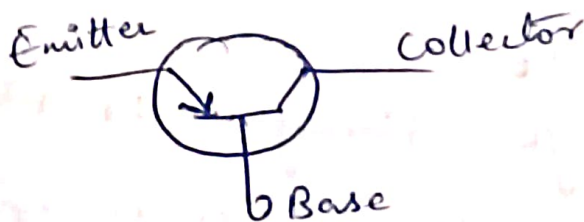
* PNP Transistor construction and operation:

When a transistor is formed by sandwiching a single N-region between two P-regions.



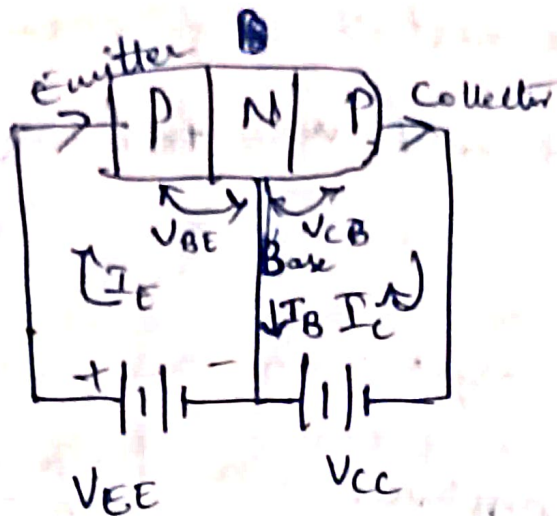
The middle region of each transistor type is called base of transistor, it is lightly doped. collector is heavily doped. Emitter is moderately doped.

Symbol:



Note:- Here also write about biased transistor Explanation.

Operation



$V_{BE} \rightarrow$ v/g at Base emitter

$V_{CE} \rightarrow$ v/g at collector emitter

$I_B \rightarrow$ Base current

$I_E \rightarrow$ Emitter current

$I_C \rightarrow$ collector current

$V_{EE} \rightarrow$ External dc v/g at emitter base

$V_{CC} \rightarrow$ External dc v/g at collector base.

→ The pnp transistor has its base v/g's V_{EE} & V_{CC} reversed from those in the npn transistor. This is necessary to forward bias the emitter base junction & reverse-bias the collector base junction.

→ The f.b EB junction causes the holes in the p-type emitter to flow towards the base. This constitutes the emitter current I_E .

→ As these holes flow through the n-type, base, they tend to combine with e^- s in n-region (base). As the base is very thin and lightly doped, very few of the holes injected into the base from the emitter recombine with e^- s to constitute base current, I_B .

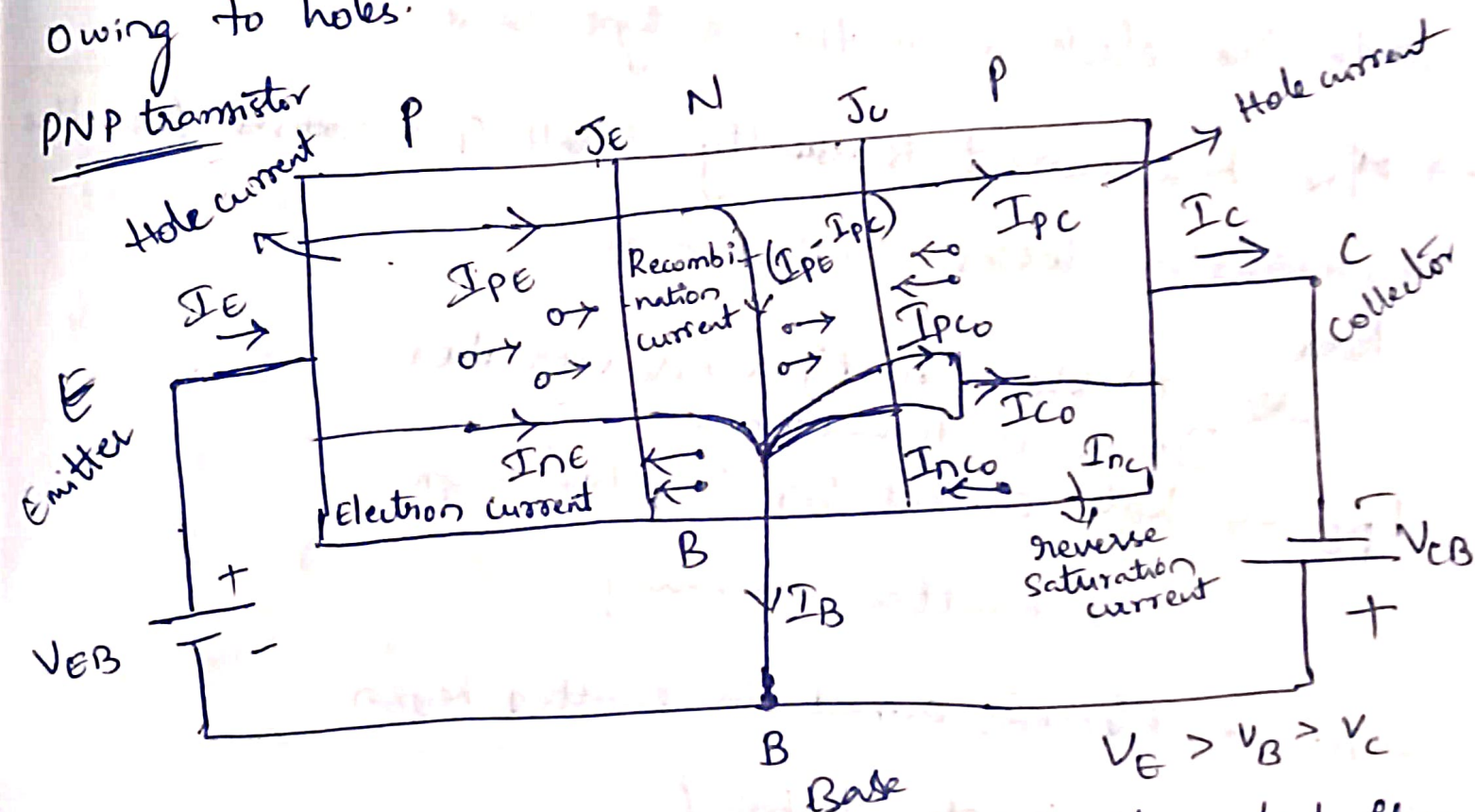
→ The remaining large no. of holes cross the depletion region and move through the collector region to the -ve terminal of the external dc source.

→ This constitutes collector current I_C . Thus the hole flow constitutes the dominant current in an pnp transistor.

* Current Components and Transistor Actions:-

→ Current components in a transistor:-

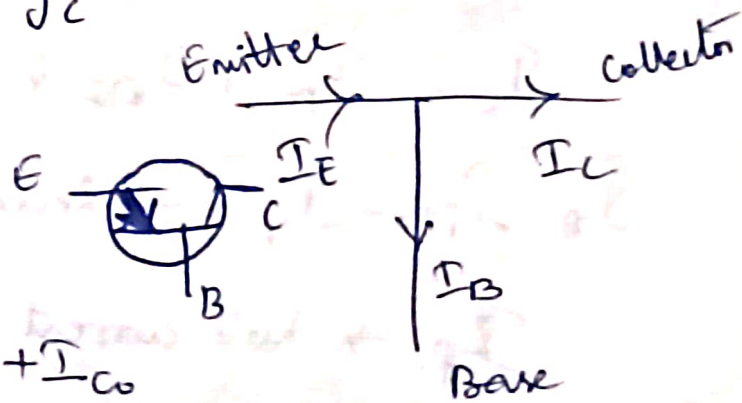
→ The conduction of current in NPN transistor is owing to electrons and in PNP transistor, it is owing to holes.



→ In the fig. we show the various components which flow across the forward biased emitter junction J_E & the reverse-biased collector junction J_C .

$J_E \rightarrow$ forward biased

$J_C \rightarrow$ Reverse biased



$$I_C = I_{pc} + I_{co}$$

→ Emitter current I_E consists of hole current I_{pE} holes crossing from the emitter to base and electrons current I_{nE} electrons crossing from base into the emitter.

→ Doping of the emitter is larger than the doping of the base.

→ Not all the holes crossing the emitter junction J_E reach the collector junction J_C because some of them combine with the electrons in the n-type base.

→ The base current is usually small & accounts for the recombination losses in the base.

here

I_E (Emitter current) $\approx I_{nE} + I_{pE}$
 J_E is in forward bias;

$I_{pE} \rightarrow$ hole current in Emitter region
[Emitter to base]

$I_{nE} \rightarrow$ Electron current in emitter Region
[Emitter to base]

$I_E = I_{pE} + I_{nE} \rightarrow$ total emitter current (E to B)

$I_C = I_{pC} + I_{nC} \rightarrow$ total collector current

$I_B = I_{pE} - I_{pC} \rightarrow$ Recombination current

$I_{pC} \rightarrow$ hole current in collector region

J_c is in Reverse bias

$I_{nco} \rightarrow$ Reverse saturation current due to electron e^-
 direction of I_{nco} is from Base to collector

$I_{pco} \rightarrow$ Due to holes direction of current from
 Base to collector

Total Reverse saturation current (I_{co}) =

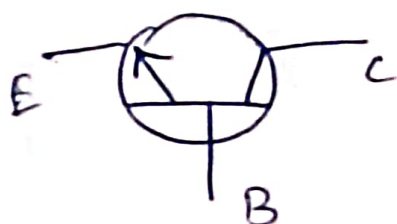
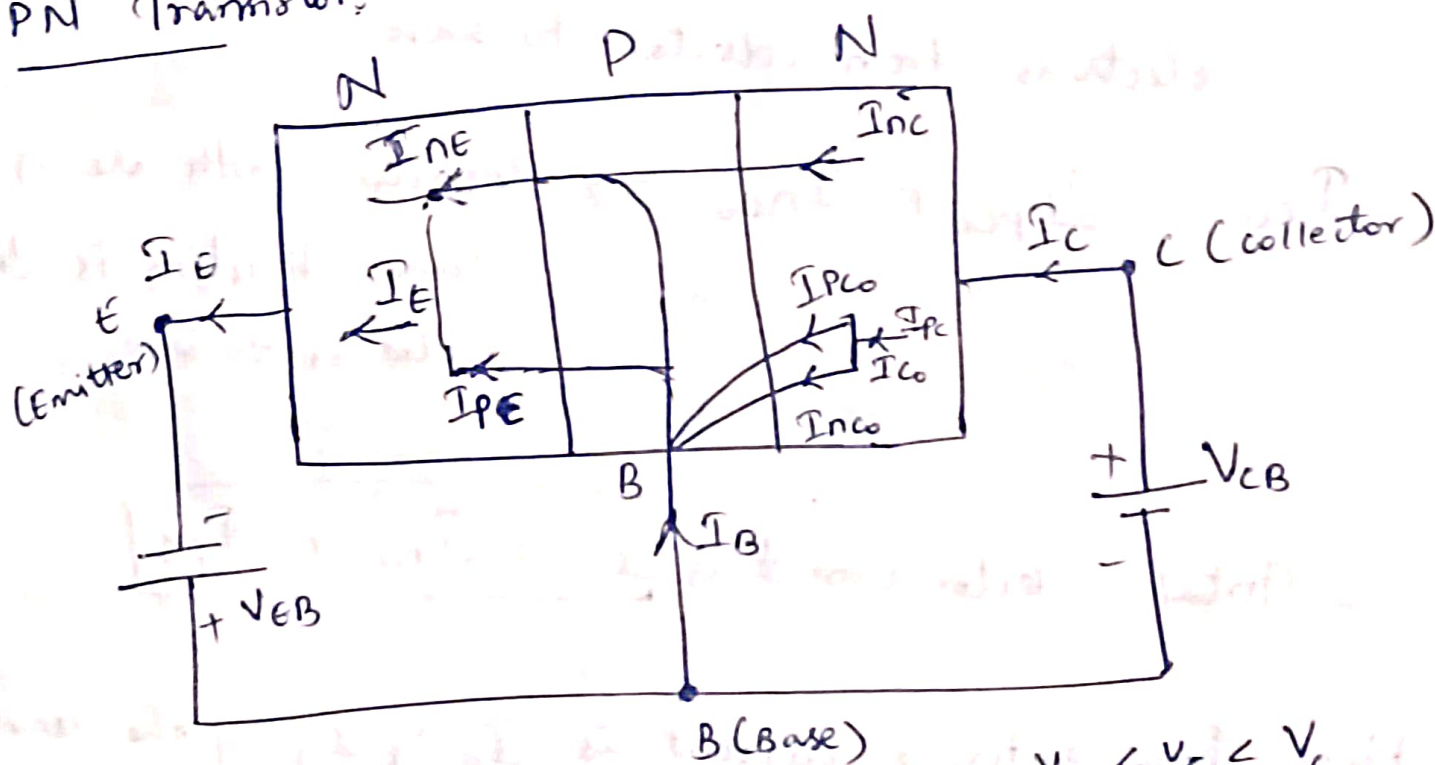
$$I_{co} = I_{nco} + I_{pco}$$

Direction of current from B to C

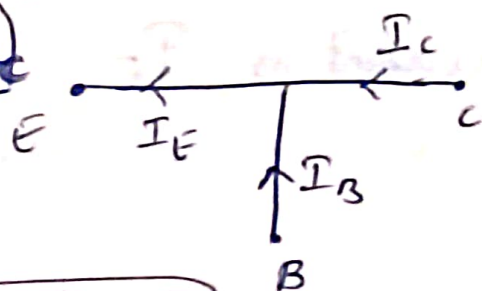
$I_{pc} \rightarrow$ Base to collector (B to C)

$I_{co} \rightarrow$ Base to collector (B to C)

NPN Transistor:



$$I_C = I_{nC} + I_{pC}$$



$$I_E = I_B + I_C$$

I_E is in forward bias

$I_{NE} \rightarrow$ electron current in emitter region

$I_{PE} \rightarrow$ hole current in emitter region

$I_E = I_{PE} + I_{NE}$ its direction is Base to emitter

and it is outwards from Transistor

$I_{NC} =$ ~~collector~~ electron current in collector region
and its direction is from collector to base.

$I_{PCO} \rightarrow$ Reverse saturation current due to holes from collector to Base.

Similarly $I_{NCO} \rightarrow$ Reverse saturation current due to electrons from collector to base.

$I_{CO} = I_{PCO} + I_{NCO} \Rightarrow$ Because both are in same direction is from collector to base.

Total collector current is $I_C = I_{NC} + I_{PC}$

Here ~~Base~~ entering current is I_C & I_B & the leaving

current is I_E i.e.,

$$I_E = I_B + I_C$$

Current Parameters :

(i) Emitter efficiency (η) :

It is the ratio of current of injected carriers at emitter base junction to total emitter current.

$$\eta = \frac{\text{current of injected carriers at JE}}{\text{Total emitter current}}$$

$$\eta = \frac{I_{PE}}{I_{PE} + I_{NE}} = \frac{I_{PE}}{I_E}$$

(ii) Transport factor (β^*) : It is the ratio of injected carrier current reaching at collector base junction J_C to injected carrier current at emitter base junction J_E

$$\beta^* = \frac{I_{PC}}{I_{PE}}$$

(iii) Large signal current gain (α) : It is the ratio of current due to injected carrier I_{PC} to total emitter current I_E .

$$\alpha = \frac{I_{PC}}{I_E} \quad \left| \quad \alpha = \frac{I_C - I_{C0}}{I_E} \Rightarrow \alpha I_E = I_C - I_{C0} \right.$$

$$I_C = \alpha I_E + I_{C0}$$

' I_{C0} ' Very small, so neglect I_{C0}

$$\boxed{I_C = \alpha I_E}$$

* BJT Configurations and its input & output characteristics

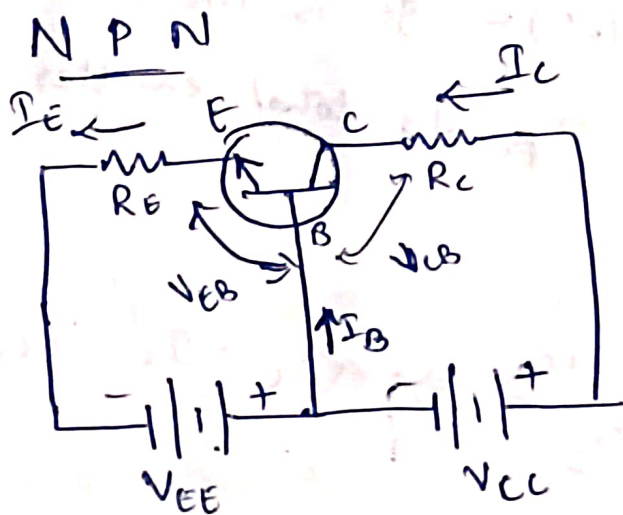
The transistor can be connected in a circuit

following three configurations.

- (i) common base configuration (CB)
- (ii) common emitter configuration (CE)
- (iii) common collector configuration (CC)

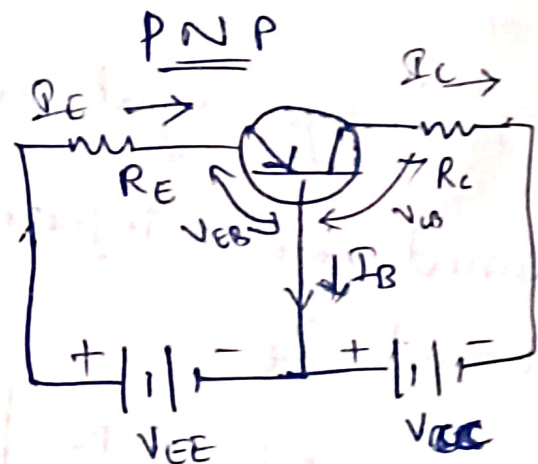
* (i) common Base configuration (CB) ÷

In this configuration, input is applied between emitter and base and output is ~~between~~ taken from the collector and base. Base is common for both input and output.



fig(1) common base configuration using NPN transistor.

(or)



fig(2) common base configuration using PNP transistor.

Here input current is I_E | Emitter-Base $\rightarrow$ forward bias
Output current is I_C | collector-Base $\rightarrow$ reverse bias

Amplification factor α is used in this configuration

$$\alpha = \frac{\text{Output current}}{\text{Input current}} = \frac{I_C}{I_E}$$

$$\alpha = \frac{I_C}{I_E}$$

$$\boxed{I_C = \alpha I_E}$$

' α ' ranges from 0.9 to 0.98

The o/p current is majority current (I_C) + minority current is I_{CBO}

$$\times \text{ Total } I_C = I_C + I_{CBO}$$

$$\boxed{I_C = \alpha I_E + I_{CBO}} \quad \times$$

$\rightarrow$ Emitter $\rightarrow$ Input terminal

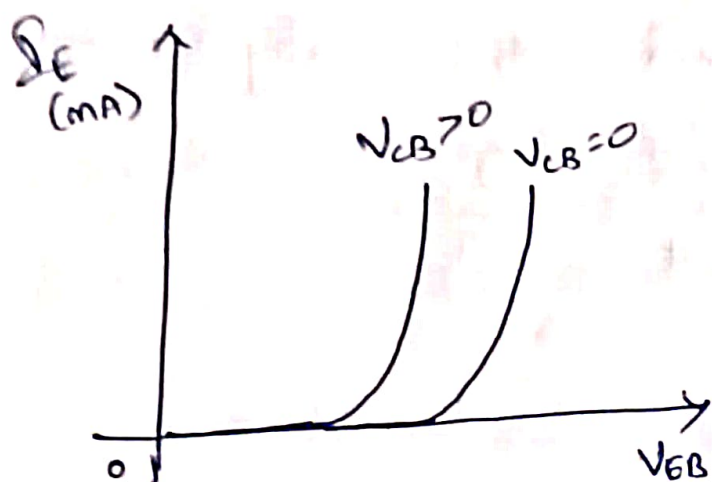
$\rightarrow$ collector $\rightarrow$ output terminal

$\rightarrow$ Base $\rightarrow$ common to both input and output.

Emitter - Base $\rightarrow$ F.B

collector - Base $\rightarrow$ R.B

Input characteristics of CB configuration:-



i) when V_{CB} is kept constant as zero

I_E is increased rapidly by increasing V_{EB}

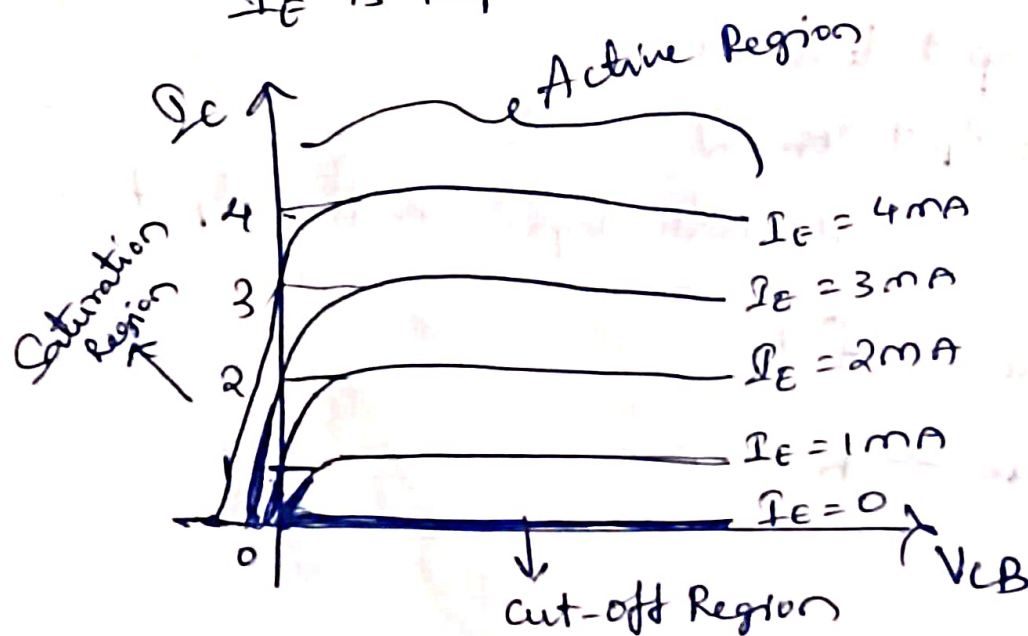
$V_{CB} = 0$; $I_E \uparrow$, & $V_{EB} \uparrow$

(ii) when V_{CB} is increased, the width of the base region is decreased.

→ Then the curve shifts towards left.

Output characteristics of CB configuration:-

→ To determine the output characteristics I_E is kept constant.



$$I_E \approx I_C$$

* for a constant value of I_E , I_C is independent of V_{CB}

→ The o/p curves are parallel to V_{CB} .

Three region in the output characteristics:

(i) Active Region:

E-B junction is forward biased

C-B junction is Reverse biased

$$\boxed{I_C \approx I_E}$$

I_C is Independent of V_{CB} .

(ii) Cut-off Region: The region below the curve $I_E = 0$ because of minority current flows i.e., $I_E = 0$ is known as ~~cut~~ cut-off Region.

→ E-B junction & C-B junction both are Reverse biased.

(iii) Saturation Region: It is the region to the left

of the $V_{CB} = 0$

→ I_C increases exponentially as V_{CB} increases towards

0 V.

$I_C \uparrow$ $V_{CB} \uparrow$ towards zero.

→ E-B & C-B junctions are forward bias.

Region	E-B junction	C-B junction	operation
Active Region	Forward bias	R. B	$I_C \approx I_E$
Cut-off Region	Reverse bias	R. B	$I_E = 0$
Saturation Region	forward bias	f. B	$I_C \uparrow$ $V_{CB} \uparrow$ to '0'

(ii) Common Emitter Configuration (CE):-

- In this configuration input is applied b/w base & emitter and output is taken from collector and emitter
- Emitter is common to both input & output circuits

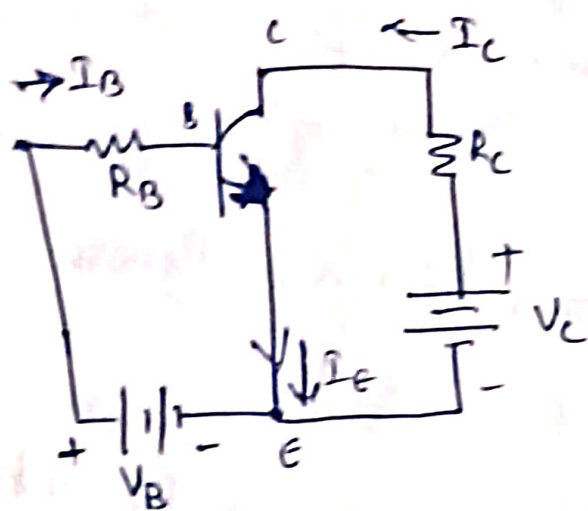
Base → i/p terminal

Collector → o/p "

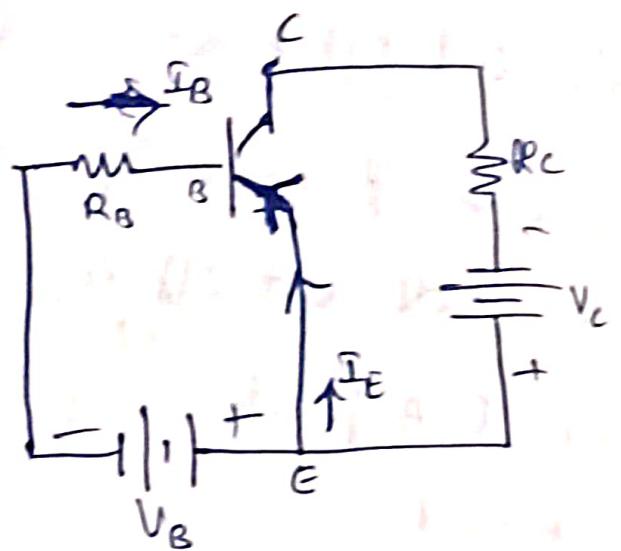
Emitter → common to i/p & o/p

E-B → F.B

C-B → R.B



(or)



Common emitter configuration
using NPN

Common emitter configuration
using PNP

Current amplification factor (β)

$$\beta = \frac{\Delta I_C}{\Delta I_B} ; \quad \beta = \frac{I_C}{I_B}$$

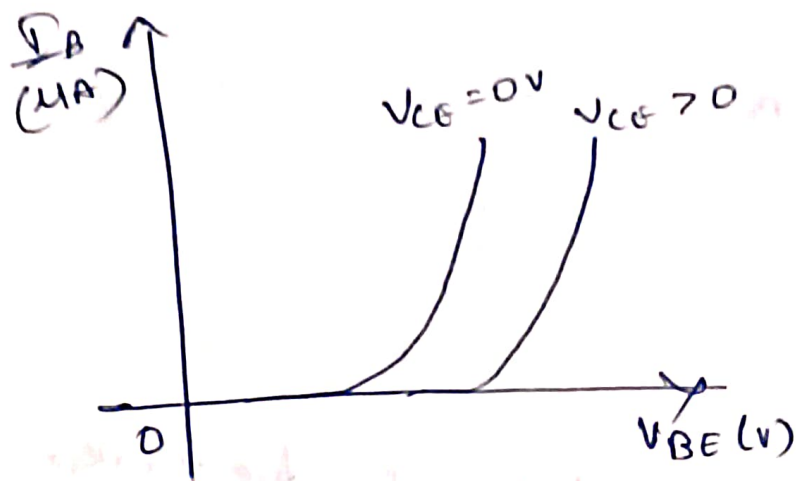
Expression for I_C is

$$I_C = \beta I_B + I_{CE0}$$

I_{CE0} → collector - emitter current with Base open.
($I_B = 0$)

Input characteristics of CE configuration:

→ It is the curve b/w i/p current I_B & i/p V_{BE} at constant o/p V_{CE}



when $V_{CE} = 0$, the E-B junction acts as a f.B. V_{CE} kept constant

→ I_B increases rapidly after the cut-in V_{BE} with small increment in V_{BE} .

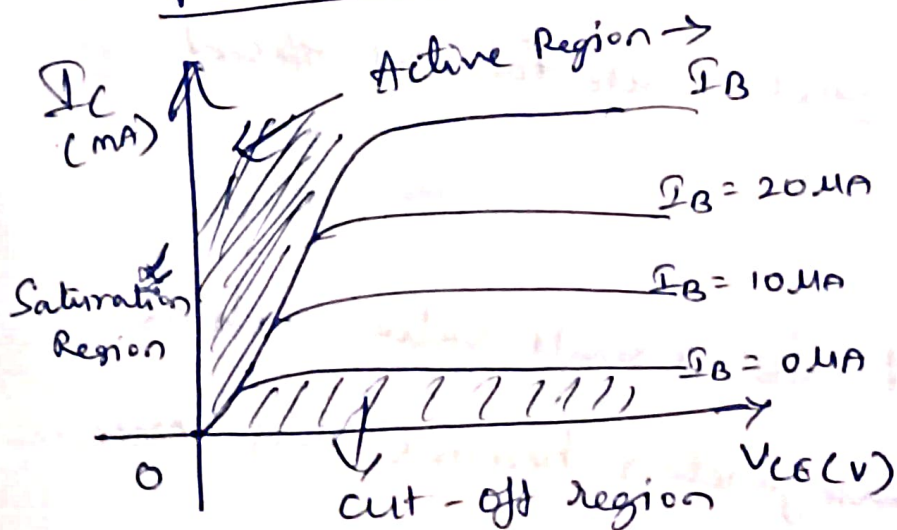
→ Input Resistance is very small.

→ when V_{CE} is $\uparrow$ ($V_{CE} > 0$), the $I_B \downarrow$ for the

same V_{BE}

→ the i/p curve shifts to the right as $V_{CE} \uparrow$.

output characteristics of CE configuration:



To determine the o/p characteristics

I_B is kept constant

" I_C vs V_{CE} " Small V_{CE} , $I_C \uparrow$ rapidly

(i) Active Region:

- Base-Emitter junction is forward biased
- collector-Emitter " is Reverse "

$$I_C > I_B$$

(ii) cut-off Region:

- The Region Below $I_B = 0$
- If $I_B = 0$, the o/p current is only due to the Reverse leakage current (I_{CE0})

B-E & C-E are in Reverse biased

∴ Transistor is in 'off' condition

- large current may damage transistor.

(iii) Saturation Region:

- B-E & C-B both junctions are forward biased

~~At $V_{CE} = 0$~~

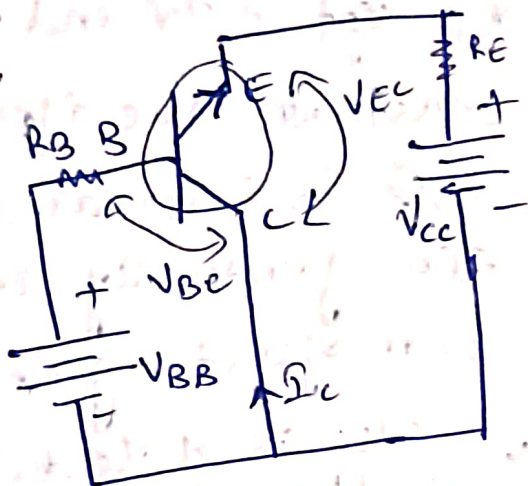
- If V_{CE} is reduced to a small value such as

0.2V then collector base junction becomes f.B hence

transistor goes to Saturation Region.

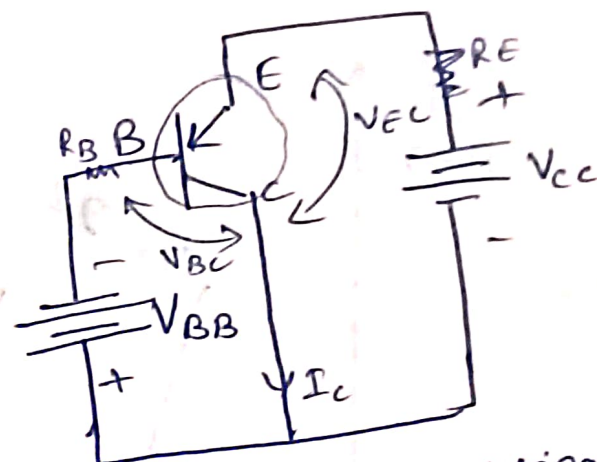
(iii) Common collector configuration :-

In this input is applied b/w base and collector and output taken from emitter & collector. collector is common for both input & output.



Common collector using NPN transistor

(or)



common collector using PNP transistor

Base - i/p terminal, (I_B)

Emitter - o/p "

collector - common to both i/p & o/p

→ B - c junction is f.B

→ E - c " " R.B

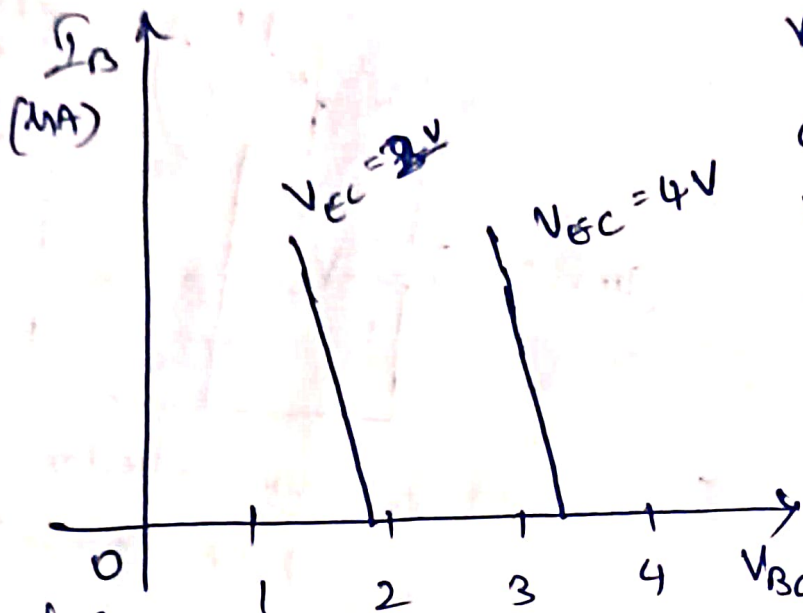
Current Amplification factor (β) :-

$$\beta = \frac{\text{o/p}}{\text{i/p}} \Rightarrow \frac{I_E}{I_B}$$

* Input characteristics

I/p parameters: Base current I_B &
Base-collector v/g (V_{BC})

I_B vs V_{BC} with constant V_{CE}



The output voltage V_{CE} kept at 2V and kept constant. The i/p voltage V_{BC} is increased from zero gradually and the corresponding i/p current

I_B is noted. Then V_{CE} the o/p voltage which is kept constant and o/p let's say 4V and kept $\rightarrow$ If the i/p v/g $\uparrow$'s, the base current (I_B) $\downarrow$'s

$$V_{BC} \uparrow \quad I_B \downarrow$$

$\rightarrow$ The V_{BC} is determined by the V_{CE} .

$\rightarrow$ i/p resistance is high.

constant and o/p voltage is gradually increases and i/p current noted. graph is shifted to right side.

* Output characteristics:

output parameters:-

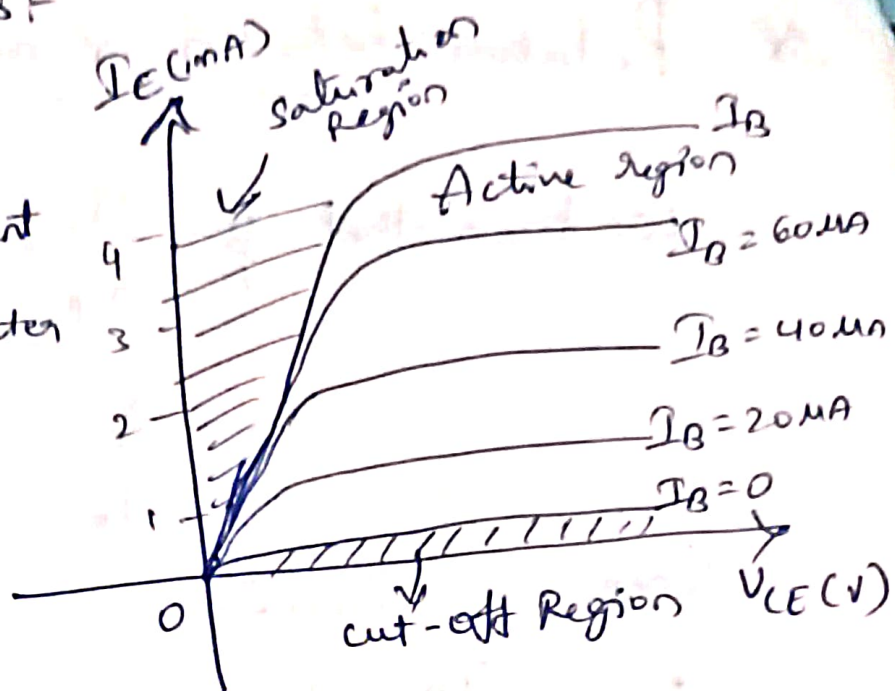
I_E - Emitter current

V_{CE} - Collector-Emitter voltage

I_E vs V_{CE}

I_B kept constant

To determine the o/p characteristics, I_B is kept constant.



* Active Region:

→ Base-collector is forward biased

→ Emitter-collector is Reverse biased

In this Region, the transistor is in ON condition i.e., working in the desired Q-point.

$$I_E = \beta I_B + \beta I_{C0}$$

* cut-off Region: Both junctions are R.B, $I_B = 0$

→ If $I_B = 0$ the o/p current is only due to the leakage current (I_{C0}) - negligibly small. $I_E \approx 0 \rightarrow$ Transistor is OFF

* Saturation Region: Both junctions are f.B

→ for small increment of V_{CE} 0 to 0.2 or 0.3 V, there is large change in I_E

→ If V_{CE} decreases, CE junction is forward biased.

* Relation between α and β :-

We know that $\beta = \frac{I_C}{I_B} \rightarrow (1)$

$$\alpha = \frac{I_C}{I_E} \rightarrow (2)$$

Since $I_E = I_B + I_C$

$$I_B = I_E - I_C$$

Sub I_B in eq (1)

$$\beta = \frac{I_C}{I_E - I_C}$$

divide denominator & numerator by I_E

$$\beta = \frac{\frac{I_C}{I_E}}{\frac{I_E}{I_E} - \frac{I_C}{I_E}} \Rightarrow \frac{I_C/I_E}{1 - \frac{I_C}{I_E}} \quad \left[\because \alpha = \frac{I_C}{I_E} \right]$$

$$\boxed{\beta = \frac{\alpha}{1 - \alpha}} \rightarrow (3)$$

Dividing the LHS/RHS side of eq'n (3) by $1 + \beta$

$$\frac{\beta}{1 + \beta} = \frac{\frac{\alpha}{1 - \alpha}}{1 + \beta} \Rightarrow \frac{\frac{\alpha}{1 - \alpha}}{1 + \frac{\alpha}{1 - \alpha}} \quad \left[\because \beta = \frac{\alpha}{1 - \alpha} \right]$$

$$\frac{\beta}{1 + \beta} = \frac{\frac{\alpha}{1 - \alpha}}{\frac{1 - \alpha + \alpha}{1 - \alpha}}, \Rightarrow \alpha = \frac{\beta}{1 + \beta}$$

~~also~~ $\therefore \boxed{\alpha = \frac{\beta}{1 + \beta}}$

Comparison of Common Base, Common Emitter, Common Collector.

Characteristics	Common Base	Common Emitter	Common - collector
Terms	Emitter - input Collector - o/p Base - common	Base - i/p, Collector - o/p Emitter - common	Base - i/p Emitter - o/p, collector - common collector - common
Circuit diagram			
Input current	I_E	I_B	I_B
Input v/g applied	Emitter & Base	Base & emitter	Base & collector
Output current	I_C	I_C	I_E
Output v/g applied	Collector & Base	collector & emitter	Emitter & collector
Current Amplification factor	$\alpha = I_C/I_E$	$\beta = I_C/I_B$	$\gamma = I_E/I_B$
O/p Resistance	Very high $1M\Omega$	high $40K\Omega$	low 50Ω
i/p Resistance	Very low 20Ω	low $1K\Omega$	high $500K\Omega$
Current gain	less than unity	High 20 to hundred	high 20 to hundreds
v/g gain	medium	Medium	low
Applications	As i/p stage of Amplifier	for audio signal Amplifier	for Impedance matching

Determination of h-parameters from transistor

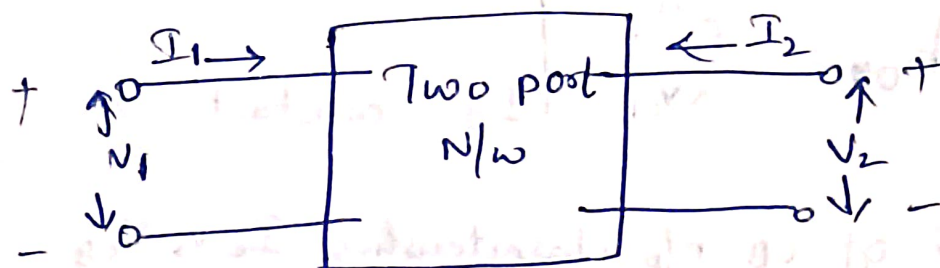
Characteristics:

→ H-parameters:

→ The four h-parameters - (hybrid parameters) of a transistor are a set of four values (h_{11} , h_{12} , h_{21} , & h_{22}) that describe its small-signal behaviour in a two-port network.

→ These are called 'Hybrid' because they combine different dimensions (Impedance, gain, admittance).

→ The parameters represent the transistor's input impedance (h_{11}), reverse voltage gain (h_{12}), forward current gain (h_{21}), and output admittance (h_{22}).



$h_{11} \rightarrow h_i$
 $h_{12} \rightarrow h_r$
 $h_{21} \rightarrow h_f$
 $h_{22} \rightarrow h_o$

$$V_1 = h_{11} I_1 + h_{12} V_2 \quad \text{--- (1)}$$

$$I_2 = h_{21} I_1 + h_{22} V_2 \quad \text{--- (2)}$$

$$h_i = h_{11} = \left. \frac{V_1}{I_1} \right|_{V_2=0} \Omega, \quad h_f = h_{21} = \left. \frac{I_2}{I_1} \right|_{V_2=0} \text{ No units}$$

$$h_r = h_{12} = \left. \frac{V_1}{V_2} \right|_{I_1=0} \text{ No units}, \quad h_o = h_{22} = \left. \frac{I_2}{V_2} \right|_{I_1=0} \frac{\text{mA}}{\text{V}}$$

$$h_i = h_{11} = \frac{V_1}{I_1} \bigg|_{V_2=0} \rightarrow \text{Input Impedance (with o/p shorted)}$$

$$h_f = h_{21} = \frac{I_2}{I_1} \bigg|_{V_2=0} \rightarrow \text{forward current gain (with o/p shorted)}$$

$$h_r = h_{12} = \frac{V_1}{V_2} \bigg|_{I_1=0} \rightarrow \text{Reverse v/g gain (with i/p open)}$$

$$h_o = h_{22} = \frac{I_2}{V_2} \bigg|_{I_1=0} \rightarrow \text{output admittance (with i/p open)}$$

$h_i \rightarrow$ It is the ratio of v/g to the current, has units of Ω

$h_o \rightarrow$ It is the ratio of ~~current~~ to the v/g, has units of $\frac{\text{mbos}}{(\text{or}) \text{ Siemens}}$

h_f and h_r being the ratio of similar quantities are pure numbers having no units.

$\rightarrow$ Thus the parameters are hybrid in nature.

$$V_1 = h_{11} I_1 + h_{12} V_2 \quad \text{--- (1)}$$

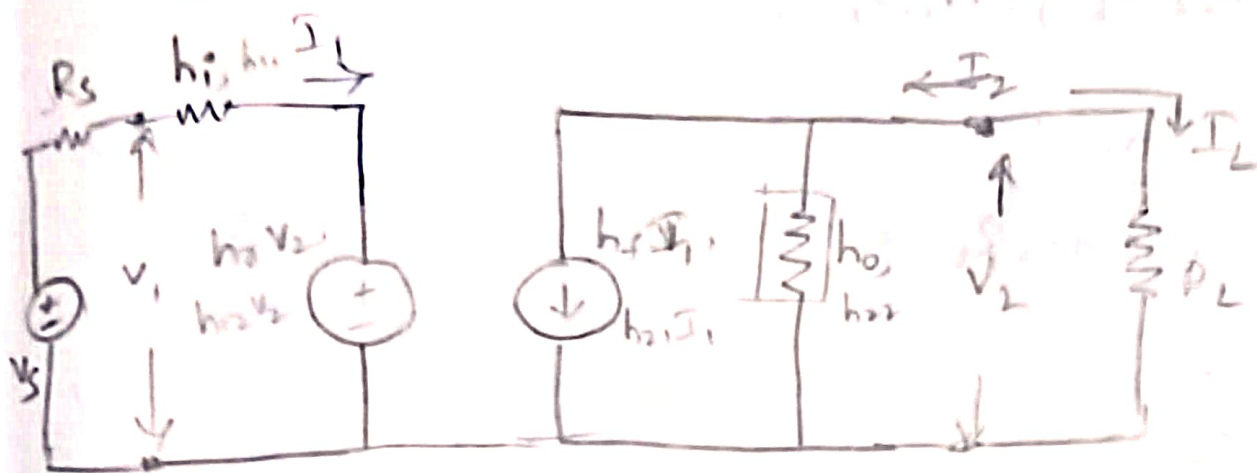
$$I_2 = h_{21} I_1 + h_{22} V_2 \quad \text{--- (2)}$$

we can write the eqⁿ's like

$$V_1 = h_i I_1 + h_r V_2 \quad \rightarrow \text{KVL}$$

$$I_2 = h_f I_1 + h_o V_2 \quad \rightarrow \text{KCL}$$

h-parameters equivalent circuit:



i/p side $\rightarrow$ KVL

o/p side $\rightarrow$ KCL

Here $V_2 = I_L R_L$, $\left[\because I_L = -I_2 \right]$

$V_2 = -I_2 R_L$

[direction is in opposite dir.]

we have to derive the equations for A_i , R_i , A_v , R_o

- ① current gain (A_i)
- ② Input Resistance (R_i)
- ③ Voltage gain (A_v)
- ④ output Resistance or output admittance.

① current Gain (A_i):

here $A_i = \frac{\text{output}}{\text{input}}$

$O/P = I_L$, $I/P = I_1$

$A_i = \frac{I_L}{I_1} \Rightarrow \frac{-I_2}{I_1}$

from eq ② $I_2 = h_{21}I_1 + h_{22}V_2$ $\because V_2 = -I_2 R_L$
from ckt

$I_2 = h_{21}I_1 - h_{22}I_2 R_L$

$I_2 + h_{22}I_2 R_L = h_{21}I_1$

$I_2[1 + h_{22}R_L] = h_{21}I_1$

$$I_2 [1 + h_{22} R_L] = h_{21} I_1$$

$$\frac{I_2}{I_1} = \frac{h_{21}}{(1 + h_{22} R_L)}$$

$$A_i = -\frac{I_2}{I_1}$$

$$A_i = -\left[\frac{h_{21}}{1 + h_{22} R_L} \right]$$

* * *

② $R_i \rightarrow$ Input Resistance $[R_{in}]$

$$R_{in} = \frac{V_1}{I_1}$$

$$\begin{aligned} [V &= IR] \\ [i.e. R &= \frac{V}{I}] \end{aligned}$$

R_{in} from eq ① $V_1 = h_{11} I_1 + h_{12} V_2$
 $\swarrow$ of h-parameter

$$R_i = \frac{h_{11} I_1 + h_{12} V_2}{I_1}$$

$$\Rightarrow \frac{h_{11} I_1}{I_1} + h_{12} \frac{V_2}{I_1}$$

$$R_i = h_{11} + h_{12} \left[\frac{V_2}{I_1} \right] \rightarrow \text{②}$$

from eq ② of h-parameters

$$I_2 = h_{21} I_1 + h_{22} V_2 \rightarrow \text{③}$$

we want $\frac{V_2}{I_1}$ value so ~~in eq ③~~ V_2 value from A_i

$$I_2 = h_{21} I_1 + h_{22} V_2 \rightarrow \text{eq (2) from h-parameter}$$

$$\therefore V_2 = -I_2 R_L$$

$$\boxed{I_2 = -\frac{V_2}{R_L}} \rightarrow \text{sub in eq (2) of h-parameter}$$

$$-\frac{V_2}{R_L} = h_{21} I_1 + h_{22} V_2$$

$$-\frac{V_2}{R_L} - h_{22} V_2 = h_{21} I_1$$

$$-V_2 \left[\frac{1}{R_L} + h_{22} \right] = h_{21} I_1$$

$$\boxed{\frac{V_2}{I_1} = -\frac{h_{21}}{\frac{1}{R_L} + h_{22}}}$$

$$R_i = h_{11} + h_{12} \frac{V_2}{I_1}$$

$$\text{Sub } \frac{V_2}{I_1} \text{ in } R_i$$

$$R_i = h_{11} + h_{12} \left[\frac{-h_{21}}{\frac{1}{R_L} + h_{22}} \right]$$

$$R_i = h_{11} - \frac{h_{12} \cdot h_{21}}{\frac{1}{R_L} + h_{22}}$$

$$\boxed{R_i = h_{11} - \frac{h_{12} \cdot h_{21}}{\frac{1}{R_L} + h_{22}}}$$

③ (A_v) voltage gain:

$$A_v = \frac{V_2}{V_1}$$

we know $R_i = \frac{V_1}{I_1}$

$$V_1 = R_i I_1$$

$$A_v = \frac{V_2}{R_i I_1} = \frac{1}{R_i} \cdot \frac{V_2}{I_1}$$

$$A_v = \frac{1}{R_i} \cdot \left(\frac{-h_{21}}{\frac{1}{R_L} + h_{22}} \right) \quad \left[\because \frac{V_2}{I_1} = \frac{-h_{21}}{\frac{1}{R_L} + h_{22}} \right]$$

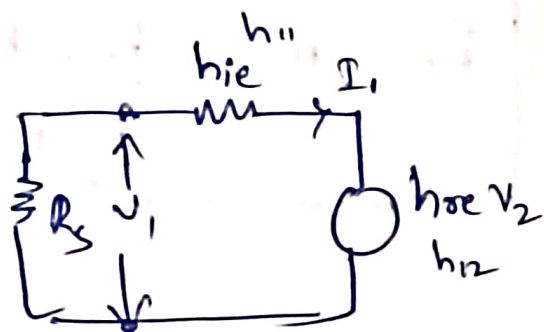
$$A_v = \frac{-h_{21}}{R_i \left[\frac{1}{R_L} + h_{22} \right]}$$

④ (R_o) output Resistance or output Admittance:

$$R_o = \frac{1}{Y_o}$$

$$\text{So } Y_o = \frac{I_2}{V_2} \Big|_{V_s = 0}$$

$$\therefore I_2 = h_{21} I_1 + h_{22} V_2$$



Divide by v_2

$$\frac{I_2}{v_2} = h_{21} \frac{I_1}{v_2} + h_{22} \frac{v_2}{v_2}$$

$$y_o = \frac{I_2}{v_2} = h_{21} \left[\frac{I_1}{v_2} \right] + h_{22} \frac{v_2}{v_2}$$

$$I_1 (h_{11} + R_s) + h_{12} v_2 = 0 \quad \text{from ckt}$$

$$I_1 (h_{11} + R_s) = -h_{12} v_2$$

$$\frac{I_1}{v_2} = \frac{-h_{12}}{(h_{11} + R_s)}$$

→ sub in $\frac{I_2}{v_2} = y_o$

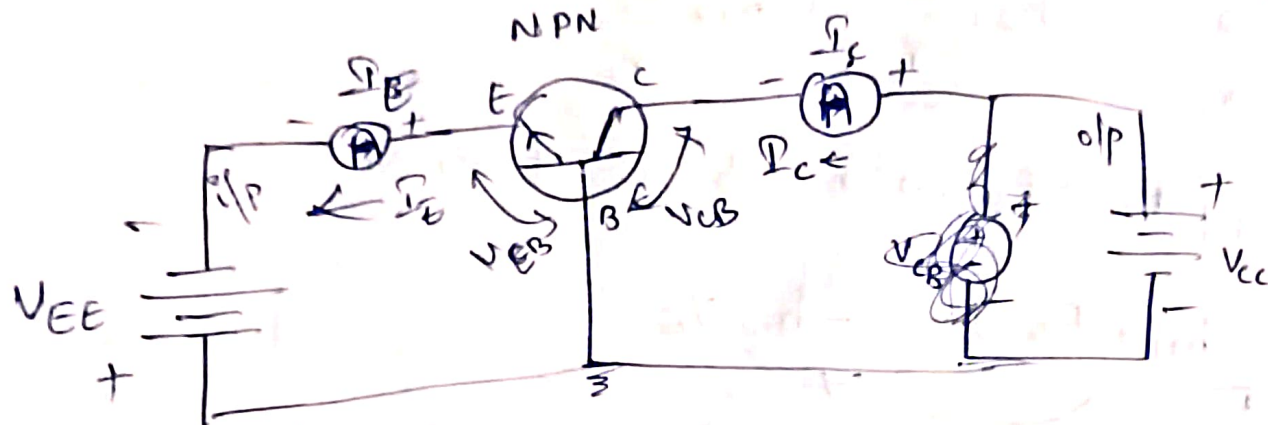
$$y_o = \frac{I_2}{v_2} = h_{21} \left[\frac{-h_{12}}{h_{11} + R_s} \right] + h_{22}$$

$$y_o = h_{22} - \frac{h_{21} \cdot h_{12}}{h_{11} + R_s}$$

→ h-parameters in BJT configurations CB, CE, CC:

h-parameters in CB configuration:

Common-Base



(h_{ib})
① Input Impedance: The ratio of the change in

i/p v/g (ΔV_{EB}) to the change in i/p current (ΔI_E)

$$h_{ib} = \left. \frac{\Delta V_{EB}}{\Delta I_E} \right|_{V_{CB} - \text{constant}}$$

$$[h_i = h_{in} = \frac{V_i}{I_i}]$$

② forward current gain (h_{fe}):

→ The ratio of the change in the o/p collector current (ΔI_C) to the corresponding change in the (i/p) ^{Emitter} ~~base~~ current (ΔI_E) keeping the (o/p) collector ^{Base} ~~emitter~~ v/g V_{CB} at constant

$$h_{fb} = \left. \frac{\Delta I_C}{\Delta I_E} \right|_{V_{CB} - \text{constant}} \quad [h_f = h_{21} = \frac{I_2}{I_1}]$$

③ Reverse v/g gain: (h_{rb}):

→ The ratio of the change in the i/p ~~Base~~ ^{Emitter-Base} v/g (ΔV_{EB}) to the corresponding change in the o/p collector - emitter v/g, at a constant value of i/p current I_E .

$$h_{rb} = \frac{\Delta V_{EB}}{\Delta V_{CB}} \Big|_{I_E - \text{constant}} \left[h_{rb} = h_{12} = \frac{V_1}{V_2} \right]$$

④ output Impedance

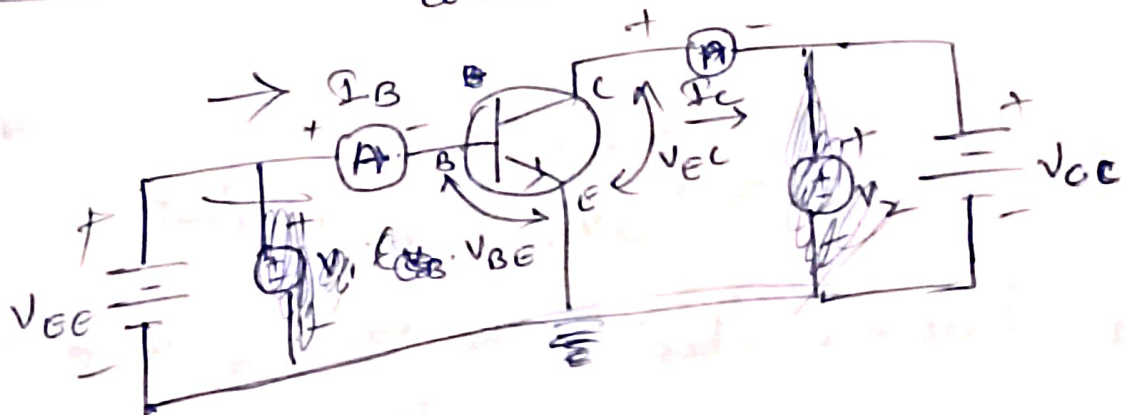
④ output Admittance: (h_{ob}):

The ratio of change in collector current (ΔI_C) to the change in collector - base v/g (ΔV_{CB}) at constant Emitter current (I_E).

$$h_{ob} = \frac{\Delta I_C}{\Delta V_{CB}} \Big|_{I_E - \text{constant}}$$

$$h_o = h_{22} = \frac{I_2}{V_2}$$

→ h-parameters in CE configuration
 Common-Emitter



⑤

* Input Impedance: (h_{ie}):

→ The ratio of change in base-emitter v/g ΔV_{BE} to the change in base current (ΔI_B). & V_{CE} is constant.

$$h_{ie} = \frac{\Delta V_{BE}}{\Delta I_B} \bigg|_{V_{CE} - \text{constant}} \quad \left[h_{ie} = h_{11} = \frac{V_1}{I_1} \right]$$

* Forward current Gain: (h_{fe})

→ The ratio of change in o/p collector current (ΔI_C) to the change in i/p base-current (ΔI_B) & V_{CE} is constant

$$h_{fe} = \frac{\Delta I_C}{\Delta I_B} \bigg|_{V_{CE} - \text{constant}} \quad \left[h_{fe} = h_{21} = \frac{I_2}{I_1} \right]$$

* Reverse v/g gain: (h_{re}):

→ The ratio of the change in i/p Base-emitter v/g to the change in the o/p collector-emitter v/g at a constant

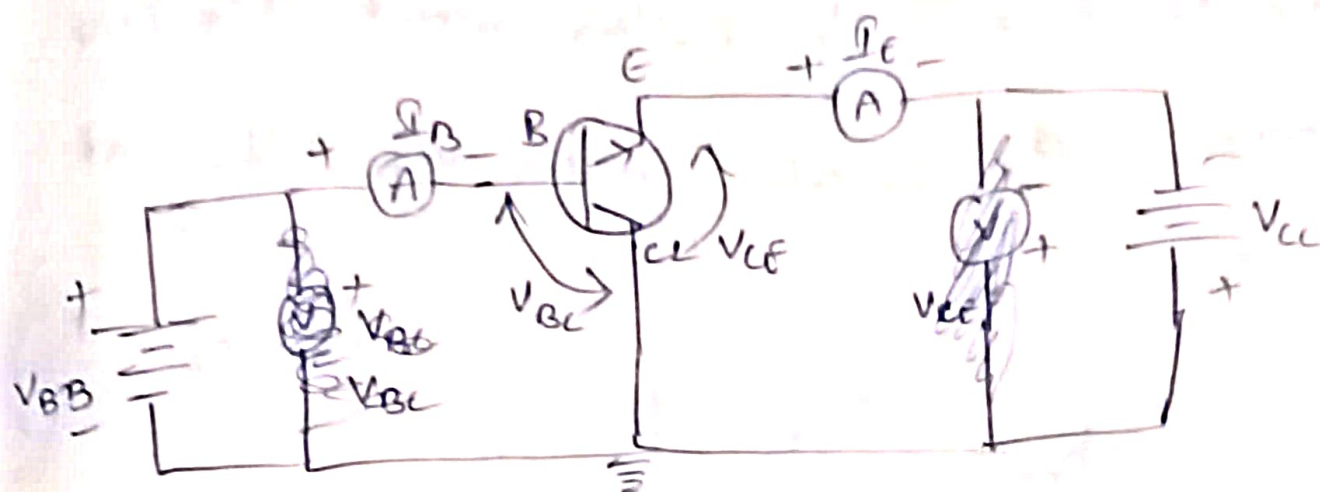
I_B .

$$h_{re} = \frac{\Delta V_{BE}}{\Delta V_{CE}} \bigg|_{I_B - \text{constant}} \quad \left[h_{re} = h_{12} = \frac{V_1}{V_2} \right]$$

* Output Admittance: (h_{oe}): The ratio of change in collector current ΔI_C to the change in the collector-emitter v/g (ΔV_{CE}) with constant I_B

$$h_{oe} = \frac{\Delta I_C}{\Delta V_{CE}} \bigg|_{I_B - \text{constant}} \quad \left[h_o = h_{22} = \frac{I_2}{V_2} \right]$$

* h -parameter in c.c.c. configuration
 ↓
 common-collector



* Input Impedance (h_{ic}):-

The ratio of change in Base-collector v/g ΔV_{BC} to the change in Base current (ΔI_B) & V_{CE} is constant.

$$h_{ic} = \left. \frac{\Delta V_{BC}}{\Delta I_B} \right|_{V_{CE} - \text{constant}} \quad \left[h_i = h_{11} = \frac{V_1}{I_1} \right]$$

* Forward Current Gain (h_{fc}):- The ratio of change in o/p Emitter current ΔI_E to the change in i/p Base-collector current ΔI_B , at a constant V_{CE}

$$h_{fc} = \left. \frac{\Delta I_E}{\Delta I_B} \right|_{V_{CE} - \text{constant}} \quad \left[h_f = h_{21} = \frac{I_2}{I_1} \right]$$

* Reverse v/g gain (h_{rc}):-

The ratio of change in i/p Base-collector v/g ΔV_{BC} to the change in the o/p Emitter-collector v/g ΔV_{CE} at a constant I_B constant

$$h_{rc} = \left. \frac{\Delta V_{BC}}{\Delta V_{CE}} \right|_{I_B - \text{constant}} \quad \left[h_r = h_{12} = \frac{V_1}{V_2} \right]$$

→ output admittance (h_{oc}):

The ratio of change in o/p emitter current (ΔI_E) to the change in o/p collector-emitter v/g ΔV_{CE} , at I_B - constant

$$h_{oc} = \frac{\Delta I_E}{\Delta V_{CE}} \bigg|_{I_B - \text{constant}}$$

$$\left[h_o = h_{22} = \frac{I_L}{V_L} \right]$$

UNIT - III

* BJT BIASING *

BJT Biasing (or) Transistor Biasing:-

→ The process of providing proper supply voltages and resistance for obtaining the desired Q-point is called biasing.

→ The transistor can be operated in three regions cut-off region, Active Region, & saturation Region, by applying proper biasing conditions.

Need for Biasing and stabilization:-

→ To maintain operating point stable we have to supply external dc voltages of correct polarity & magnitude to the two junctions of the transistor to operate in desired region.

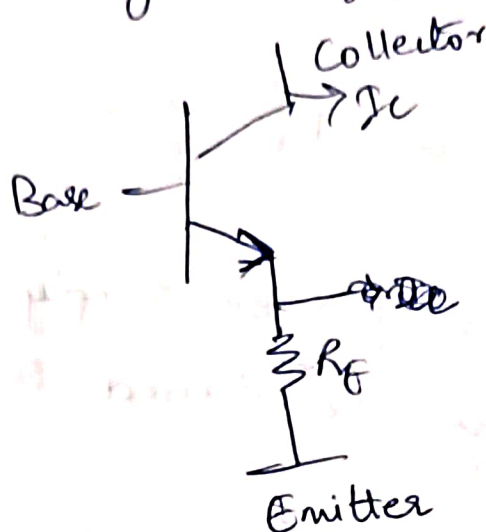
→ The transistor must be in the active Region to act as an amplifier.

→ To ensure faithful Amplification to set the Operating Point (Q-point) it fixes the correct collector current (I_C) & collector-emitter v/g (V_{CE}).

→ Without proper bias, the o/p signal gets distorted.

→ To avoid transistor cut-off or saturation region

the transistor always in the active region for the full input signal swing.



Need for Stabilization:-

→ It means keeping the operating point constant, even when conditions change.

① Temperature changes:-

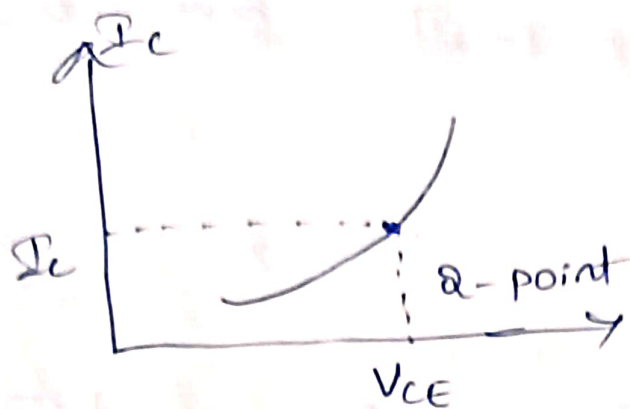
→ As temperature increases, transistor current tends to increase, leading to distortion or damage.

② Variations in transistor parameters:-

Each transistor (even of same type) may have different current gain (β), which affects current.

③ Power supply variations:-

Changes in supply voltage can shift the operating point.



~~Stability~~

stabilization factor (S) :-

→ In CE transistor circuit, the output current is

$$I_c = \beta I_B + (1 + \beta) I_{co}$$

I_B , β , I_{co} are temperature dependent.

The extent to which the I_c is stabilized with varying I_{co} (β & V_{BE}) is measured by a stability factor.

$$S \rightarrow \frac{\partial I_c}{\partial I_{co}} \bigg|_{V_{BE}, \beta}$$

$$S_{V_{BE}} = S' \rightarrow \frac{\partial I_c}{\partial V_{BE}} \bigg|_{I_{co}, \beta}$$

$$S_{\beta} = S'' \rightarrow \frac{\partial I_c}{\partial \beta} \bigg|_{I_{co}, V_{BE}}$$

→ Definition of stability factor (S) :-

→ It is defined as the ratio of change of collector current (I_c) with respect to the leakage current (I_{co}) keeping V_{BE} & β as constant.

$$S = \frac{\partial I_c}{\partial I_{co}} \bigg|_{\beta \text{ \& \& } V_{BE} \text{ as constant}}$$

→ 'S' factor should be small to have better thermal stability.

Derivation:

For a CE amplifier, the collector current (I_c) is given as,

$$I_c = \beta I_B + (1 + \beta) I_{C0} \quad \text{--- (1)}$$

Differentiating eqn, (1) w.r.t I_c

$$\frac{\frac{dI_c}{dI_c}}{\frac{dI_c}{dI_c}} = \beta \frac{dI_B}{dI_c} + (1 + \beta) \frac{dI_{C0}}{dI_c}$$

$$1 = \beta \frac{dI_B}{dI_c} + (1 + \beta) \frac{dI_{C0}}{dI_c}$$

$$\left[S = \frac{\partial I_c}{\partial I_{C0}} \right]$$

$$(1 + \beta) \frac{dI_{C0}}{dI_c} = 1 - \beta \frac{dI_B}{dI_c}$$

$$\frac{dI_{C0}}{dI_c} = \frac{1 - \beta \left(\frac{dI_B}{dI_c} \right)}{1 + \beta} \quad \left[\right.$$

Here we want to get " $\left(\frac{dI_c}{dI_{C0}} \right)$ " for that we can take the Reciprocal term

$$S = \frac{dI_c}{dI_{C0}} = \frac{1 + \beta}{1 - \beta \left(\frac{dI_B}{dI_c} \right)}$$

's' should be small as ~~possible~~ possible to have better stability.

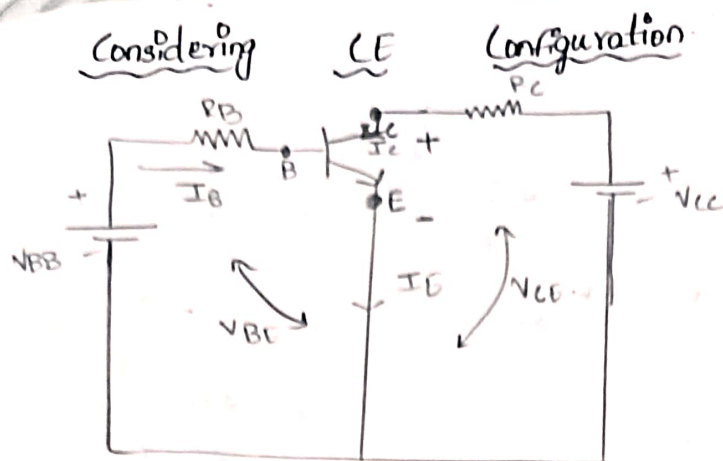
stability factor S' & S''

$$S' = \frac{\partial I_C}{\partial V_{BE}} \approx \frac{\Delta I_C}{\Delta V_{BE}} \bigg|_{I_B \text{ \& } \beta \text{ constant}}$$

$$S'' = \frac{\partial I_C}{\partial \beta} \approx \frac{\Delta I_C}{\Delta \beta} \bigg|_{I_B \text{ \& } V_{BE} \text{ constant}}$$

→ Load line and operating point:

- The Load line is a straight line drawn on a Transistor characteristics curves which represents all possible dc output conditions [Combination of voltage and current] for a given circuit.
- The Operating Point or Q-point is the specific point where the load line intersects the transistor characteristics curve for a particular bias condition. This Q-point represents the dc values of voltage and current when no AC signal is applied, and it is the stable operating state around which any signal variations will occur.



→ The Transistor is a two-port device we have 2 operating points, Input operating point and output operating point. We can define Input operating point as the co-ordinates of plane by the Intersection of Load line with Input characteristics and then we will draw the load line and the point of Intersection between the load line and Input characteristics for particular Output Voltage will give us Input operating point.

Apply the KVL across the Input loop

$$V_{BB} - I_B R_B - V_{BE} = 0$$

→ $V_{BE} = 0$. (To get point of Y-axis ; X-axis = 0)

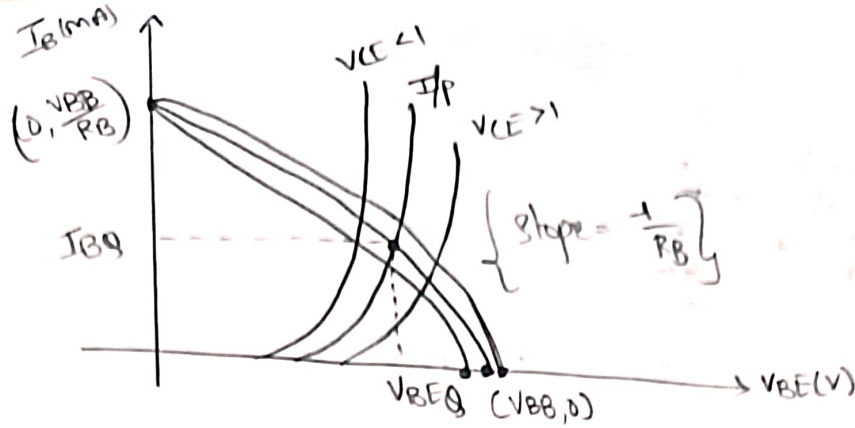
$$V_{BB} - I_B R_B = 0$$

$$\boxed{I_B = \frac{V_{BB}}{R_B}} ; \text{Point}(P_1) = \left[0, \frac{V_{BB}}{R_B} \right].$$

→ $I_B = 0$ (To get point on X-axis, Y-axis = 0)

$$\boxed{V_{BB} = V_{BE}}$$

$$P_2 = [V_{BB}, 0].$$



operating point depends on R_B value. As R_B increases slope of load line decreases.

→ Output operating point.

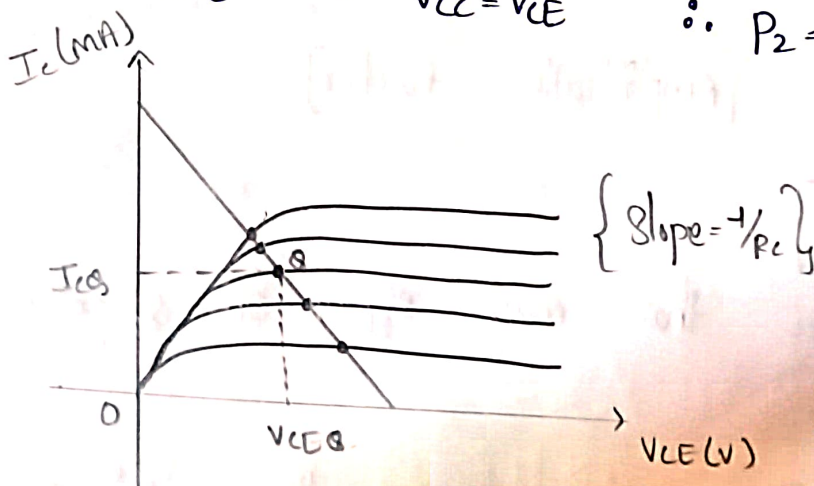
→ output operating point is intersection of load line with transistor output characteristics for particular value of Base current I_B , gives the operating point.

Apply KVL across output loop

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$V_{CE} = 0 \Rightarrow I_C = \frac{V_{CC}}{R_C} \quad \therefore P_1 = \left[0, \frac{V_{CC}}{R_C} \right]$$

$$I_C = 0 \Rightarrow V_{CC} = V_{CE} \quad \therefore P_2 = [V_{CC}, 0]$$

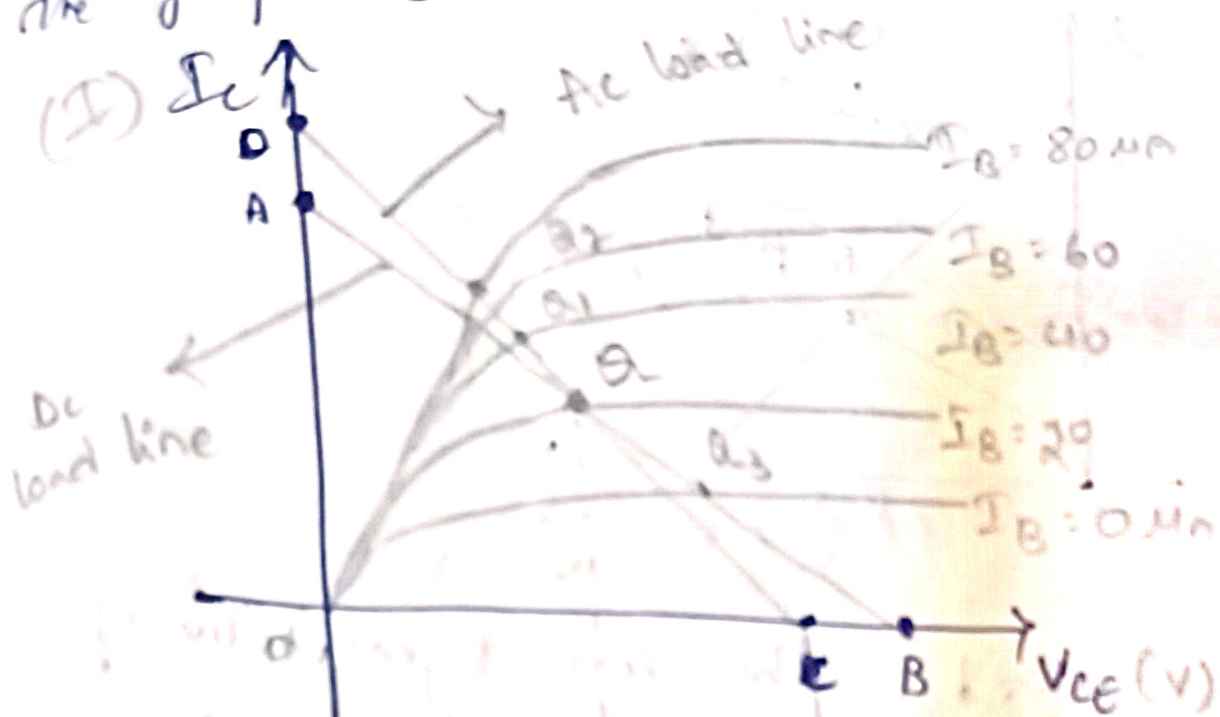


→ Always choose operating point in the middle of the load line or in the Active Region for pure Amplification.

→ If the operating point is near to cut off region the positive portion of wave form is clipped (from below fig.)

output stage of the common emitter amplifier

By combining the AC load line & DC load line the graph is shown below.



Here,

AB - DC load line

CD - AC load line

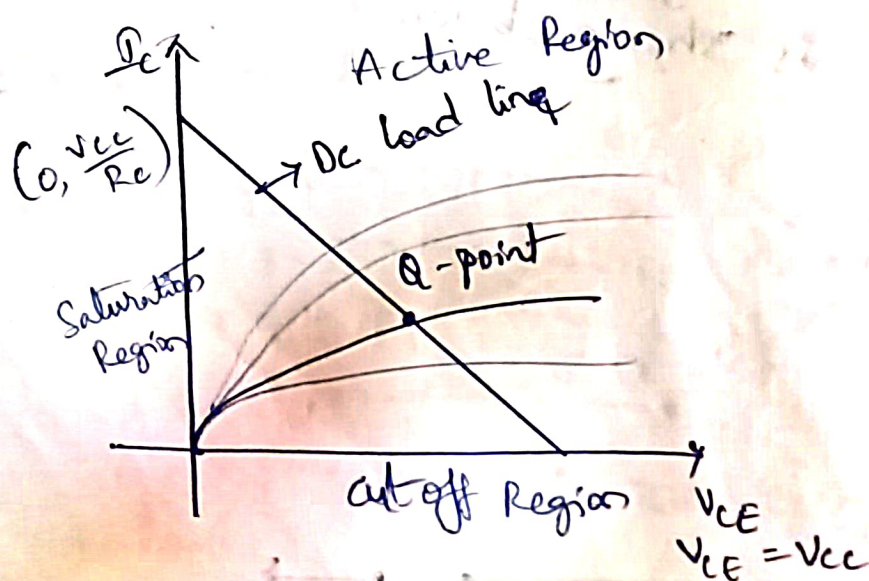
→ It is steeper than DC load line due to loading and capacitor.

* Operating point (or) Q-point (or) Quiescent point:

→ It is the specific point where the transistor can be operated efficiently to get the maximum output.

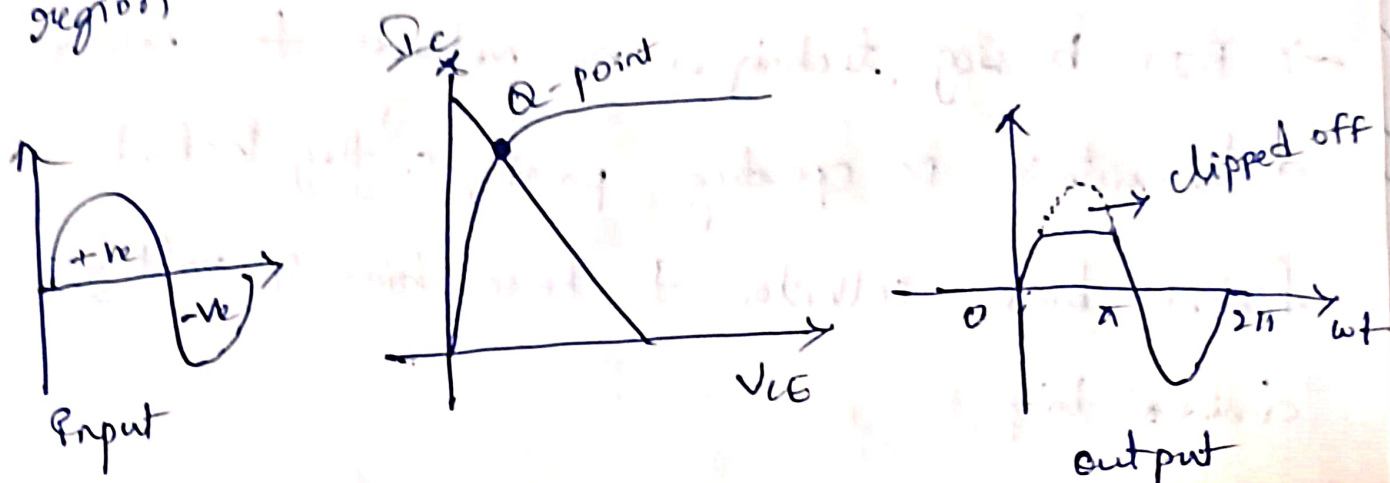
→ The operating point is fixed in the active region for ensuring the proper operation of the transistor as an Amplifier.

→ It is defined as the point at which output characteristics & DC load line intersect each other is called operating point.

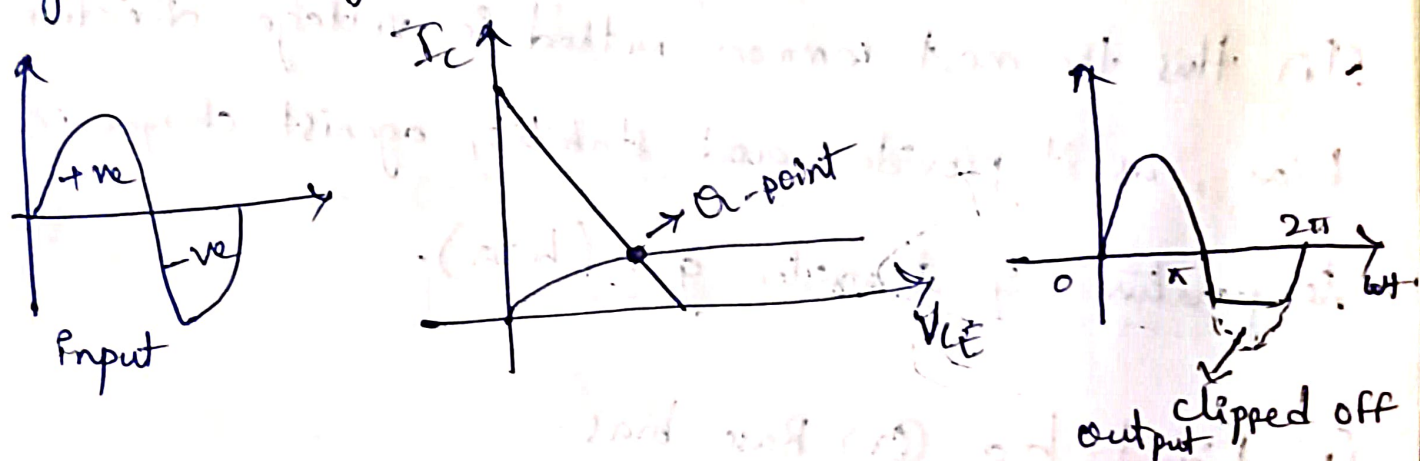


→ It is also defined as the zero signal value of collector current (I_C) & collector to emitter v/g (V_{CE}) are known as operating point (or) Q-point

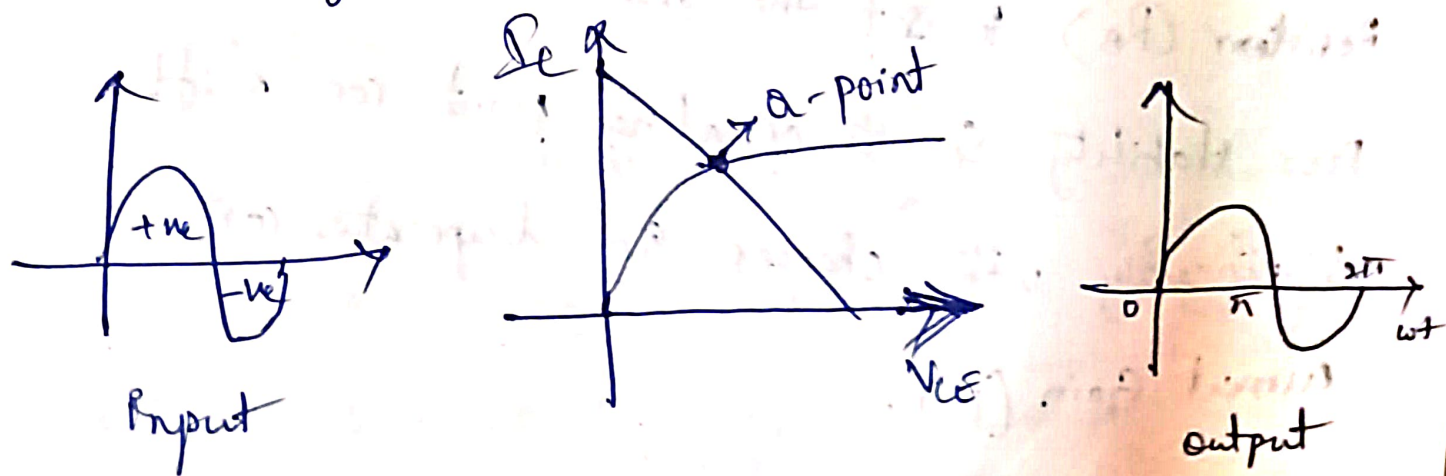
Case i) If operating point is chosen near saturation region then positive peak is 'clipped off'.



Case ii) If operating point is chosen near the cut-off region then negative peak is 'clipped off'.



Case iii) If operating point is chosen near the Active Region then the wave form is not clipped.



* Biasing Techniques of BJT

→ BJT biasing techniques are methods for setting a transistor's DC operating point, & they include fixed bias, collector to base bias & voltage divider bias.

→ Fixed bias

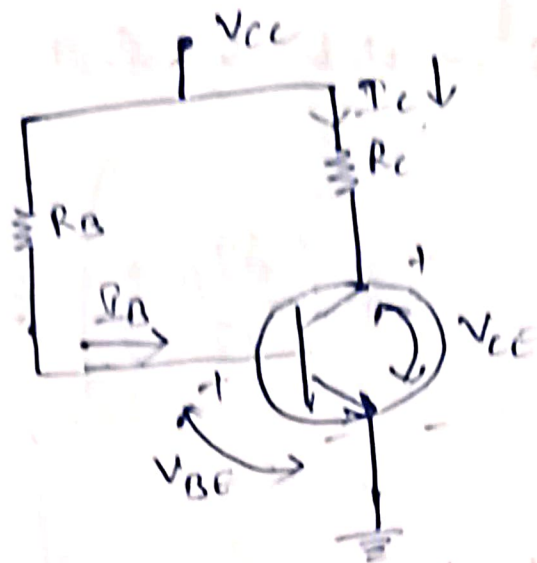
→ collector to base bias

→ voltage divider bias.

IN this the most common method is voltage divider bias, as it provides good stability against changes in temperature & transistor gain (β).

① Fixed bias (or) Base bias

This is the simplest method using a single Resistor (R_B) to set the base current. However it has poor stability & its operating point can shift significantly with changes in temperature (or) current Gain (β).



Apply KVL to the base circuit (i/p) we get

$$V_{CC} = I_B R_B + V_{BE}$$

$$V_{CC} - V_{BE} = I_B R_B$$

$$\therefore \boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B}}$$

Apply KVL to collector circuit (o/p) we get

$$V_{CC} = I_C R_C + V_{CE}$$

$$V_{CC} - V_{CE} = I_C R_C$$

$$\therefore \boxed{I_C = \frac{V_{CC} - V_{CE}}{R_C}}$$

Stability factor 'S' for fixed bias:-

consider eqⁿ

$$V_{CC} = I_B R_B + V_{BE} \Rightarrow \boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B}} \quad \text{--- (1)}$$

~~differentiate w.r.to I_C then we get~~

Base current I_B is $\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B}} \quad \text{--- (1)}$

The formula of 'S' - stability factor

$$S = \frac{1 + \beta}{1 - \beta \left(\frac{\partial I_B}{\partial I_C} \right)} \quad \text{--- (2)}$$

Differentiating (1) wrt to I_C

$$\frac{\partial I_B}{\partial I_C} = \frac{d}{dI_C} \left[\frac{V_{CC} - V_{BE}}{R_B} \right] \quad \text{--- (3)} \quad \left[I_B \rightarrow \text{constant} \right]$$

Ques here $\frac{\partial I_B}{\partial I_C} = 0 \rightarrow$ sub in (2)

$$S = \frac{1 + \beta}{1 - \beta(0)}$$

$$S = 1 + \beta$$

If I_{C0} increases, I_C increases $(1 + \beta)$ times.



Advantages

- It is simple to shift the operating point anywhere in the active region by changing Base resistor (R_B)
- A very small number of components are required.

Disadvantage

- It has very poor thermal stability.
- The collector current I_C depends directly on β , which is not constant from transistor to transistor.
- As Temp $\uparrow$, collector current $\uparrow$, causing more heat which again $\uparrow$ current.
This can damage the transistor.

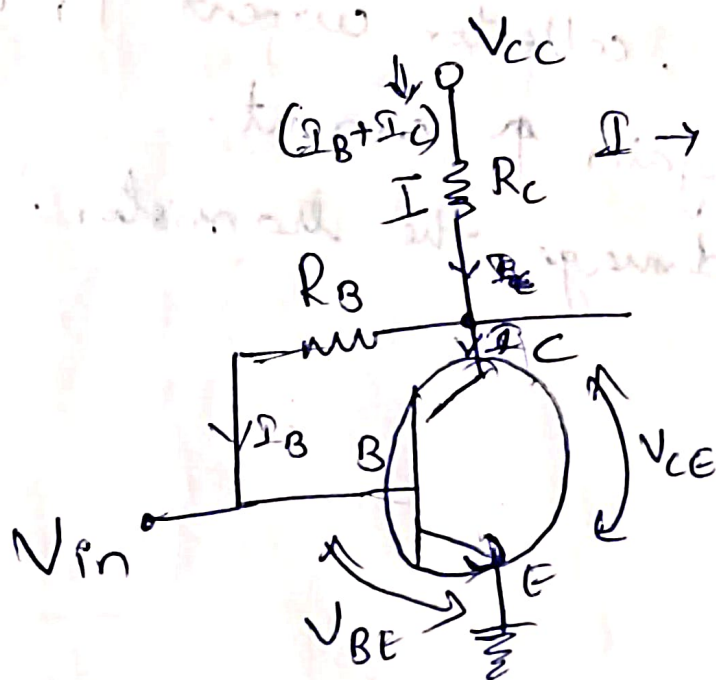
② Collector to base bias:

→ The base resistor is connected from the collector to the base, with the base bias V_B derived from the collector V_C .

→ It provides improved stability compared to fixed bias because it is less sensitive to β changes but less commonly used compared to V_{CC} divider bias.

This is also known as collector feed back bias (or)

Base Bias with collector feed back.



$I \rightarrow$ Total current

$$[I = I_B + I_C]$$

$$[\therefore \beta = \frac{I_C}{I_B}]$$

$$[I_C = \beta I_B]$$

Current Gain

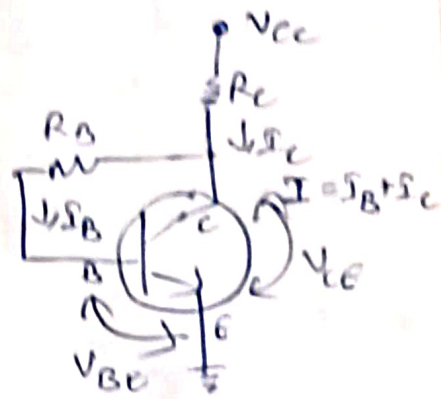
$$\beta = \frac{I_C}{I_B} ; I_C = \beta I_B$$

Apply KVL to circuit (i/p) i.e. Base-emitter

$$V_{CC} = I R_C + I_B R_B + V_{BE}$$

$$V_{CC} \Rightarrow (I_B + I_C) R_C + I_B R_B + V_{BE}$$

$$V_{CC} \Rightarrow I_B R_C + I_C R_C + I_B R_B + V_{BE}$$



$$V_{CC} = I_B (R_C + R_B) + I_C R_C + V_{BE}$$

$$I_B (R_C + R_B) = V_{CC} - I_C R_C - V_{BE}$$

$$I_B = \frac{V_{CC} - I_C R_C - V_{BE}}{R_C + R_B} \quad \text{--- (1)}$$

Differentiate (1) w.r.t I_C

$$\frac{dI_B}{dI_C} = \frac{d}{dI_C} \left[\frac{V_{CC} - I_C R_C - V_{BE}}{R_C + R_B} \right]$$

$$\frac{dI_B}{dI_C} \Rightarrow \frac{0 - R_C - 0}{R_C + R_B}$$

$$\boxed{\frac{dI_B}{dI_C} = \frac{-R_C}{R_C + R_B}} \quad \text{--- (2)}$$

Substitute eq (2) in the stability factor 'S'

$$S = \frac{1 + \beta}{1 - \beta \left(\frac{dI_B}{dI_C} \right)} \quad \text{--- (3)}$$

Sub (2) in (3)

$$S = \frac{1 + \beta}{1 - \beta \left(\frac{\partial I_B}{\partial I_C} \right)}$$

$$S = \frac{1 + \beta}{1 - \beta \left(\frac{-R_C}{R_C + R_B} \right)}$$

$$S = \frac{1 + \beta}{1 + \beta \left(\frac{R_C}{R_C + R_B} \right)}$$

Apply KVL across (o/p) collector

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

$$I_C = \frac{V_{CC} - V_{CE}}{R_C + R_E}$$

If Temperature changes β is also change which result collector current is also changes as a result voltage drop across R_C ↑'s.

Advantages:-

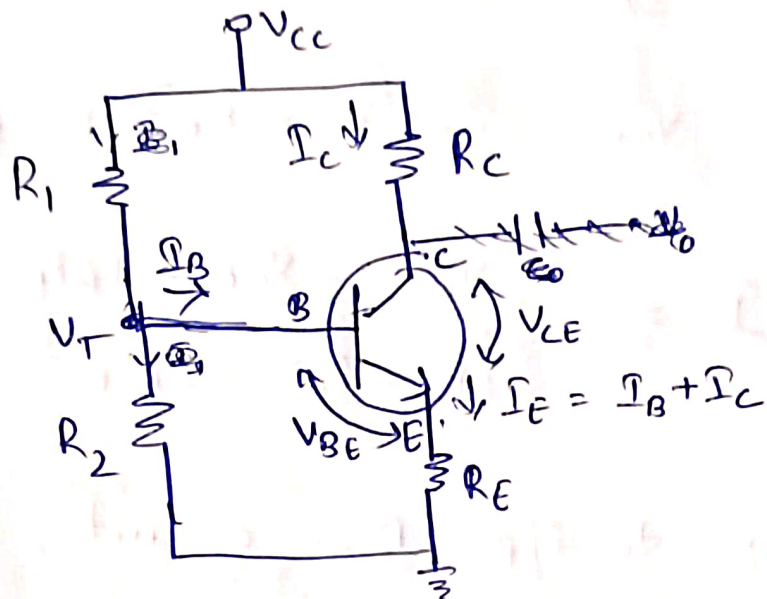
- It is very simple circuit
- It provides Better stability than fixed bias.

Disadvantages:-

- If R_C is very small, $S = 1 + \beta$
 - poor stability
- The value of R_C must be quite large for better Stabilization.
- This circuit provides -ve feedback & reduces the gain.

* Voltage Divider Bias (or) Self Bias (or) Potential divider Bias

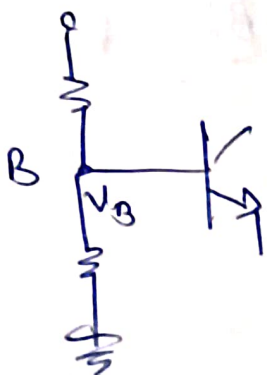
- It provides good stability of the operating point.
- It includes two resistors R_1 & R_2 forming a voltage divider across the supply voltage V_{CC} .



- The v/g drop across R_2 f.B the Base- Emitter junction
- The v/g drop across R_E r.B the Emitter junction.
- Self Bias is used as a constant current source.

→ let us consider Thevenin's Equivalent circuit

$$\text{i.e., } R_B = R_1 \parallel R_2 = \frac{R_1 \cdot R_2}{R_1 + R_2}$$



$$V_B = \frac{R_2}{R_1 + R_2} \cdot V_{CC}$$

$$R_B = \frac{R_1 R_2}{R_1 + R_2}$$

Apply KVL to o/p (Base)(collector) circuit

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$V_{CC} - V_{CE} = I_C R_C + I_E R_E$$

$$\Rightarrow I_C R_C + (I_C + I_B) R_E$$

$$\Rightarrow I_C R_C + I_C R_E + I_B R_E$$

$$V_{CC} - V_{CE} = I_C [R_C + R_E] + I_B R_E$$

$$I_C = \frac{V_{CC} - V_{CE} - I_B R_E}{(R_C + R_E) + I_B R_E}$$

Apply KVL to i/p (Base circuit)

$$V_T = I_B R_B + V_{BE} + I_E R_E$$

$$V_T = I_B R_B + V_{BE} + (I_B + I_C) R_E$$

$$V_T = I_B R_B + V_{BE} + (I_B + I_C) R_E$$

$$V_T = I_B R_B + V_{BE} + I_B R_E + I_C R_E$$

Differentiate w.r.t I_C we get

$$0 = \frac{\partial I_B}{\partial I_C} R_B + \frac{\partial I_B}{\partial I_C} R_E + \frac{\partial I_C}{\partial I_C} R_E$$

$$\therefore \frac{\partial I_B}{\partial I_C} R_B + \frac{\partial I_B}{\partial I_C} R_E + R_E$$

Q

$$\frac{\partial \beta}{\partial \beta_c} (R_B + R_E) = -R_E$$

$$\boxed{\frac{\partial \beta}{\partial \beta_c} = \frac{-R_E}{R_B + R_E}} \quad \text{--- (1)}$$

Sub in 's'

Stability factor 's'

$$s = \frac{1 + \beta}{1 - \beta \left(\frac{\partial \beta}{\partial \beta_c} \right)}$$

$$s = \frac{1 + \beta}{1 - \beta \left(\frac{-R_E}{R_B + R_E} \right)}$$

$$s = \frac{1 + \beta}{1 + \beta \left(\frac{R_E}{R_B + R_E} \right)}$$

$\frac{R_E}{R_B + R_E} \ll 1$, so neglect $\frac{R_E}{R_B + R_E}$

$$s = \frac{1 + \cancel{\beta}}{1 + \beta}$$

$$\boxed{s = 1}$$

Advantages:-

- It provides better stability than other biasing methods
- It is Independent of β

Disadvantages:-

- It uses no. of components more
- Design is slightly complex.

* Thermal Runaway Process:-

→ Definition:-

Thermal runaway is a cumulative process of self-heating of a transistor which will damage it due to excessive self-heating.

- When a transistor gets hot, its current increases.
- But when current increases, it becomes even hotter.

In Common Emitter circuit

The collector current ' I_c ' is given as

$$I_c = \beta I_B + (1 + \beta) I_{co}$$

Here, Thermal runaway is self increasing cycle of heat & current in a transistor that can lead to its destruction.

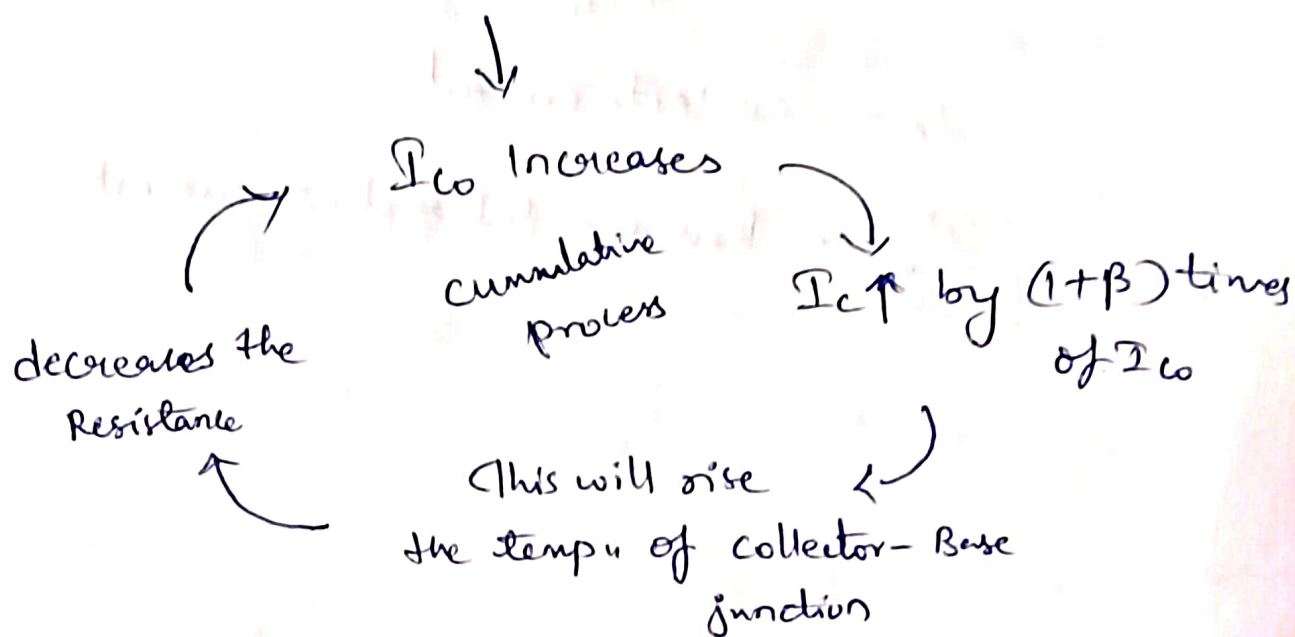
where $\beta \rightarrow$ current gain

$I_B \rightarrow$ Base current

$I_{CO} \rightarrow$ reverse leakage current.

Here
 β , I_B and I_{CO} are temperature dependent
i.e., β , I_B & I_{CO} increases as the temperature increases.
 I_{CO} doubles for every 10°C rise in temperature.

If Temperature Increases



→ As a result, I_C ↑'s further cumulatively to burnout the transistor.

→ This effect of an unstabilized transistor due to self-heating process is known as thermal runaway.

How to prevent thermal runaway:

→ use -ve feed back like emitter and resistor.

→ use v/g divider bias provides better thermal stability

- use heat sink: to improve heat dissipation
- Heat sink: It is used in power transistor.
- use constant current source: It limits the current through the transistor.

Thermal stability factor:

$$S = \frac{\partial I_c}{\partial I_{co}}$$

$I_c \rightarrow$ collector current

$I_{co} \rightarrow$ Reverse saturation current.

UNIT - IV

TRANSISTOR AMPLIFIERS

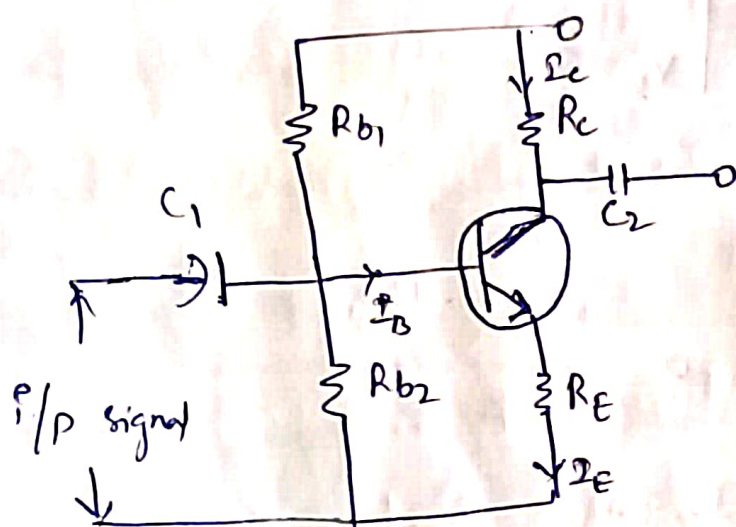
Transistor Amplifier

- Transistors can act as an amplifiers while they are functioning in the active Region.
- When we want to increase or amplify the input signal, A transistor can take in a very small weak signal through the base junction & release the amplified signal through the collector.
- It is used in RF (Radio frequency), OFC (Optic fibre communication), audio Amplification etc.

* Transistor as a small-signal Amplifier:

- When a signal level is too small (like, microphone, antenna, etc), the signal must be amplified to a desired level.
- A transistor acts as a small signal Amplifier by increasing the amplitude of weak input signals applied at its base, resulting in a larger output signal at its collector.
- This function is widely used in radios, audio Equipments & many electronic devices.

Amplification is known as the process of converting the relatively weaker signal to a stronger signal is called Amplification.



$C_1 \rightarrow$ i/p coupling Capacitor

$C_2 \rightarrow$ o/p coupling Capacitor

$R_{b1}, R_{b2} -$ v/g divider bias Resistors

$R_C \rightarrow$ Collector Resistor

$R_E \rightarrow$ Emitter Resistor

$\rightarrow R_{b1}$ & R_{b2} form a v/g divider to keep the transistor in the active region

$\rightarrow R_E$ provides thermal stability

$\rightarrow C_1$ allows AC i/p to reach the base but blocks DC

$\rightarrow C_2$ passes Amplified AC o/p while blocking DC components

$\rightarrow$ The i/p signal produces a small variation in base current I_B

$$\text{Since } I_C = \beta I_B$$

Even a small change in I_B causes a large change in collector current I_C .

→ this varying I_c flows through R_c , creating a much larger change in o/p voltage.

$$V_{out} = V_{cc} - I_c R_c$$

→ The CE amplifier gives a 180° phase shift b/w input & output.

for small signals, v/g Gain

$$A_v \approx \frac{R_c}{R_E}$$

Advantages:-

- High voltage Gain
- Simple circuit
- widely used in audio & RF amplifiers.

Disadvantages:-

- The v/g Gain is not very high (or) limited Gain
- Temperature is sensitive
- It requires proper Biasing.

* h-parameters Equivalent circuit:

→ This is known as hybrid parameters & have a different dimensions [Impedance, Gain, Admittance].

→ The parameters represents the ① Input Impedance (h_{11})

& (h_i), ① Input Impedance (h_{11}) - h_i

② ^{Reverse} Voltage Gain (h_{12}) - h_R

③ forward current Gain - (h_{21}) - h_f

④ output admittance (h_{22}) - h_o

$$\therefore \begin{aligned} h_{11} &= h_i \\ h_{12} &= h_R \\ h_{21} &= h_f \\ h_{22} &= h_o \end{aligned}$$

$$V_i = f_1(I_i, V_o)$$

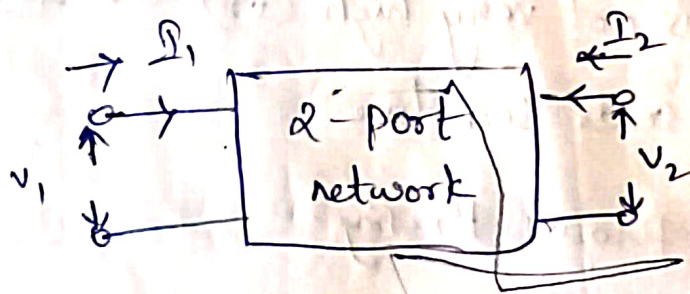
$$I_o = f_2(I_i, V_o)$$

V_i of $I_o \rightarrow$ Dependent variables
 I_i of $V_o \rightarrow$ Independent variables

Case (i), when $V_2 = 0$

$$h_{11} = \frac{V_1}{I_1} \Big|_{V_2=0}$$

$$h_{21} = \frac{I_2}{I_1} \Big|_{V_2=0}$$



$$V_1 = h_{11} I_1 + h_{12} V_2$$

$$I_2 = h_{21} I_1 + h_{22} V_2$$

we can write this

$$V_1 = h_i I_1 + h_R V_2$$

$$I_2 = h_f I_1 + h_o V_2$$

Case (ii) when $I_1 = 0$

$$h_{12} = \frac{V_1}{V_2} \Big|_{I_1=0}$$

$$h_{22} = \frac{I_2}{V_2} \Big|_{I_1=0}$$

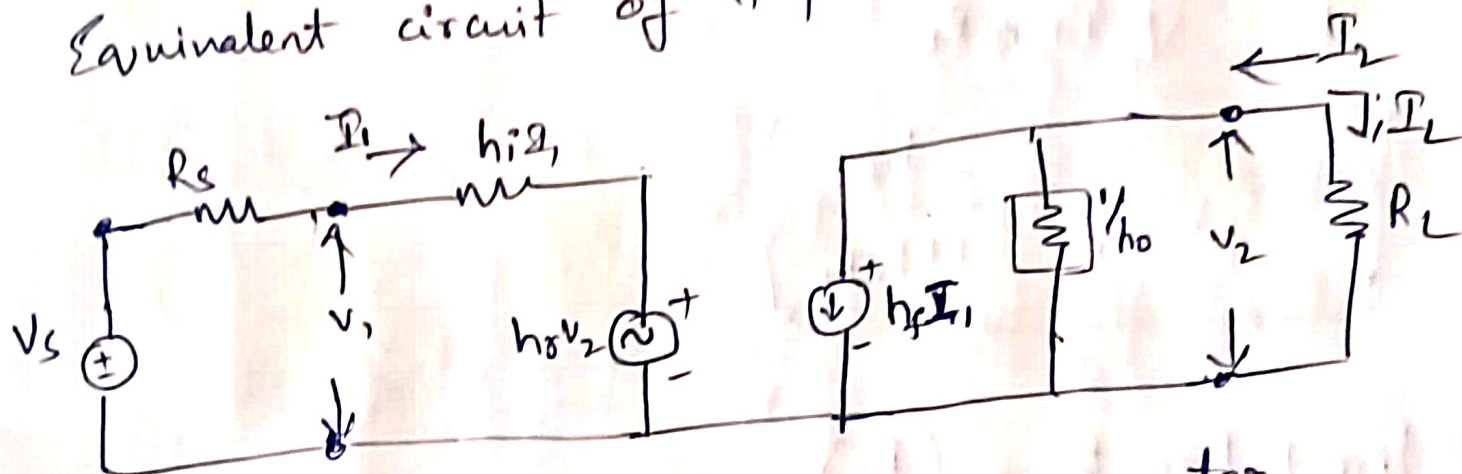
$$\text{So, } h_i = \frac{V_1}{I_1}, \quad h_f = \frac{I_2}{I_1}$$

$$h_R = \frac{V_1}{V_2}, \quad h_o = \frac{I_2}{V_2}$$

$$\text{So } V_1 = h_i I_1 + h_o V_2 \quad \text{--- (1)}$$

$$I_2 = h_f I_1 + h_o V_2 \quad \text{--- (2)}$$

Here by using both the equations we can draw the Equivalent circuit of H-parameter.



Equivalent circuit of H-parameter.

Here $V_2 = I_L R_L$ [$I_L = -I_2$] $\rightarrow$ direction is in opposite direction

$$\text{So, } \boxed{V_2 = -I_2 R_L}$$

we have to derive the equation for A_i , R_i , A_v , R_o

(1) Current Gain (A_i) (2) Input Resistance (R_i)

(3) Voltage Gain (A_v) (4) Output Resistance (R_o)

(1) Current Gain (A_i) : This is the ratio of output current to input current $A_i = \frac{o/p}{i/p}$

$$A_i = \frac{I_2}{I_1} \Rightarrow \therefore I_2 = -I_1 \quad \left\{ \begin{array}{l} V_1 = h_i I_1 + h_o V_2 \quad \text{--- (1)} \\ I_2 = h_f I_1 + h_o V_2 \quad \text{--- (2)} \end{array} \right.$$

$$A_i = \frac{-I_2}{I_1}$$

So from eq (2) $I_2 = h_f I_1 + h_o V_2$ $\therefore V_2 = \frac{I_2}{h_o}$

$$I_2 = h_f I_1 - h_o I_2 R_L$$

$$I_2 + h_o I_2 R_L = h_f I_1$$

$$I_2 [1 + h_o R_L] = h_f I_1$$

$$\frac{I_2}{I_1} = \frac{h_f}{1 + h_o R_L}$$

$$A_{i^*} = \frac{-I_2}{I_1} = \frac{-h_f}{1 + h_o R_L}$$

② Input Resistance (R_i)

$$R_i = \frac{V_1}{I_1} \quad \left[\because V_2 = 0 \right]$$

$$\left[R = \frac{V}{I} \right]$$

Eqn's of h-parameter

$$V_1 = h_i I_1 + h_o V_2 \quad \text{--- (1)}$$

$$I_2 = h_f I_1 + h_o V_2 \quad \text{--- (2)}$$

from eqn (1) $V_1 = h_i I_1 + h_o V_2$

~~Divide eqn (1) by I_1~~
 ~~$R_i = \frac{V_1}{I_1} = \frac{h_i I_1 + h_o V_2}{I_1}$~~
 $\frac{V_1}{I_1} = \frac{h_i I_1}{I_1} + h_o \frac{V_2}{I_1}$
 $\underbrace{\frac{V_1}{I_1}}_{R_i} = h_i + h_o \frac{V_2}{I_1}$

$$R_i = h_i + h_o \frac{V_2}{I_1} \quad \text{--- (3)}$$

$$\left[\because V_2 = -\frac{I_2 R_L}{1} \right]$$

$$I_2 = -\frac{V_2}{R_L}$$

eqn (2) $I_2 = h_f I_1 + h_o V_2$

$$-\frac{V_2}{R_L} = h_f I_1 + h_o V_2$$

$$-\frac{V_2}{R_L} - h_o V_2 = h_f I_1$$

$$-V_2 \left[\frac{1}{R_L} + h_o \right] = h_f I_1$$

$$\frac{V_2}{I_1} = \frac{-h_f}{\frac{1}{R_L} + h_o}$$

$$\frac{V_2}{I_1} = \frac{-h_f}{\frac{1}{R_L} + h_o} \rightarrow \text{sub in eq (3)}$$

$$\text{Now } \rightarrow R_i = h_i + h_r \frac{V_2}{I_1} - \text{ i.e., (3)}$$

$$R_i = h_i + h_r \left[\frac{-h_f}{\frac{1}{R_L} + h_o} \right]$$

$$\boxed{R_i = h_i - \frac{h_r \cdot h_f}{\frac{1}{R_L} + h_o}}$$

(3) voltage Gain (A_v):-

$$A_v = \frac{V_2}{V_1}$$

$$\text{we know } R_i = \frac{V_1}{I_1}$$

$$V_1 = R_i I_1 \rightarrow \text{sub in 'A}_v\text{'}$$

$$A_v = \frac{V_2}{R_i I_1} = \frac{1}{R_i} \left(\frac{V_2}{I_1} \right)$$

$$A_v = \frac{1}{R_i} \left[\frac{-h_f}{\frac{1}{R_L} + h_o} \right]$$

$$\left[\because \frac{V_2}{I_1} = \frac{-h_f}{\frac{1}{R_L} + h_o} \right]$$

↓
(This is from R_i)

$$A_v = \frac{-h_f}{R_i \left[\frac{1}{R_L} + h_o \right]}$$

④ output Admittance (R_o):-

$$R_o = \frac{1}{Y_o}$$

$$Y_o = \frac{I_2}{V_2} \Big|_{V_s=0}$$

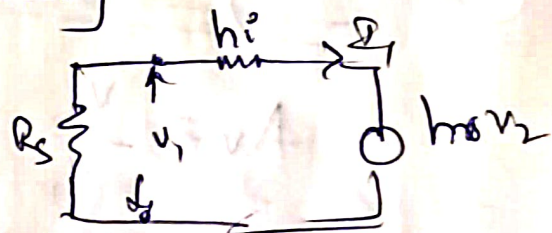
from eq(2) $I_2 = h_f I_1 + h_o V_2$

Divide by ' V_2 ' $\Rightarrow \frac{I_2}{V_2} = h_f \frac{I_1}{V_2} + h_o \frac{V_2}{V_2}$

$$Y_o = \frac{I_2}{V_2} = h_f \frac{I_1}{V_2} + h_o$$

$$I_1 (h_i + R_s) + h_r V_2 = 0 \quad [\text{from ckt}]$$

$$I_1 (h_i + R_s) - h_r V_2$$



$$\frac{I_1}{V_2} = \frac{-h_r}{h_i + R_s}$$

$$Y_o = \frac{I_2}{V_2} = h_f \left(\frac{-h_r}{h_i + R_s} \right) + h_o$$

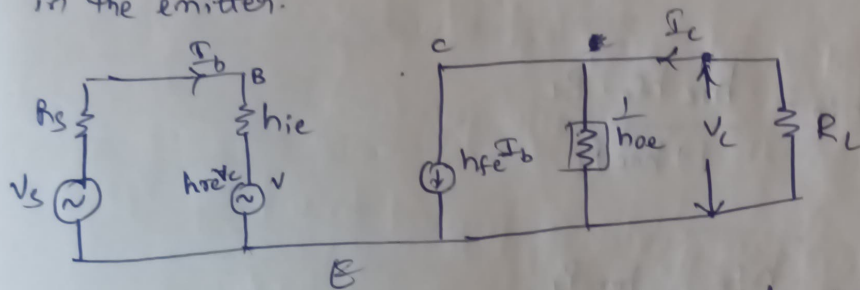
$$Y_o = h_o - \frac{h_f h_r}{h_i + R_s}$$

* CE, CB, CC Amplifier Analysis using H-parameters:

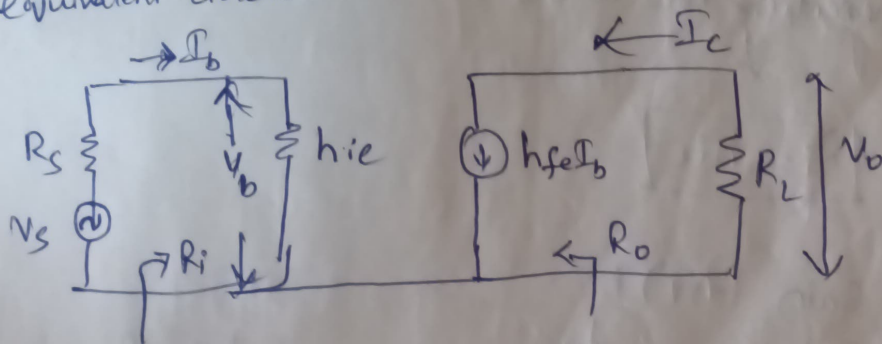
① Analysis of common - Emitter Amplifier using H-parameters:

→ Since $\frac{1}{h_{oe}}$ is in parallel with R_L & R_C if

$\frac{1}{h_{oe}} \gg R_L \parallel R_C$ then h_{oe} may be neglected, if we neglect h_{oe} , the collector current I_C is given by $I_C = h_{fe} I_b$, under the conditions the magnitude of the v/g of the generator in the emitter.

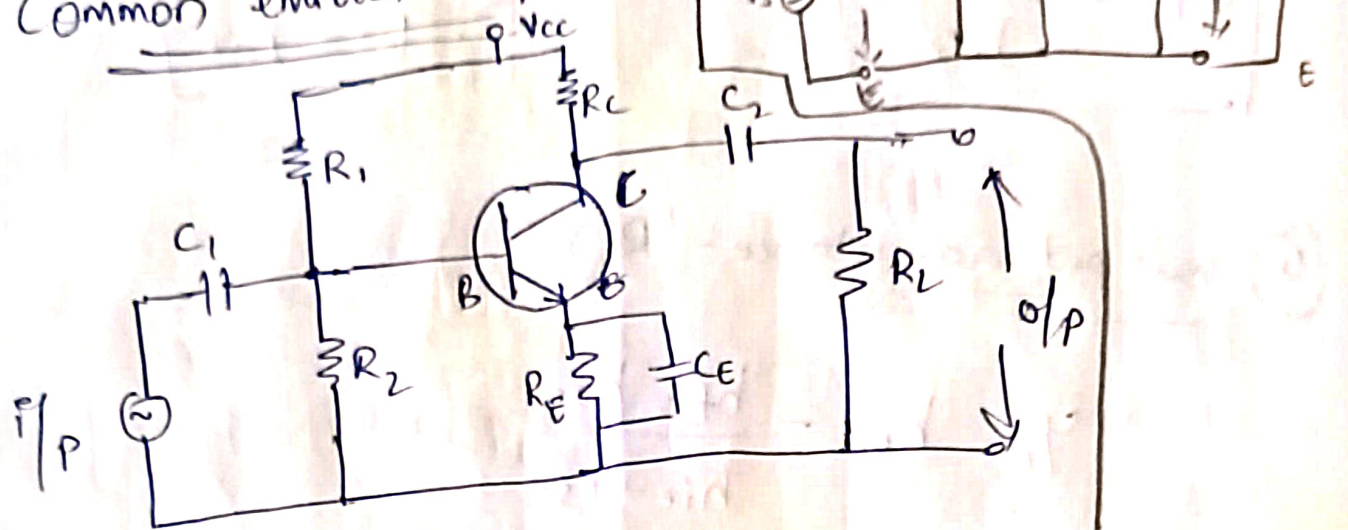


Since $h_{re} h_{fe} = 0.01$ this v/g may be neglected in comparison with the $h_{ie} I_b$ drop across h_{ie} , If the load Resistance $R_L \parallel R_C$ is small it is possible to neglect the parameters h_{re} & h_{oe} in the h-parameter equivalent circuit.



* CE, CB, CC Amplifier Analysis using H-parameter :-

① Common emitter Amplifier :-



→ The input signal is applied b/w base-emitter & o/p is taken from the collector base junction.

→ The emitter-base junction is forward biased by V_{BE} & collector-base junction is reverse Biased by V_{CC} .

→ when positive half of the signal is applied, the v_{be} b/w base & emitter (V_{be}) is increased because it is already positive with respect to ground.

→ So, forward bias is increased, i.e., the base current is increased.

→ Due to transistor action, the collector current I_C is increased β times.

→ when this current flows through R_C , the drop $I_C R_C$ increases considerably. As the consequence of this, the v_{ce} b/w collector and emitter (V_{ce}) decreases.

→ In this way amplified v_{ce} appears across R_C .

→

→ It is also obvious from the circuit that the positive going input-signal appears as a negative going o/p signal i.e. there is a phase shift of 180° between input and output.

① A_i (Current Gain) :-

→ Here $A_i = \frac{-I_2}{I_1} = \frac{-h_f}{1 + h_o R_L}$

This is from H-parameter derivation

$$A_{ie} = \frac{-h_{fe}}{1 + h_{oe} R_L}$$

[Note: E represents Emitter]

② Input Resistance (R_i)

$$R_i = h_{ie} - \frac{h_{fe} \cdot h_{oe} R_L}{1 + h_{oe} R_L}$$

$$R_{ie} = h_{ie} - \frac{h_{oe} \cdot h_{fe}}{\frac{1}{R_L} + h_{oe}}$$

$$R_{ie} = h_{ie} - \frac{h_{oe} \cdot h_{fe}}{\frac{1 + h_{oe} R_L}{R_L}}$$

$$R_{ie} = h_{ie} - \frac{h_{fe} \cdot h_{oe} \cdot R_L}{1 + h_{oe} R_L}$$

[E - represents Emitter]

(iii) (3) Voltage Gain (A_v) :-

$$A_v = \frac{-h_f}{R_i \left[\frac{1}{R_L} + h_o \right]}$$

[E] represents emitter

$$A_{ve} = \frac{-h_{fe}}{R_{ie} \left[\frac{1}{R_L} + h_{oe} \right]}$$

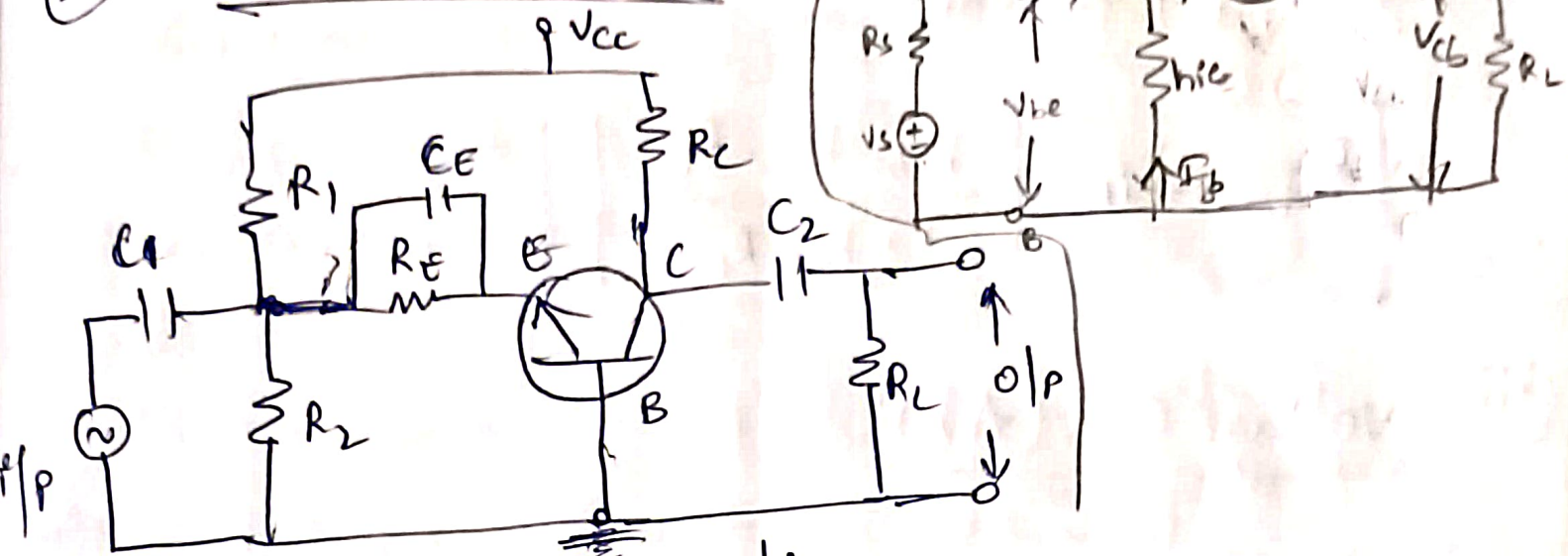
(4) Output Resistance (R_o) :-

$$R_o = h_o - \frac{h_f \cdot h_r}{h_i + R_s}$$

[E - represents emitter]

$$R_{oe} = h_{oe} - \frac{h_{fe} \cdot h_{re}}{h_{ie} + R_s}$$

② Common Base Amplifier:



Common Base Amplifier

- The input signal is applied b/w Emitter base, while the output is taken from collector Base junction.
- E-B junction is f.B, V_{EE} , & C-B is $R_1 \parallel B(V_{cc})$
- when no signal is applied, the o/p would be Q-point
- i.e., there is no o/p signal. ($I_c = 0$)
- consider that the signal is applied b/w E & B for +ve half of the applied signal R_s ~~app~~ the f.B is decreased.
- As a result the Base current I_b is decreased.
- And here both I_c & I_E are decreased as they are nearly- β times of the Base current.

$$V_{CB} = V_{CC} - I_c R_C$$

① A_i (Current Gain) :-

$$A_{ib} = \frac{h_{fb}}{1 + h_{ob} R_L}$$

[Note: B represents Base]

(i) Current Gain (A_i)

$$A_{ib} = \frac{I_c}{I_b} = \frac{-h_{fe} I_b}{I_b}$$

from fig $I_e + I_b + h_{fe} I_b = 0$

$$I_e = -I_b [1 + h_{fe}]$$

$$A_{ib} = \frac{-h_{fe} I_b}{-I_b [1 + h_{fe}]}$$

$$A_{ib} = \frac{h_{fe} I_b}{I_b [1 + h_{fe}]}$$

(ii) Input Resistance (R_{ib})

$$R_{ib} = \frac{V_{eb}}{I_e} = \frac{-h_{ie} I_b}{-(1 + h_{fe}) I_b}$$

$$R_{ib} = \frac{h_{ie} I_b}{(1 + h_{fe}) I_b}$$

$$R_{ib} = \frac{h_{ie}}{(1 + h_{fe})}$$

(iii) voltage Gain (A_{vb})

$$A_{vb} = \frac{V_{cb}}{V_{eb}} = \frac{-h_{fe} I_b R_L}{-h_{ie} I_b}$$

$$A_{vb} = \frac{h_{fe} R_L}{h_{ie}}$$

(iv) output Impedance R_{ob}

$$R_{ob} = \frac{V_{cb}}{I_c} \text{ with } R_L = \infty \text{ \& } V_s = 0$$

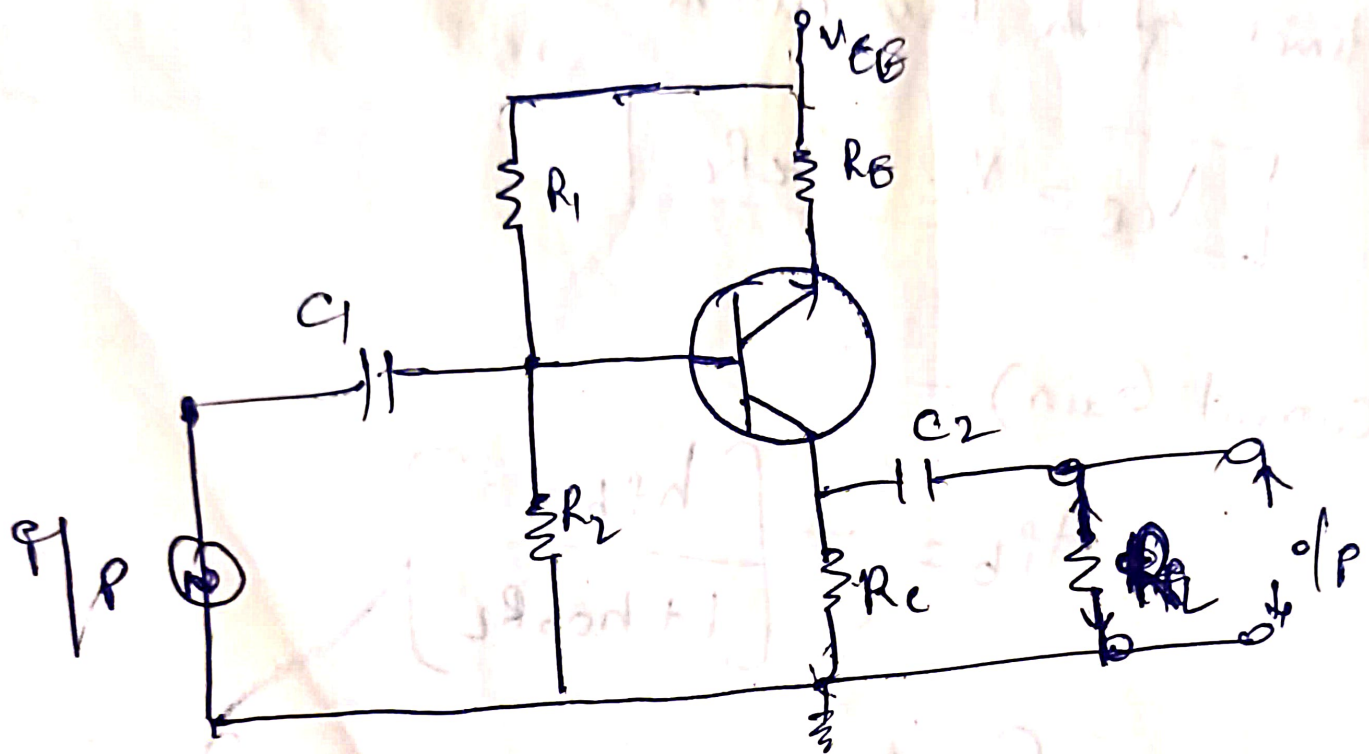
with $V_s = 0$, $I_e = 0$ \& $I_b = 0$

1. $I_c = 0$

$$\therefore R_{ob} = \frac{V_{cb}}{0} = \infty$$

$$R_{ob} = \infty$$

③ Common collector Amplifier



- The i/p signal is applied b/w base-collector circuit while the o/p signal is taken from emitter-collector circuit.
- The E-B junction is f.b, the v/g of E-B is V_{EE} & collector-base junction is reverse-bias by V_{CC} .
- Both I_B & I_E are increased.
- The v/g drop across R_E i.e., o/p v/g is increased.
- As a result, we get +ve half cycle. There is no phase reversal in this case i.e., input & output are in phase.

① (A_i) current Gain :

$$A_{iC} = - \frac{h_{fc}}{1 + h_{oc} R_L}$$

['C' represents collector]

② R_i (Input Resistance)

$$R_{ic} = h_{ic} - \left(\frac{h_{fc} h_{oc} R_L}{1 + h_{oc} R_L} \right)$$

③ output Resistance (R_o) :-

$$R_{oc} = h_{oc} - \frac{h_{fc} \cdot h_{oc}}{h_{ic} + R_s}$$

④ voltage Gain (A_v) :-

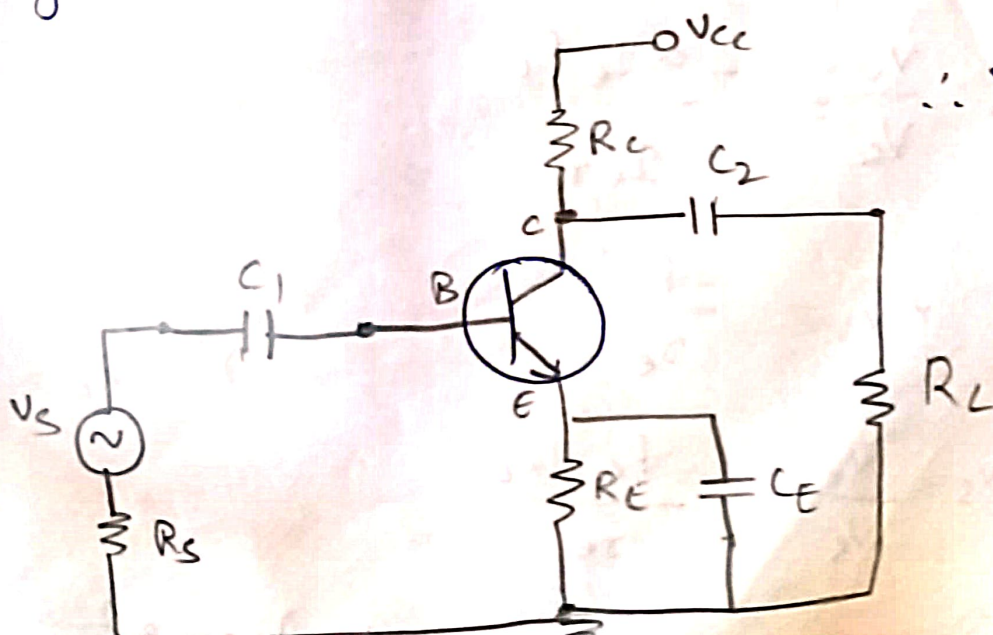
$$A_{vc} = \frac{-h_{fc}}{R_{ic} \left[\frac{1}{R_L} + h_{oc} \right]}$$

* Approximate CE (Common Emitter) model with and without emitter bypass capacitor:

→ The common-emitter (CE) amplifier's AC small-signal model is primarily affected by the presence or absence of the emitter bypass capacitor (C_E) connected in parallel with the emitter resistor (R_E).

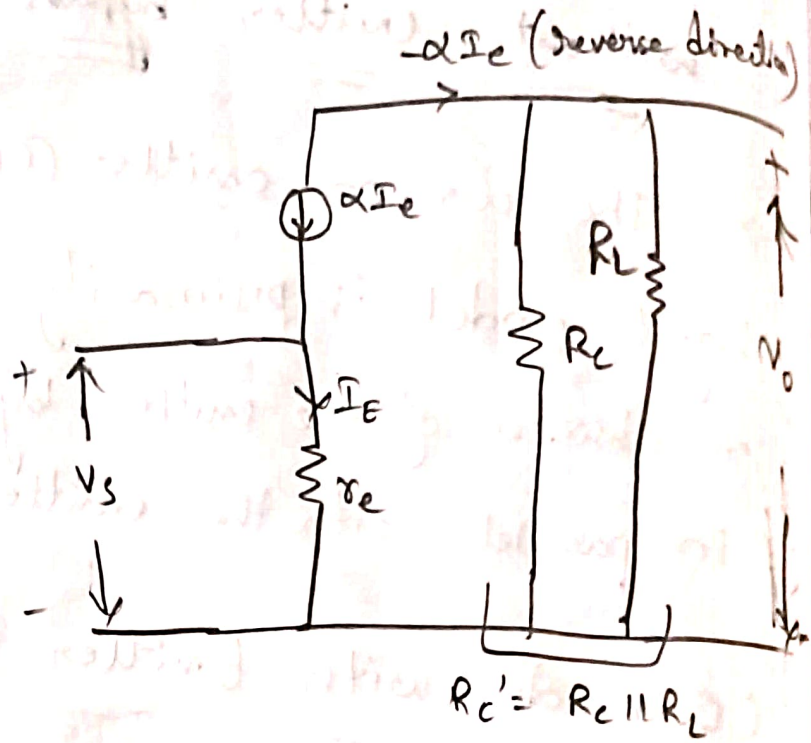
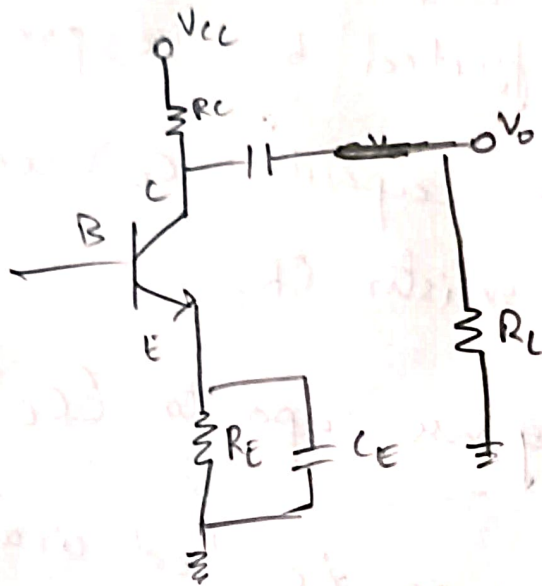
CE model with Emitter Bypass capacitor (C_E):

- when C_E is present, it acts as an AC short circuit at the midband frequencies, Block DC & allow AC signals to pass.
- This effectively removes R_E from the AC Equivalent circuit, eliminating the negative feedback it would provide.
- Bypass capacitor (C_E) connected in parallel with emitter resistor (R_E)
- Higher Gain, lower Input resistance, less stability.



∴ There is no negative feedback

$$r_e = \frac{V_T}{|I_{Ea}|}$$



$$A_{V_s} = \frac{V_o}{V_s} = \frac{-\alpha I_e R_c}{I_e r_e}$$

$$A_{V_s} \approx -\frac{R_c}{r_e}$$

$\left[\because \alpha \text{ is nearly '1' because } \beta \text{ very large} \right]$
 $\alpha = \frac{\beta}{1+\beta}$

The above equations are without load Resistance.

$$\rightarrow A_{V_s} = \frac{V_o}{V_s} = \frac{-\alpha I_e R_c'}{I_e r_e}$$

$$A_{V_s} = \frac{-R_c'}{r_e}$$

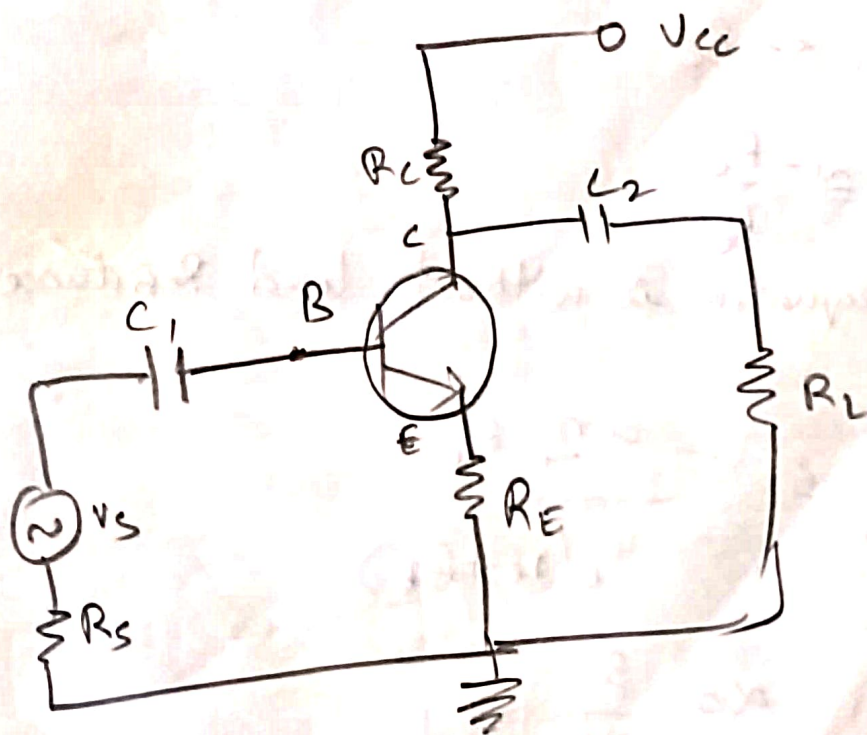
$$A_{V_s} = \frac{V_o}{V_s} = \frac{-R_c || R_L}{r_e}$$

$\left[\because R_c' = R_c || R_L \right]$

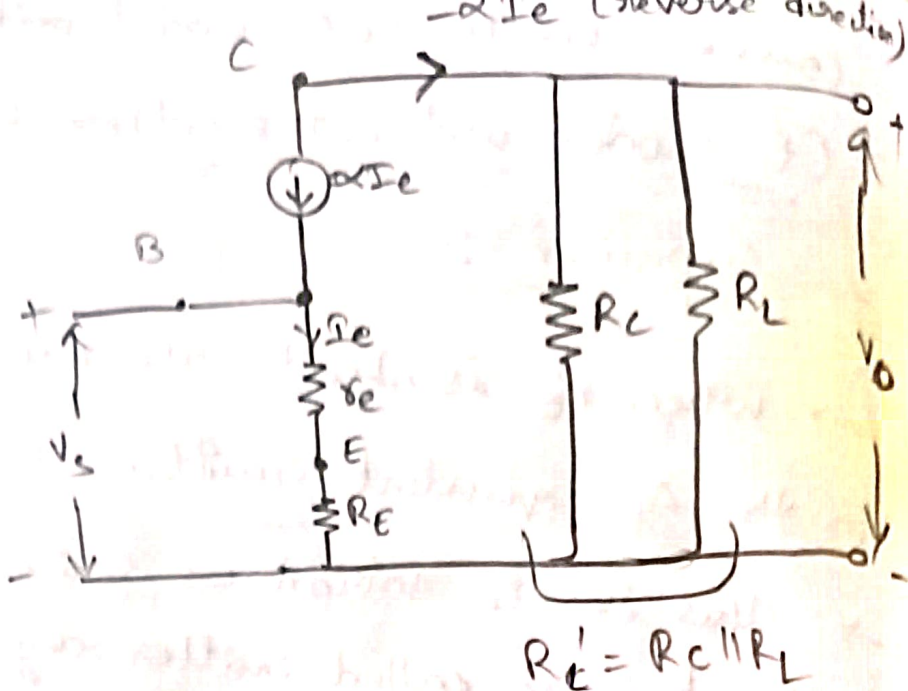
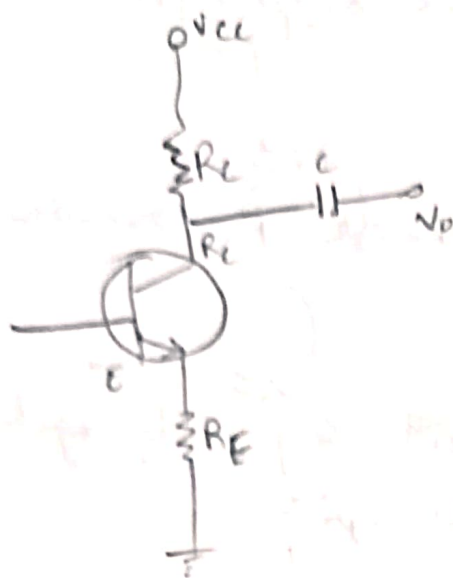
The above equations are with load resistance

Common emitter (CE) model without emitter - b
CE model without emitter bypass or unbypass
Capacitor :-

- when CE is absent, the emitter Resistor R_E remains in the AC Equivalent circuit.
- This resistor introduces series current-series v/g negative feedback (also called emitter degeneration)
- which stabilizes the Amplifier but sacrifices v/g Gain.
- No bypass capacitor → emitter resistor remains in circuit for AC signals
- provides negative feedback, Improving stability but reducing Gain
- lower Gain, higher Input resistance, better linearity & stability.



R_E introduce negative feedback



$$\rightarrow A_{V_s} = \frac{V_o}{V_s} = \frac{-\alpha I_e R_c}{I_e (r_e + R_E)}$$

$$\text{if } \beta \gg 1, \quad \alpha = \frac{\beta}{\beta + 1} \approx 1$$

$$A_{V_s} = - \frac{R_c}{r_e + R_E}$$

$$\therefore r_e \ll R_E$$

$$A_{V_s} \approx - \frac{R_c}{R_E}$$

The above equation is without load Resistance

$$\rightarrow A_{V_s} = \frac{V_o}{V_s} = \frac{-\alpha I_e R'_L}{I_e (r_e + R_E)}$$

$$\text{if } \beta \gg 1, \quad \alpha \approx \frac{\beta}{\beta + 1} \approx 1$$

$$r_e \ll R_E$$

$$A_{V_S} = \frac{-R_L'}{r_e + R_E}$$

$$A_{V_S} = \frac{V_o}{V_s} = \frac{-R_C \parallel R_L}{r_e + R_E}$$

$$A_{V_S} \approx -\frac{R_C \parallel R_L}{R_E} \quad (\because r_e \ll R_E)$$

The above equation is with load resistance.

<u>Feature</u>	<u>With CE</u>	<u>without CE</u>
Voltage Gain	High	low
Circuit stability	low	High
Distortion	Higher distortion	lower distortion

with Capacitor
 * For applications requiring maximum signal Amplification (eg: initial stages of a RF receiver) the Bypassed design

without Capacitor.
 * For applications requiring high fidelity and consistent performances (eg. driver stages, pre amplifiers), the unbypassed design is preferred.

UNIT - V

SPECIAL PURPOSE DIODES

Introduction:

- Special purpose diodes are diodes designed for specific functions other than normal rectification.
- They work based on special properties like breakdown voltage, light, temperature, or fast switching.

* Zener diode

* LED

* photodiode

* Schottky diode

* Tunnel diode

* Varactor diode

* Laser diode

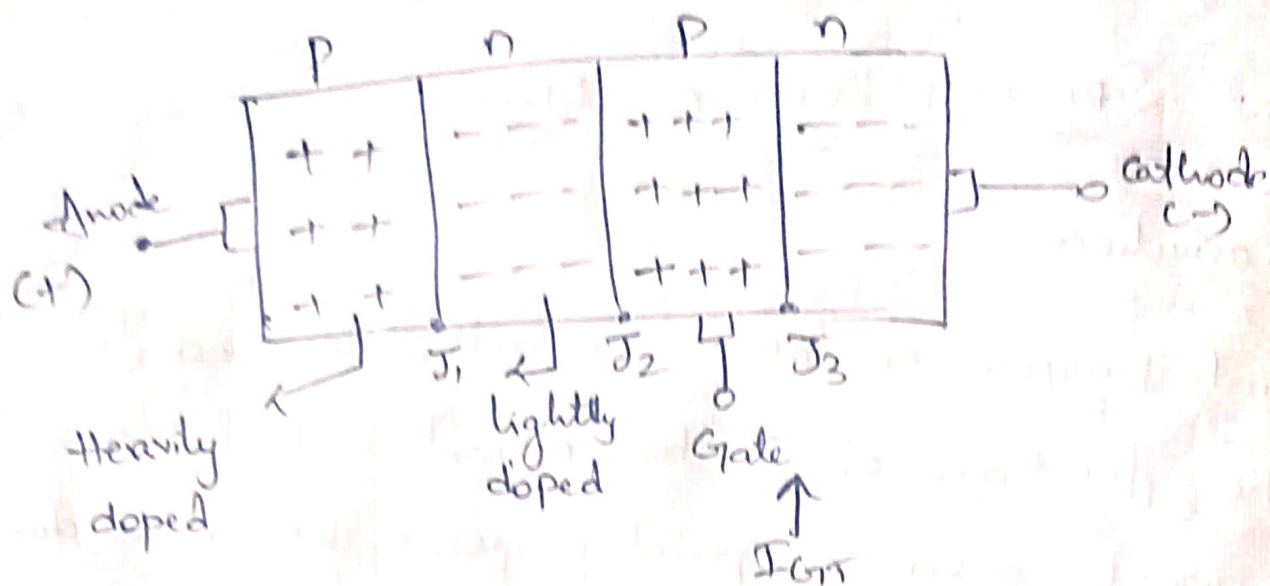
* pin diode

→ These are special applications.

* Principle of operation of - SCR:-

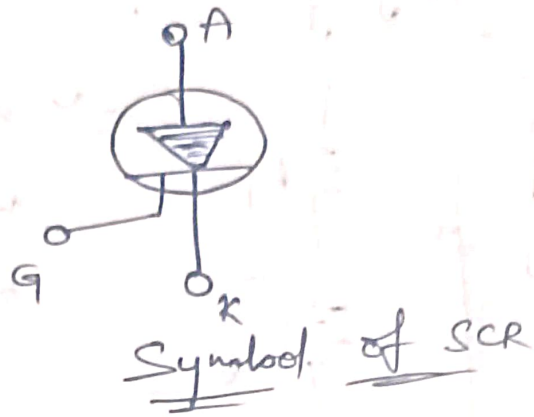
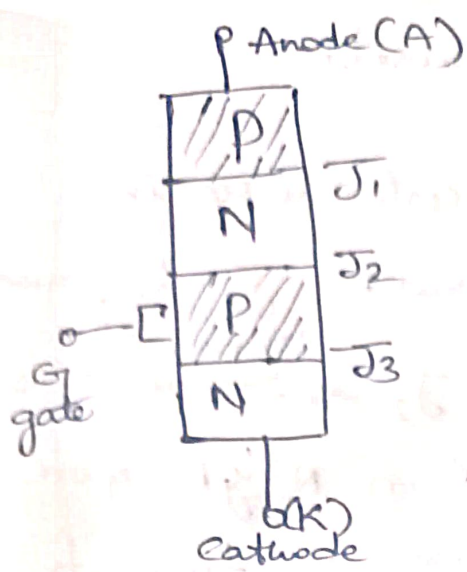
SCR → Silicon Controlled Rectifier:-

- The SCR is unidirectional device & it allows flow of current in only one direction.
- But it has built in feature to switch 'on' & 'off'.
- The SCR switching (ON, OFF) is controlled by gate and biasing conditions.



Construction of SCR

- SCR is a four layer p-n-p-n device where p & n layers alternately arranged. The outer layers are heavily doped.
- There are three pn junctions called J_1 , J_2 , J_3 .
- The outer p-layer is called anode, while outer n-layer is called cathode, the middle layer is Gate.
- Anode & Cathode are not sufficient to turn "ON," SCR.
- To make it 'ON', a current is to be passed through this gate terminal denoted as (I_{GIT}).
- Thus SCR is current operated device.



Case (i) Gate is open

Operation:-

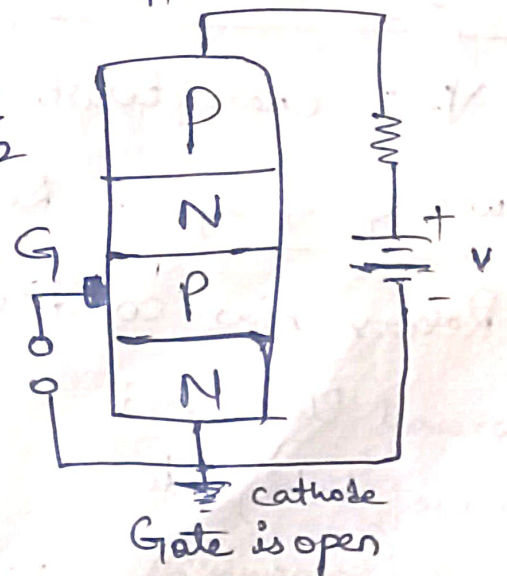
- In SCR a load is connected in series with Anode & kept positive with respect to cathode.
- The operation of SCR can be studied when the Gate is open.

- when the Gate is open no voltage applied at the gate. Then J_1 & J_3 are forward biased while J_2 is reverse biased.

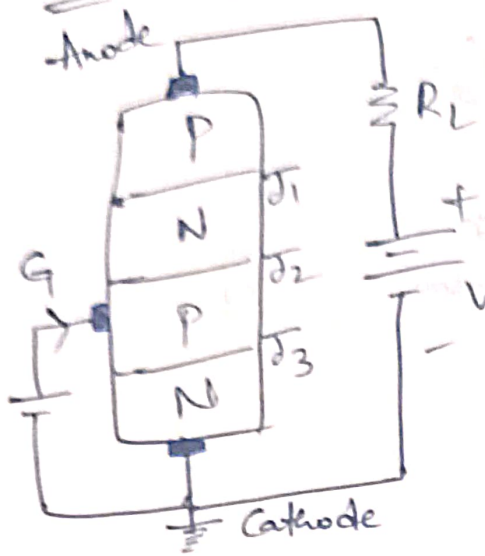
- Due to reverse bias of junction J_2 no current flows through R_L and hence SCR is cutoff when no anode voltage is increased beyond critical value, then junction ' J_2 ' breakdown.

- Now SCR conducts heavily and is said to be ON.

- Hence SCR offers little forward resistance.



Case (ii) Applying voltage at gate terminal



→ when the gate is positive w.r.t cathode J_3 is forward bias while J_2 is reverse bias. ^{Forward} electrons from N-type move across junction J_3 towards Gate while hole from p-type move across junction J_3 towards cathode.

Here J_1, J_2, J_3 are f.b

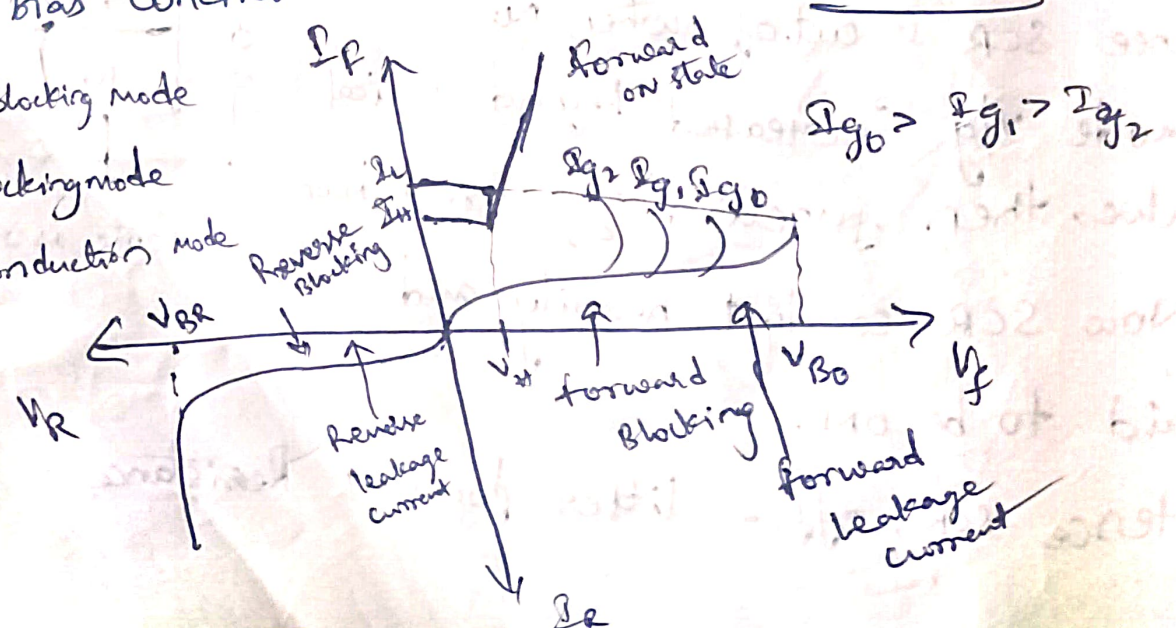
→ So Gate current start flowing $\approx I_n$, once SCR starts conducting the Gate loses all control the current keeps flowing indefinitely untill circuit is open.

V-I characteristics :-

→ V-I characteristics in forward bias condition drawn b/w V_f & I_f

→ Reverse bias condition drawn b/w V_R and I_R

- ① forward Blocking mode
- ② Reverse Blocking mode
- ③ forward conduction mode



→ V_g characteristics of a SCR for $I_G = 0$ when the anode is positive w.r.t cathode the characteristics known as forward characteristics. Once ON, SCR starts conducting even gate is removed.

→ volt corresponding to 'A' is called forward V_g , & Gate is open the breaker V_g is defined as minimum forward V_g at which SCR start conducting heavily.

→ under the condition V_g across SCR. suddenly drops as shown by dotted curve AB.

→ The current corresponding to point B is I_H & is known as holding current.

Reverse characteristics: Anode to cathode V_g is reversed then device enter into reverse blocking region, the current is negligible small & practically neglected.

→ If reverse V_g increases similar to diode at particular value avalanche breakdown occurs and large current flows through breakover V_g Greater than reverse breakover V_g .

Advantages :-

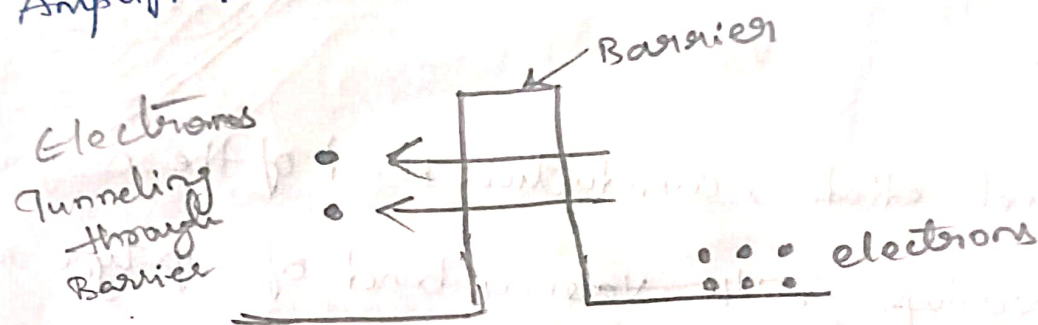
- Very small amount Gate drive required
- SCR with high V_g & current ratings available.

Disadvantages :-

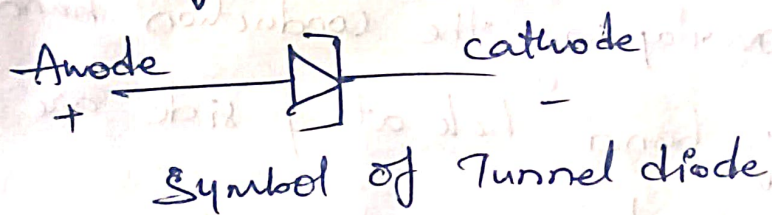
- ~~very small amount~~ Gate drive required.
- Gate has no control, Once SCR turned 'ON'.
- Operating frequency are low.

* Tunnel diode *

- Tunnel diode is a heavily doped PN junction diode in which electric current decreases as voltage increases.
- The tunnel diode is used as very fast switching device in computers. It is also used in high frequency oscillator and Amplifiers.



→ Meaning of Tunnel is moving.

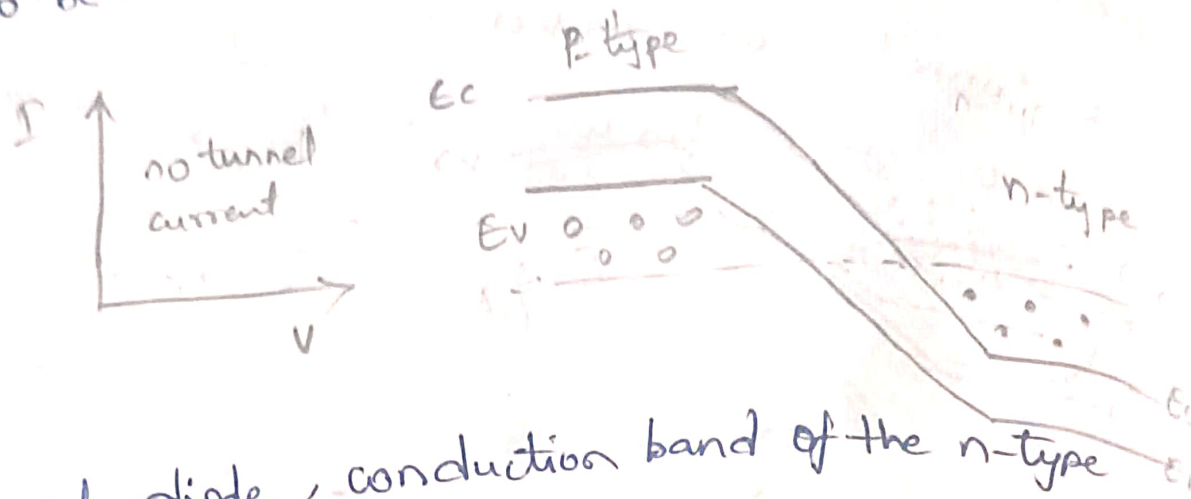


- It is mainly designed using Germanium material other than Germanium these diode are made up of Gallium Arsenide, Gallium Antimonide, Silicon.
- Anode is positively charged electrode which attracts e^- s.
- Cathode is negatively charged electrode which emits e^- s.
- n-type semiconductor emits e^- s, so it is referred to as Cathode.
- p-type semiconductor attracts e^- emitted from n-type semiconductor. so p-type referred as the anode.

Working:-

Case (i):- Unbiased tunnel diode:-

→ when no voltage is applied to the tunnel diode it is said to be an unbiased tunnel diode.



→ In a tunnel diode, conduction band of the n-type material overlaps with valency band of p-type material because of heavy doping.

→ Because of this overlapping the conduction band e^- at n-side & valency band hole at p-side are nearly at the same energy level.

→ So, when temperature increases, some electrons tunnels from conduction band of n-region to the valency band of p-region.

① → In a similar way holes tunnel from valency band of p-region to the conduction band of n-region.

②

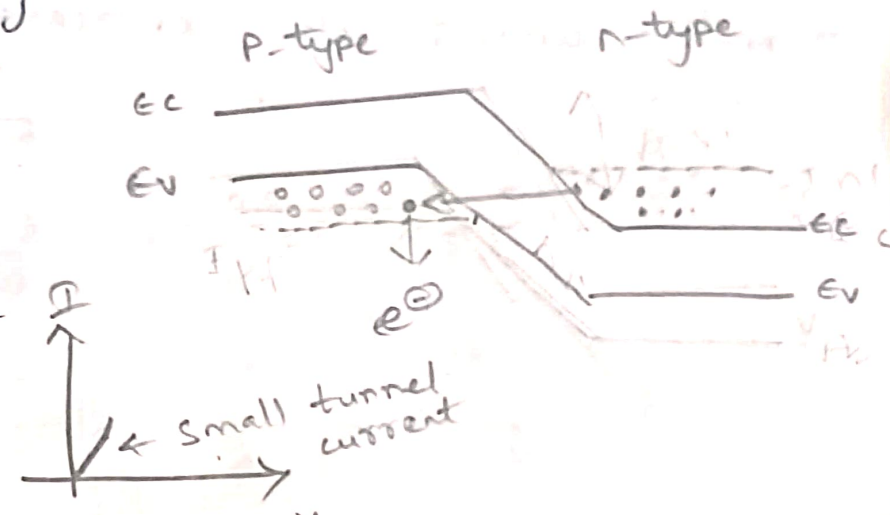
③

Case (ii):- Small voltage applied to tunnel diode

- when small voltage applied to diode is less than critical value (V_c) built in V_g of depletion layer no current flows through junction.
- small no. of e^- in conduction band will move to the empty state of valency band in p -region. This create small forward current.

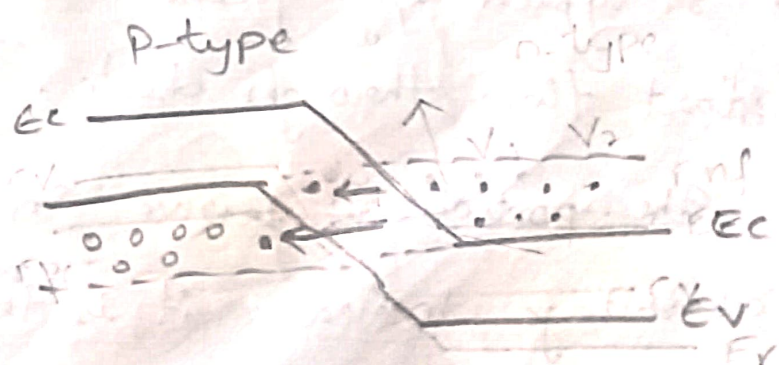
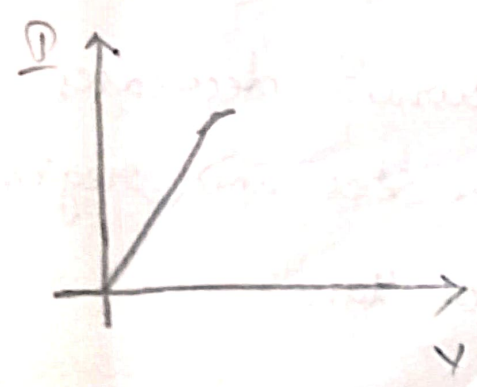
○ → hole
● → electron

C.B → conduction band
V.B → valency band



Case (iii) Applied voltage slightly increases:-

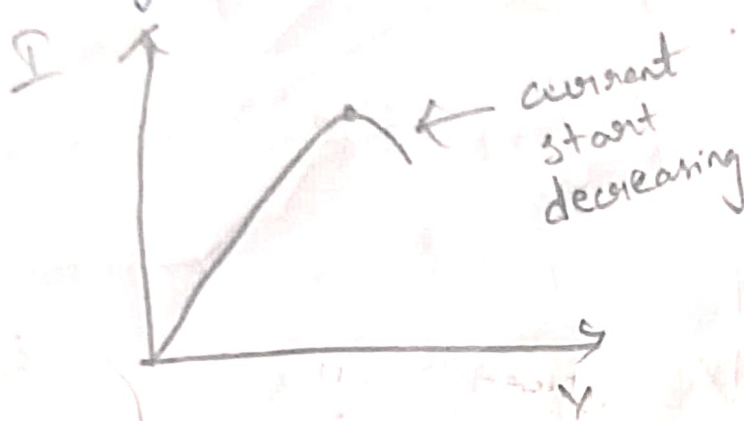
- when V_g to diode increases, large no. of free e^- , holes generated.
- V_g increases overlapping of conduction band & valency band is increased.
- Energy levels of C.B, & V.B are equal maximum current flows.



Case (iv) Applied voltage further increased:

→ If Applied V_g is further increased, misalign of C.B & V.B takes place

→ e^- from C.B move to V.B cause small current flow tunneling current start decreasing.



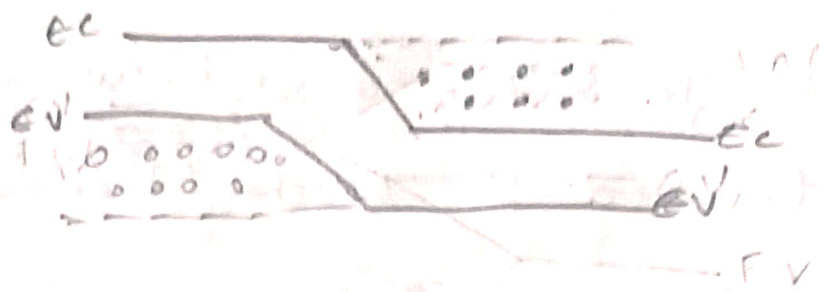
Case (v) Applied V_g largely increased:

→ If Applied V_g largely increases the tunneling current drop to zero

→ At this point no longer overlap of C.B & V.B it work similar to pn diode.

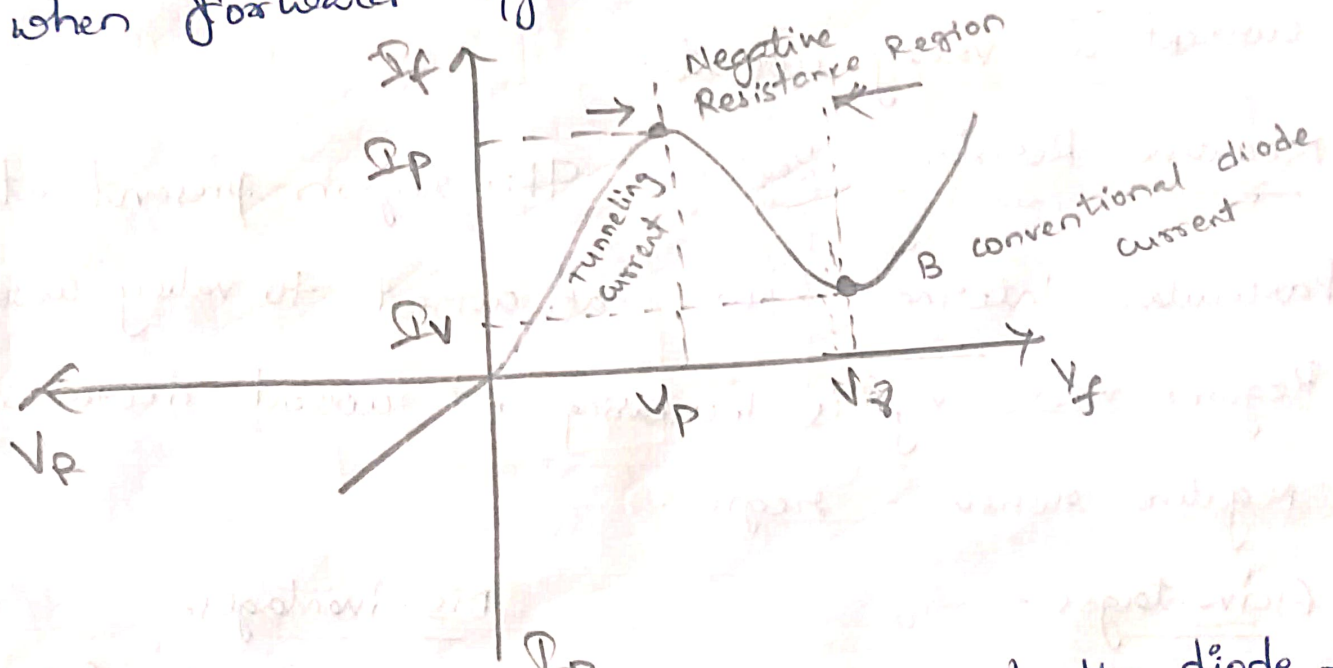
→ If applied V_g greater than built in potential current start flow through diode.

→ The portion of curve in which current decreases as voltage increases it is the negative resistance region of tunnel diode used in amplifier or oscillator



V-I characteristics:-

As soon as forward bias is applied significant current produced the current reaches its peak value I_p . when forward V_f 's reduces value V_p .



- when forward V_f is further increased the diode is current start decreasing thus reaches a point I_v corresponding to a valley voltage V_v .
- The region from point A to B is called as negative resistance region. for the voltages greater than V_v the current start rising as in case of normal pn junction diode.

Peak Current point (I_p):-

→ The voltage at which current flowing through tunnel diode reaches maximum value named as Peak current (I_p).

Valley current (I_v):- The v/g which the tunnel diode current increases after a portion of decrement of v/g at which tunnel diode ^{is ready to work as PN diode} named as valley v/g & corresponding current is valley current.

Negative Resistance Region:- This region present at Particular Interval b/w peak current to valley current. Region where v/g is increasing but current decreases i.e., negative resistance region.

Advantages:-

- low cost
- low noise
- low power consumption

Disadvantages:-

- Difficult to fabricate
- low operating v/g
- Temperature sensitivity

Applications:-

- As high speed switch
- In computer logic circuits
- High frequency oscillators, Amplifiers.

* Varactor diode :-

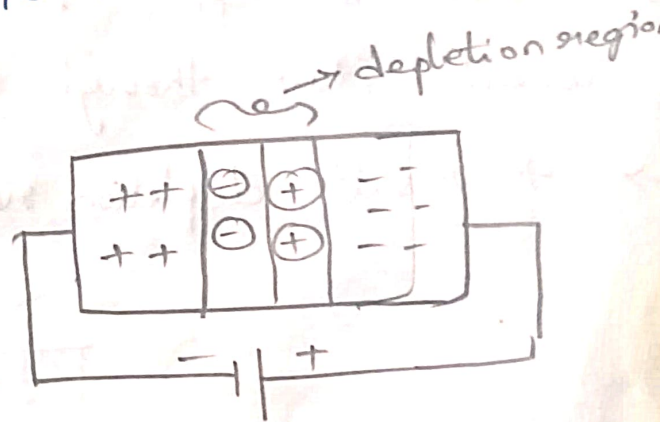
→ It is also named as variable capacitor, varicap (or) voltage variable capacitor, Tuner circuit.

→ Variable capacitor ~~or~~ varactor diode are mainly preferred under reverse bias condition. It is also a junction diode with small Impurity doping at its junction.

→ It has a useful property that its junction / Transition capacitance is easily varied due to diode preferred for high frequency applications.



Symbol of varactor diode



→ When any diode is reverse bias, a depletion region will form.

→ The larger reverse bias V_R is applied across the diode, the width of depletion region become wider & by decreasing reverse V_R become narrower.

→ Varactor diode acts like variable capacitor under reverse bias condition.

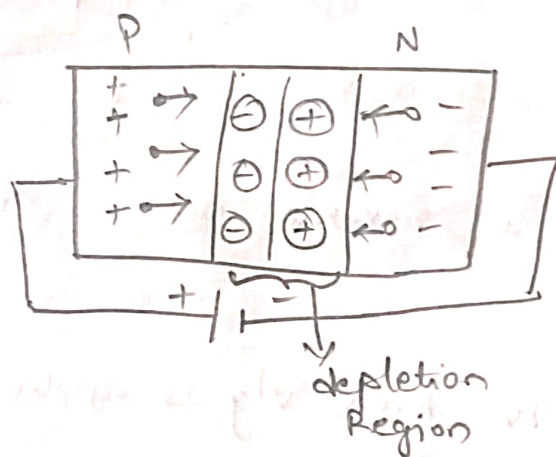
→ Another names varicap, Tuning, variable reactance, variable capacitance diode.

→ It is manufactured to show better transition capacitance property than ordinary diodes.

→ Symbol:  Two parallel lines at cathode represent two conductive plates & the space b/w two parallel lines represent dielectric.

→ when we apply forward bias V_g is applied electric current flows through diode.

→ As result depletion region become negligible

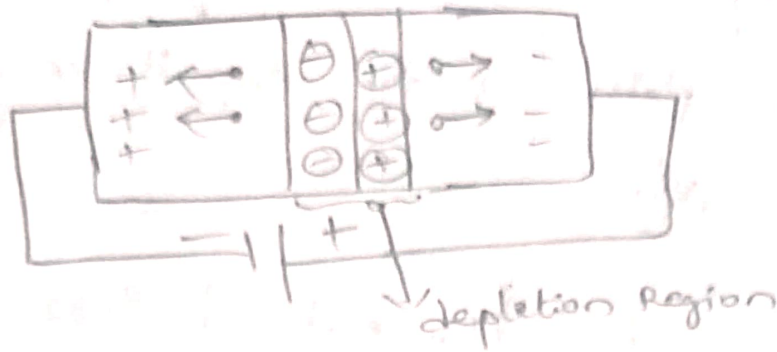


→ we know that depletion region consists of stored charges.

So stored charges become negligible which is undesirable.

→ Designing this to store charges not to conduct electric current.

→ when a Reverse bias V_g applied electron from n-region & holes from p-region move away from junction



R.B

→ As a result, width of depletion region increases and capacitance decreases.

→ Applied Reverse V/g is low then capacitance is very large

$$\text{Capacitance} \propto \frac{1}{\text{width of depletion region}}$$

→ R.B voltage ^(increases) Increases $\uparrow$, width of depletion region increases $\uparrow$, Capacitance decreases $\downarrow$.

→ The decrease in capacitance means decrease in storage charge. so R.B voltage kept at minimum to achieve large storage charge.

→ Thus, capacitance varied by varying the voltage.
 fixed capacitor → capacitance will not varied
 Variable capacitor → Capacitance varies.

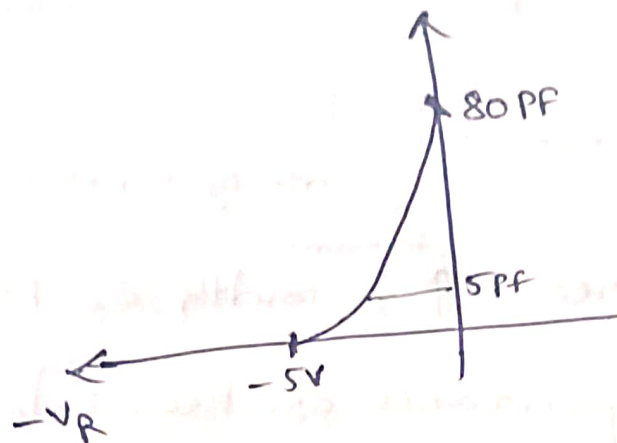
→ "Capacitance" measured in picoFarads (PF)

→ This Depletion region is consists of minority charge carriers & act like Insulator / dielectric where as two P & n region will acts as plates forming a capacitor.

→ As the Capacitance is inversely proportional to distance between the plates, so the capacitance varies inversely with applied V/g .

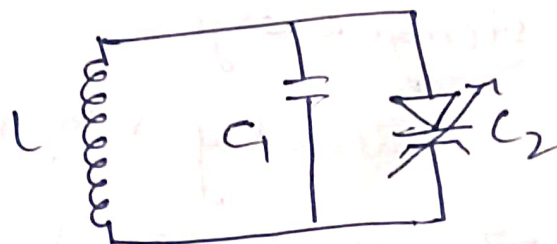
i.e., $C_T \propto \frac{1}{V_R}$

Characteristics:



Applications:

→ Main application of varactor diode is LC tuned circuit.



use of varactor diode LC tuned circuit

$$\text{Resonance frequency } (f_r) = \frac{1}{2\pi\sqrt{L(C_1 + C_2)}}$$

- FM modulator.
- Automatic frequency control device.
- Adjustable band pass filter.
- Television receivers.

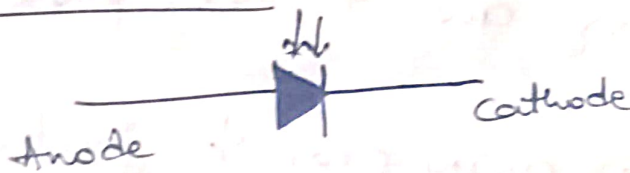
* photo diode:-

- It transforms light energy into Electrical energy very quickly.
- Another names photo detector, light detector, photo sensor.
- It operate under reverse bias condition.

Types of photo diodes:-

- pn photo diode:- It is first developed, it has poor sensitivity compared to other.
- PIN photo diode:- Mostly widely used photo diode.
- Avalanche breakdown:- Due to its high gain levels, this type of diode utilize in low light environment.
- Schottky photo diode:- It is used in optical communication it has low voltage drop

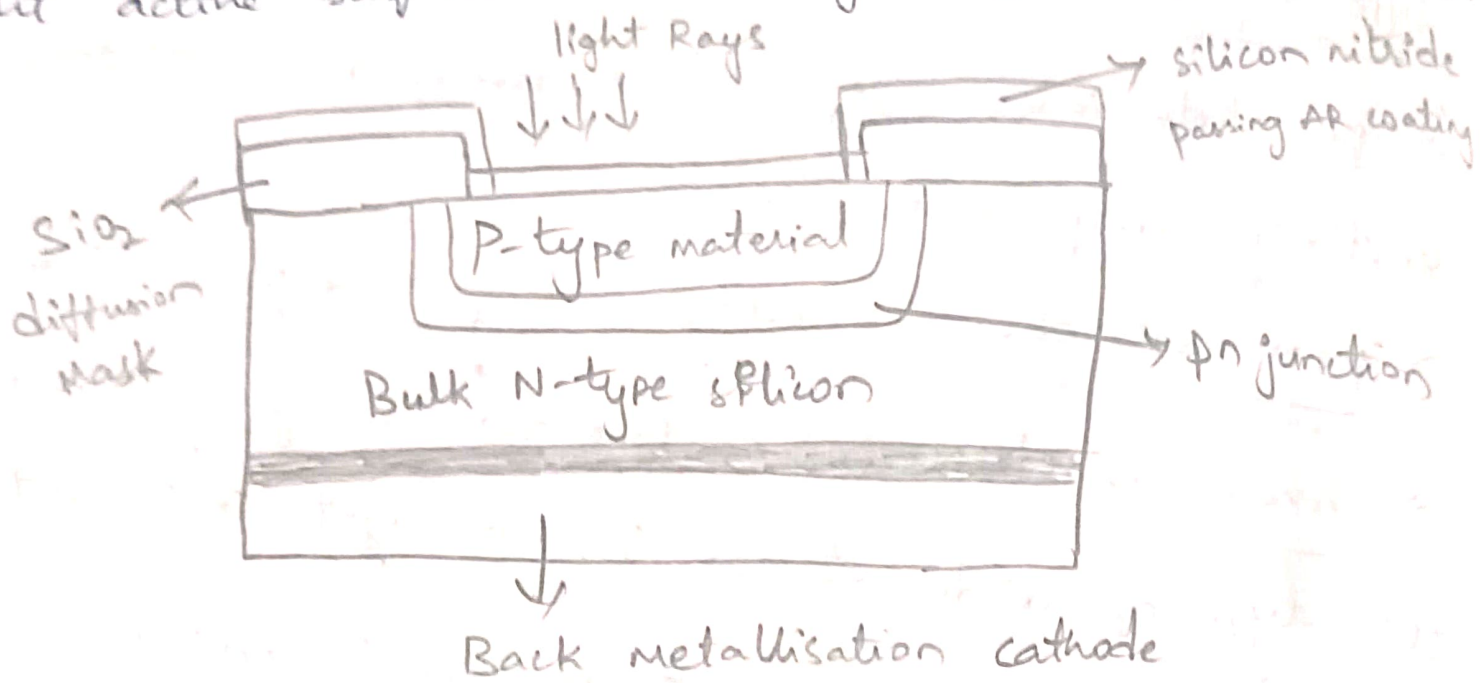
Symbol of photo diode:-



Construction:-

- P-type & N-type semiconductors can be used to create photo diode.
- Diffusion of p-type substrate, which is mildly doped. P⁺ ion layer formed due to Diffusion

- N-type epitaxial layer can form on N-type substrate
- Metals are used in the contacts construction to create two terminal that resemble an anode & cathode
- Active & non-active surfaces present
- Non-Active surface presents light rays from striking but active surface allows light rays to pass across it.



Working:

- when photon or light strike the diode it create holes and e^- recombination due to inner photoelectric effect.
- Carriers are move away from the junction
- ~~Holes~~ The sum of photo current & absence of light Make up total current flow through diode.
- Photons falls on the depletion region, & create e^- & holes.
- photo diode connected in Reverse bias, when light falls, reverse current increases.

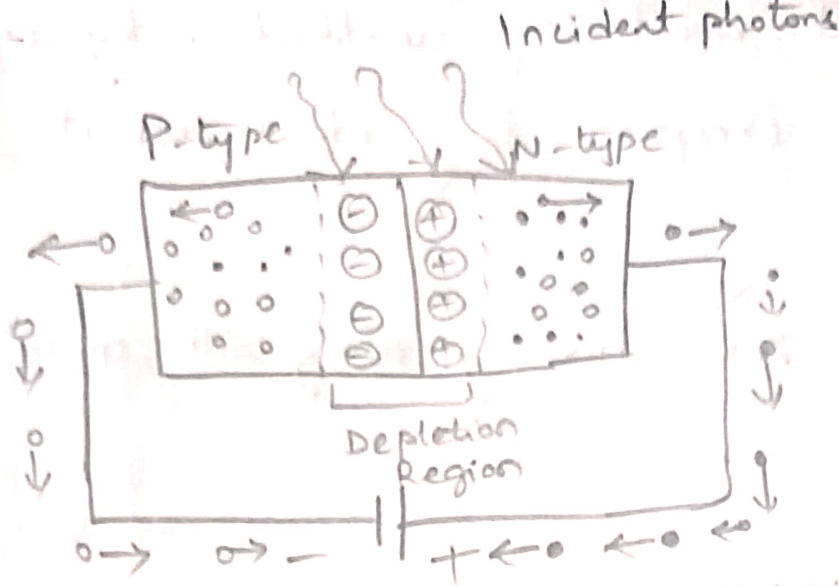


photo diode working principle

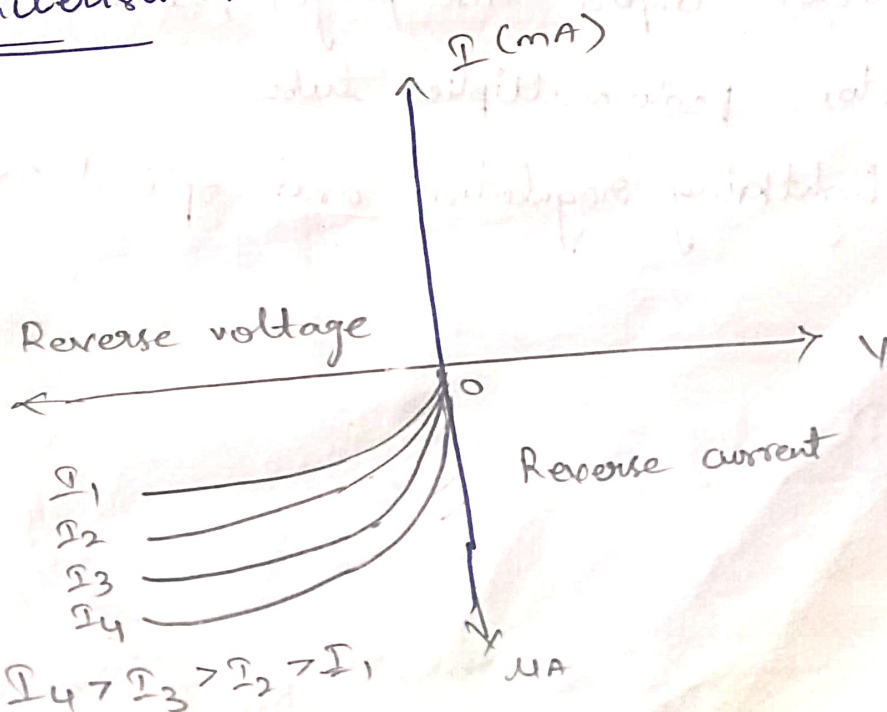
modes of operation:

① Photo voltaic mode - This referred as zero bias mode.

② photo conductive mode - width of depletion region more with applying reverse voltage

③ Avalanche breakdown - Operate with high reverse bias breakdown occur.

v-I characteristics:



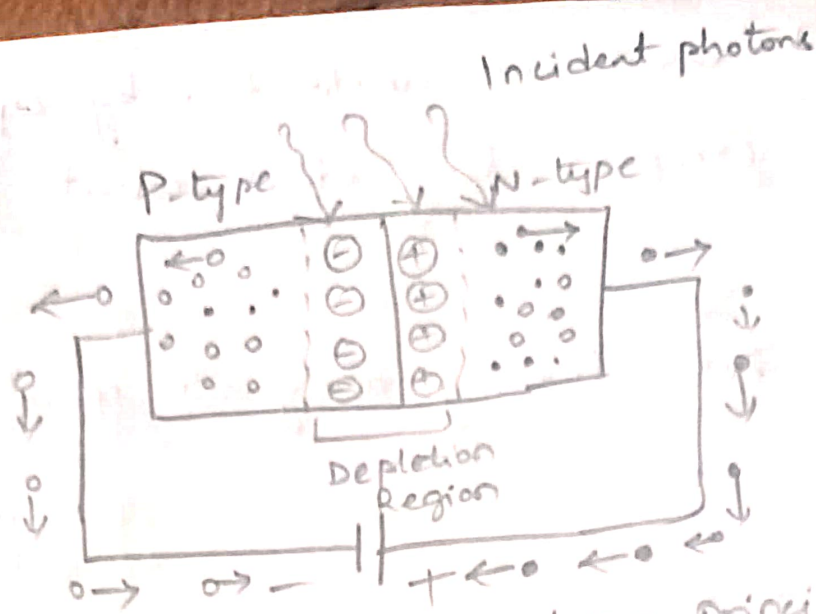
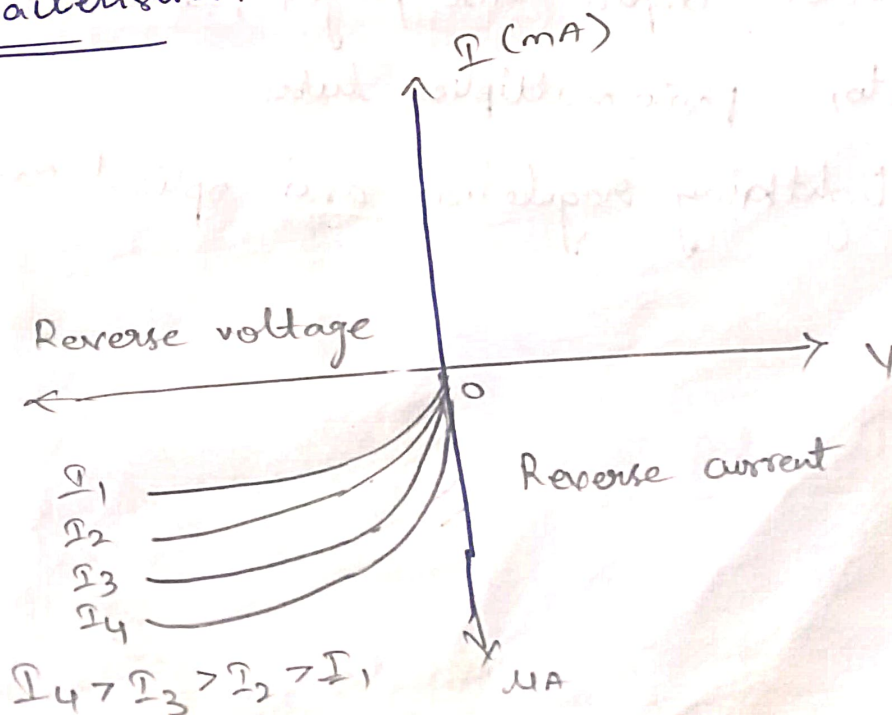


photo diode working principle

modes of operation:

- ① Photo voltaic mode - This referred as zero bias mode.
- ② photo conductive mode - width of depletion region more with applying reverse voltage
- ③ Avalanche breakdown - Operate with high reverse bias breakdown occur.

V-I characteristics:



→ photocurrent essentially unaffected by applying reverse voltage with exception tiny dark current. photocurrent is zero.

→ photocurrent rises linearly along with optical power.

Advantages:-

- less resistance
- long life span
- less noise
- less weight

Disadvantages:-

- Temperature stability is poor.
- less sensitivity.
- It uses offset voltage.

Applications:-

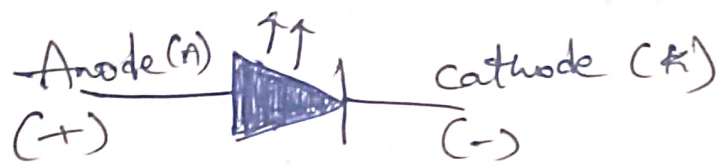
- Smoke detector, compact disc player, television
- photoconductor, photo multiplier tubes.
- Used for lightening regulation and optical communication.

* LED:- (Light Emitting Diode) :-

- An LED is a special type of diode that emits the light when electric current passes through it.
- It transfers Electrical Energy into light energy.
- It lights up when we apply the voltages it has longer life span than laser diodes.

Construction:-

- Same like pn junction diode LED also allow the current only in one direction i.e., forward bias condition. p-type material connected to +ve terminal & n-type material connected to -ve terminal of battery.
- LED consists of two terminals Anode & cathode.



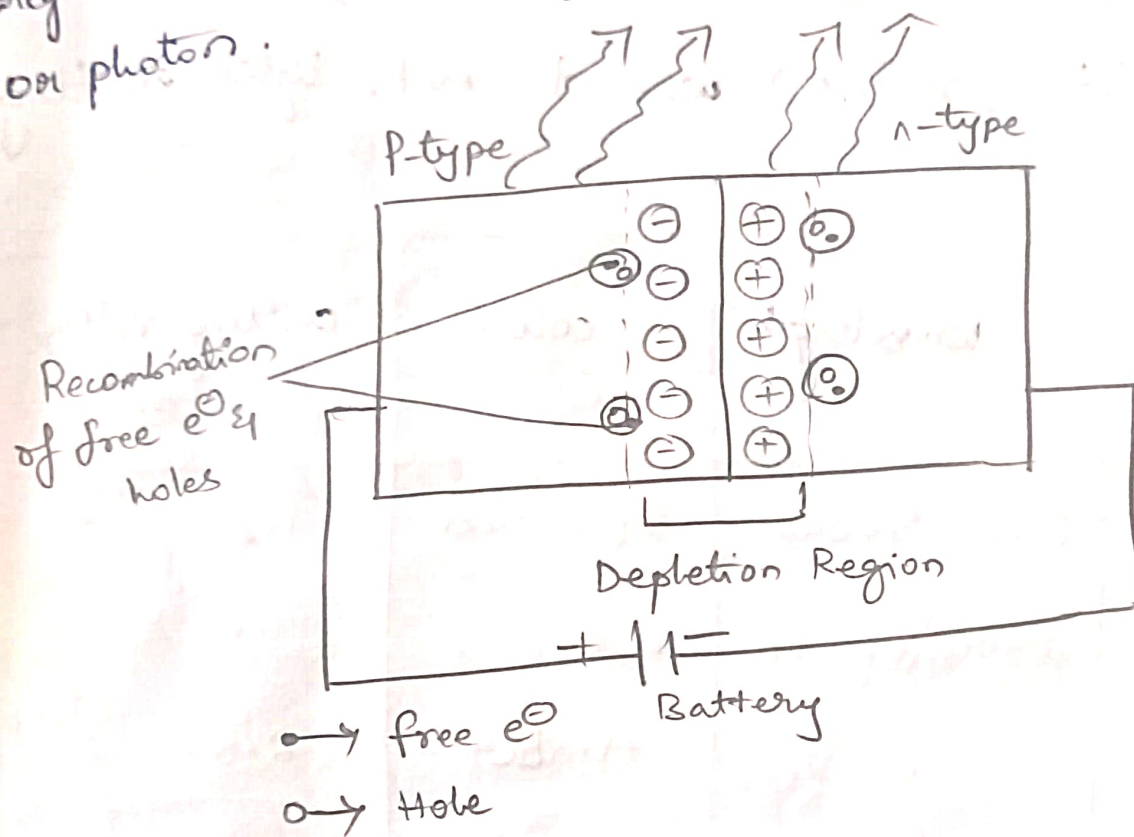
Symbol of LED.

- Light being emitted by the diode.
- LED comes in variety of colours, like, orange, yellow, Green, red LED are mostly available on LEDs.
- Symbol of LED does not represent any colour.
- Gallium, phosphorus, arsenic materials are used in construction.

Working:

→ LED function only in forward bias condition holes in the p-side & e^- s in the n-side move towards the junction.

→ electron recombine with hole width of depletion region produces. During this recombination produce light or photon.



Working of LED

Before recombining with holes in valency band the free e^- in conduction band lose the Energy in form of light.

→ The gadget may damaged if reverse bias voltage applied to LED's.

All diodes produce light (or) photons but not all of them produce ~~light (or) photons~~ visible light.

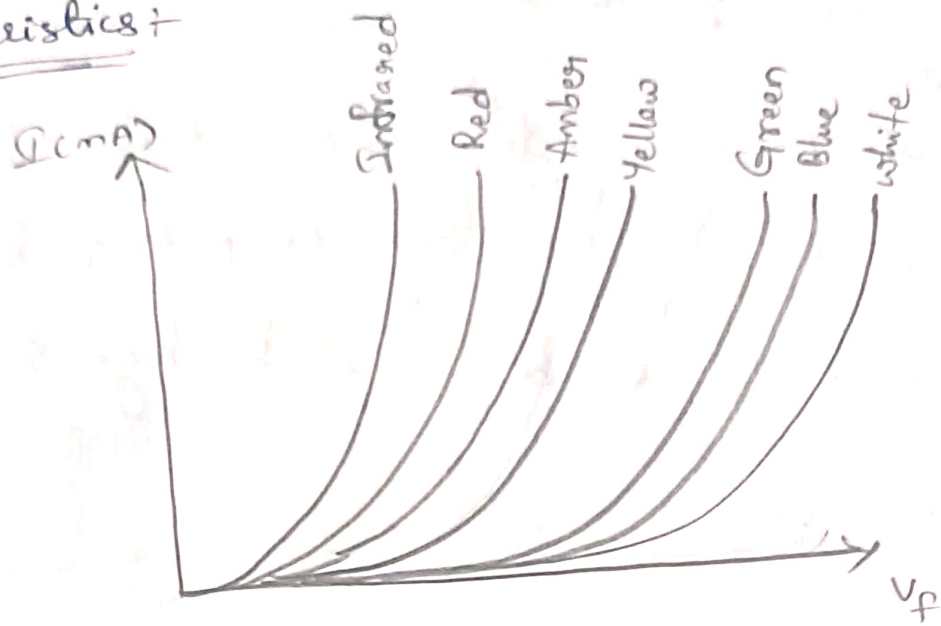
→ In just one millisecond LED can turn on & off.

Colours of LED:

Exotic semiconductor material such as gallium arsenide (GaAs), Gallium phosphide (GaP), Gallium arsenic phosphide (GaAsP), silicon carbide (SiC) (or) Gallium Indium nitride (GaInN) used to make light emitting diode.

Semiconductor Material	wavelength	colour	cutting voltage V_f
GaAs	850-940nm	Intra-red	1.2V
GaP	630-660nm	Red	1.8V
GaAsP	605-620nm	Amber	2.0V
GaAsP-N	585-595nm	Yellow	2.2V
AlGaP	550-570nm	Green	3.5V
SiC	430-505nm	Blue	3.6V
GaInN	450nm	white	4.0V

Characteristics:-



Advantages:-

- long life
- Energy efficiency
- High brightness, Reliability

Disadvantages:-

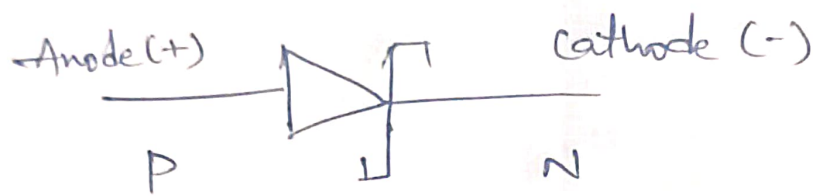
- Impact on Insects
- Temperature sensitivity
- Electrical polarity
- voltage sensitivity

Applications:-

- used As bulb in homes & Industries
- used In motorcycles & cars.
- Traffic light Signals.

* Schottky diode is a unipolar device

→ Schottky diode is a metal semiconductor junction diode that have less forward vlg drop (0.3-0.5) than Pn junction diode & can be used in high speed switching application.



Symbol of schottky diode

→ metal acts as anode and n-type semiconductor acts as cathode.

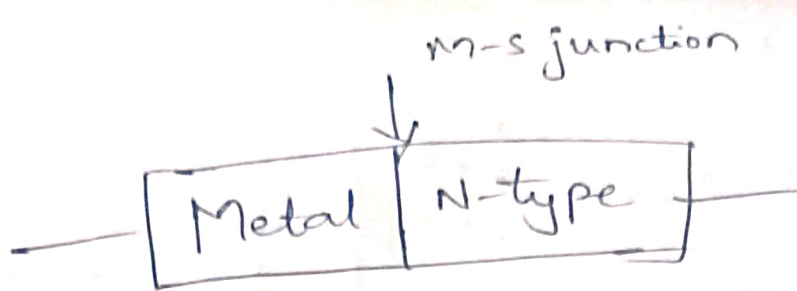
→ Metal like platinum & Aluminium replace the P-type semiconductor (Anode).

→ Another names of schottky diode are 'Schottky Barrier diode', 'surface barrier diode', 'Majority carrier device', 'Hot electron diode'

Construction : ^{when} Aluminium, platinum joined with n-type semiconductor, junction formed b/w them is called

M-S junction (or) Metal semiconductor junction (or)

Schottky barrier.



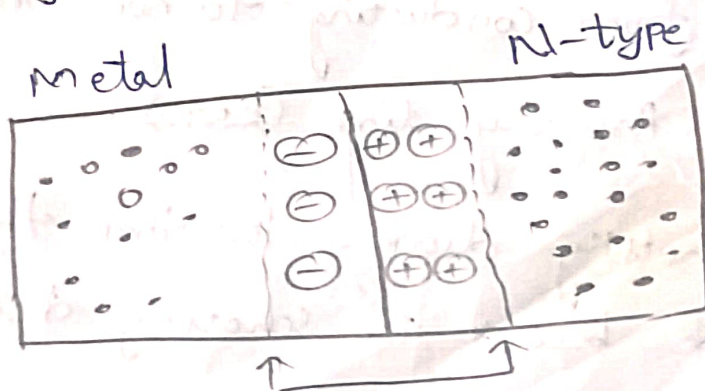
- Schottky diode can switch ON & OFF much faster than pn diode.
- produce less unwanted noise than pn diode

Working:-

- In a forward bias the electrons in N-side gain enough energy to cross the junction barrier & move into metal with large energy they are called it hot carriers.

So diode is called as hot carrier diode.

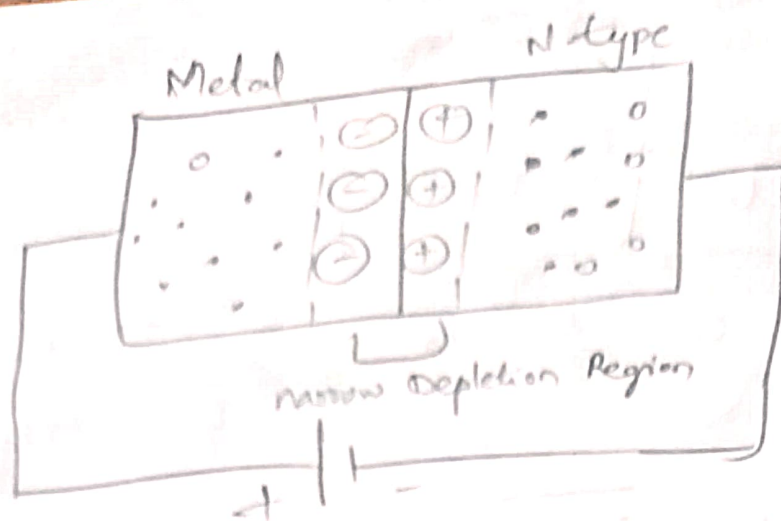
- Before applying a forward bias the e^- in N-side having less energy level than of metal so e^- cannot cross the junction barrier called Schottky barrier.



Fig(i) Schottky diode under unbiased condition

$\oplus$ → Positive ions

$\ominus$ → Negative ions



• $\rightarrow$ free e⁻
 ○ $\rightarrow$ free hole

Fig (ii) schottky diode under forward bias condition

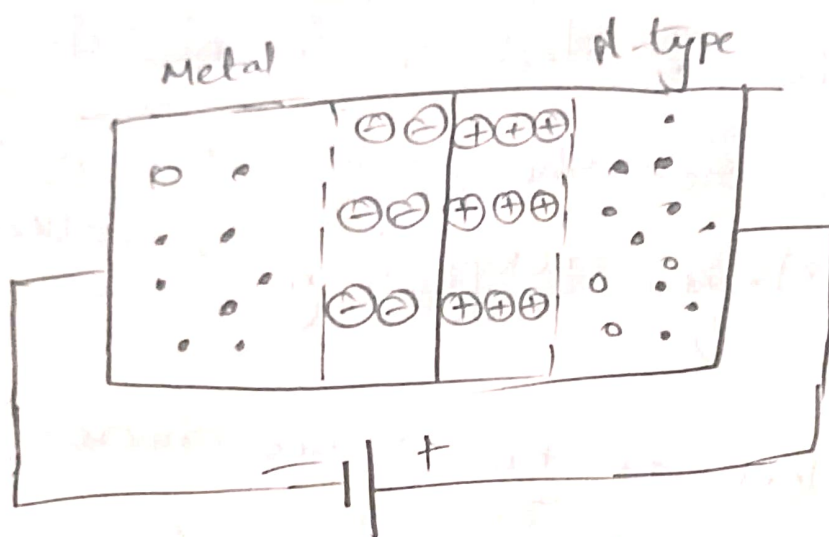


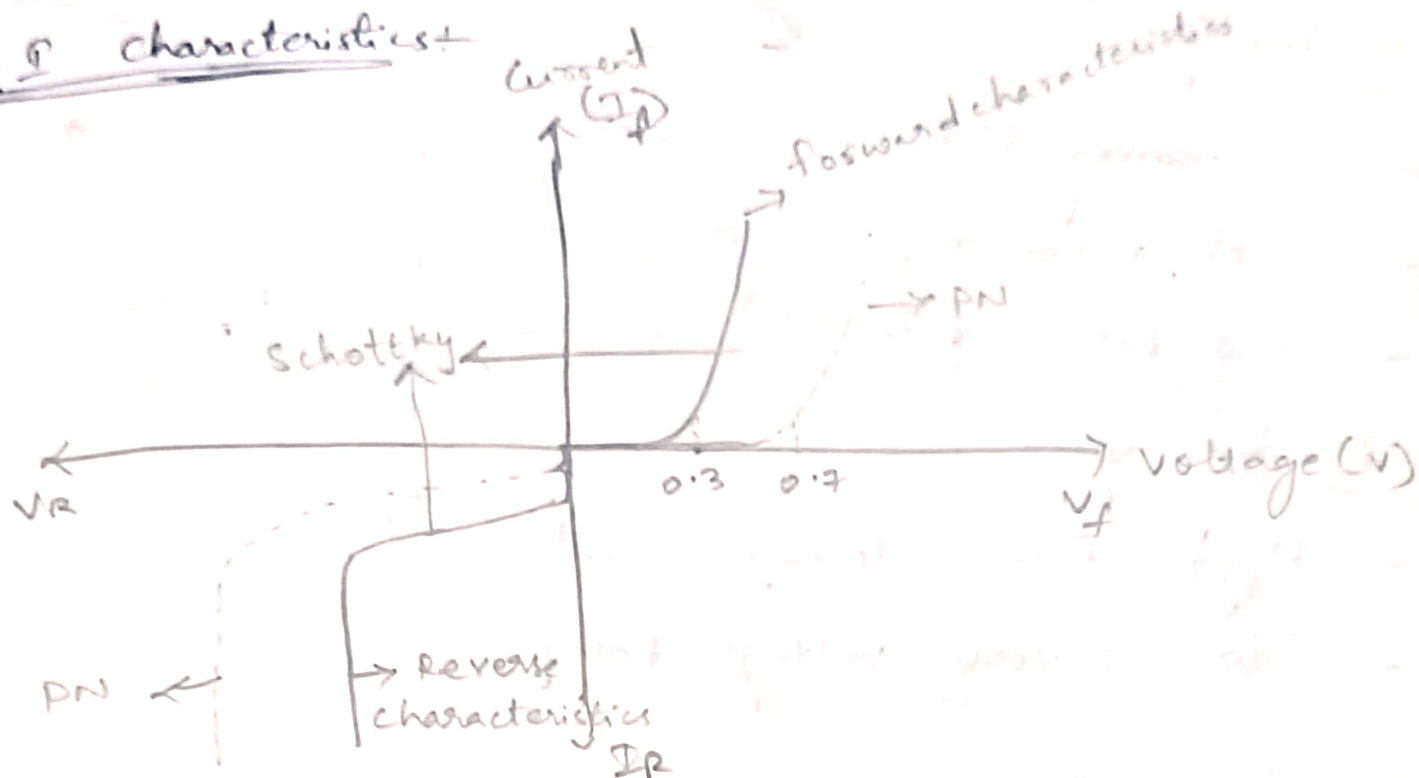
Fig (iii) schottky diode under reverse bias condition

Reverse Recovery time τ (RRT) :-

$\rightarrow$ The switching from conducting to non conducting state is called Reverse Recovery time (RRT).

$\rightarrow$ R.R.T of schottky diode is less than the normal Pn junction diode because in schottky diode No minority charge carriers.

V-I characteristics



----- Dot indicate characteristics of PN junction

—— straight line indicate characteristics of schottky

→ voltage drop of schottky diode range from 0.3 to 0.5V

Example:

Normal diode

$$I = 50A \quad V_f = 0.6V$$

$$P = V \times I \Rightarrow 50 \times 0.6$$

$$P = 30W$$

Schottky diode



$$I = 50A, \quad V_f = 0.3$$

$$P = V \times I \Rightarrow 50 \times 0.3V$$

$$P = 15W$$

Schottky diode dissipate less power due to low V_f drop than normal diode.

Advantages:

- less Recovery time
- less voltage drop
- low barrier potential

Disadvantages:-

- High Reverse leakage current.
- low reverse voltage Rating.

Applications:-

- Switching circuits.
- RF Mixers
- solar cell applications.

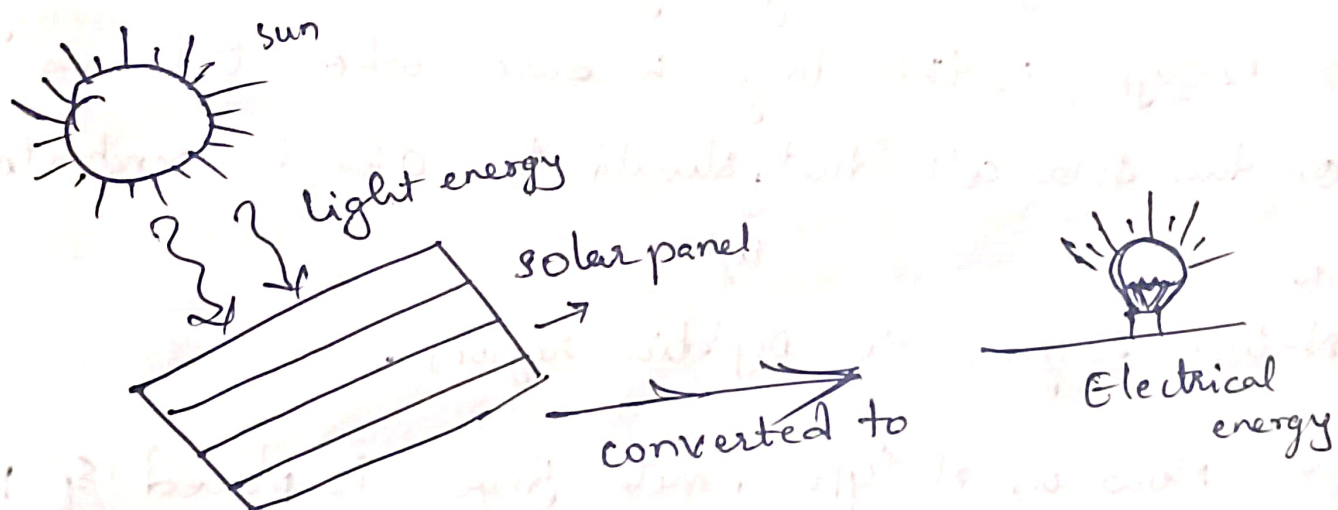
Solar Cell

Definition: A solar cell is an optical electronic device which converts light energy to Electrical energy.

→ Sun light can be used to convert it into electrical energy.

→ Beyond sun light, lamp light & also the artificial lights can be used.

for Better understanding:-

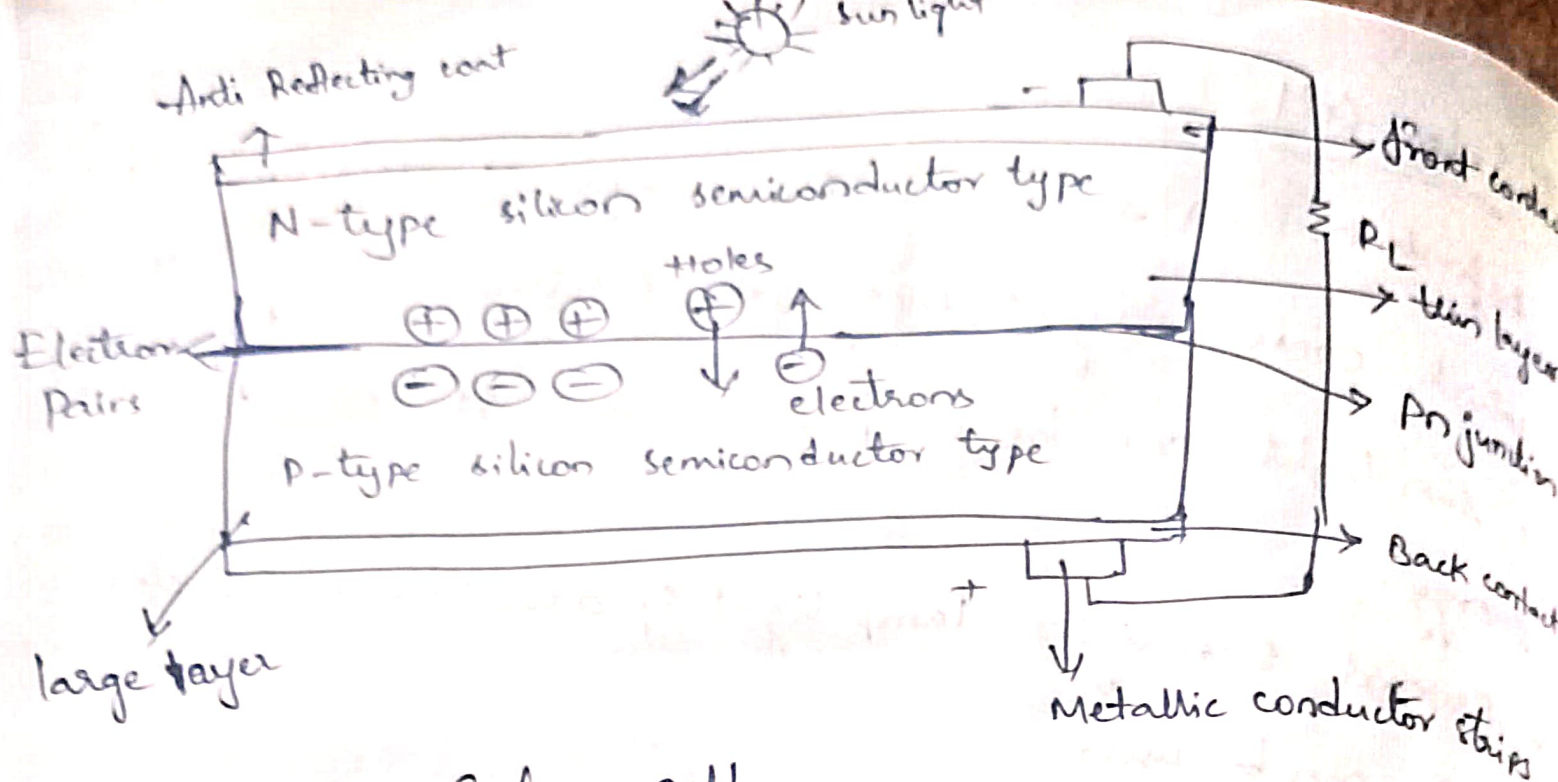


construction:

- In this solar cell we need p & n type materials.
- P-type doped with trivalent impurity.
- N-type doped with pentavalent impurity.

Note: → Here p-type is large layered

→ N-type is thin layered



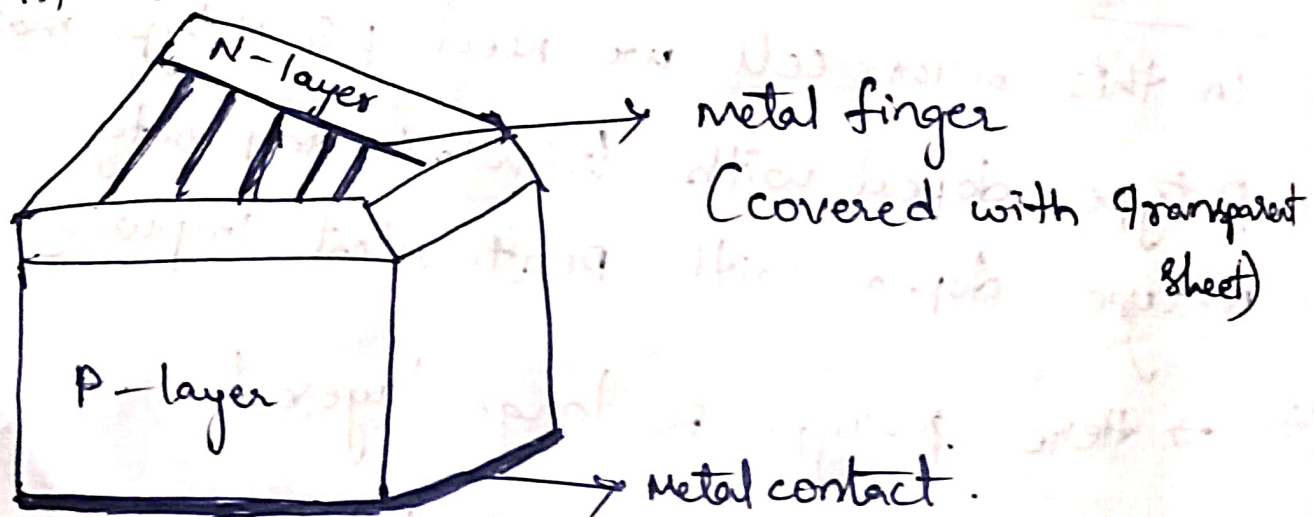
Solar cell

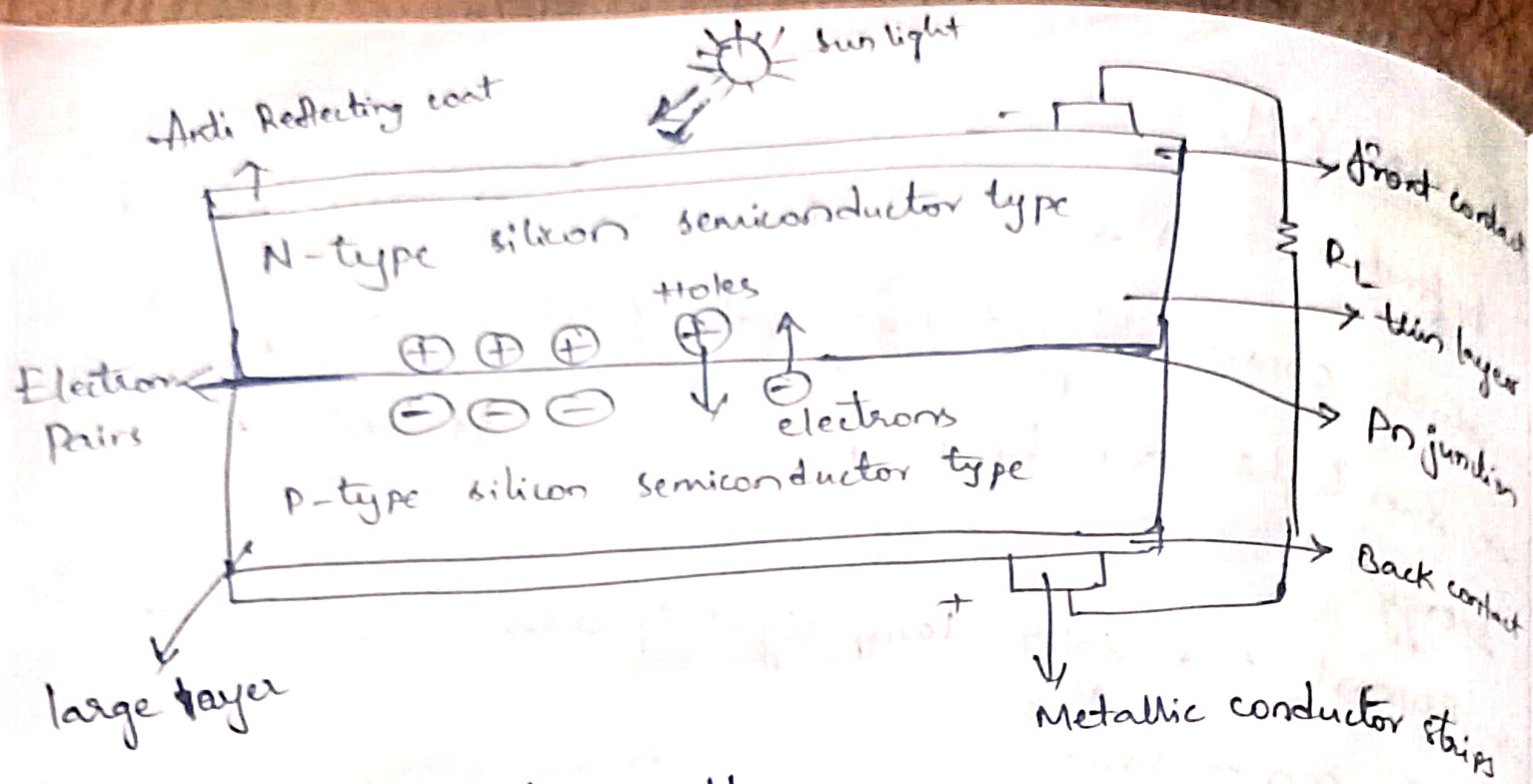
→ Here P-type is large layer.

→ N-type is thin layer because when light is incident on this solar cell that should be able to penetrate from light.

IV- N-type region to depletion region.

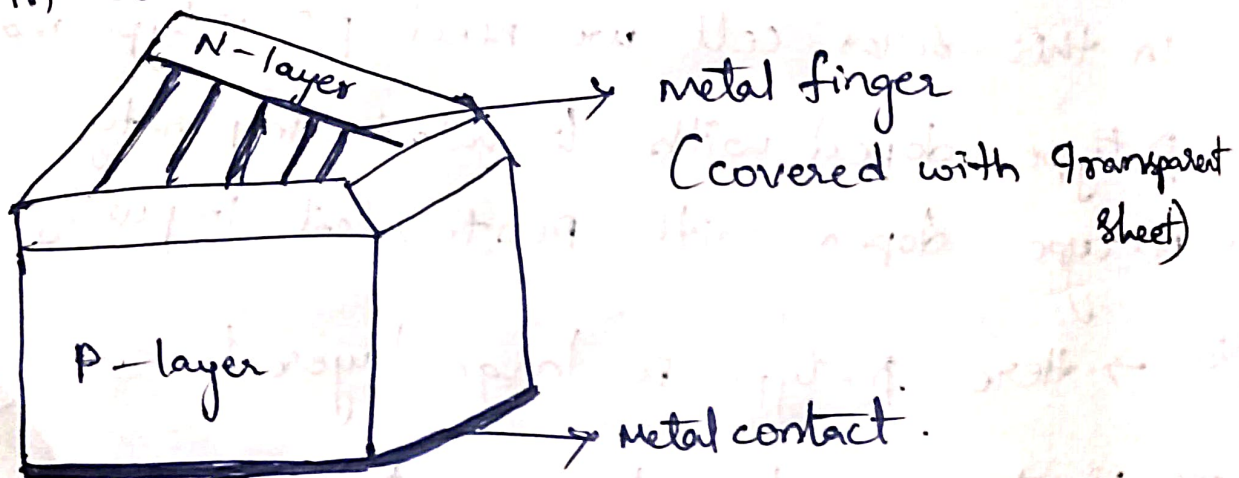
→ Now on N-type, metal finger is placed & P is made in contact to metal.



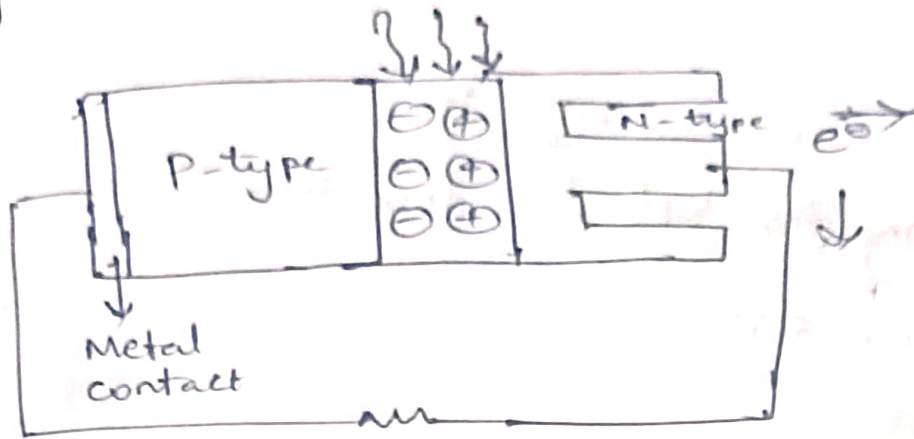


Solar cell

- Here p-type is large layer.
- N-type is thin layer because when light is incident on this solar cell that should be able to penetrate from light.
- N-type region to depletion region.
- Now on N-type, metal finger is placed & P is made in contact to metal.



Working:

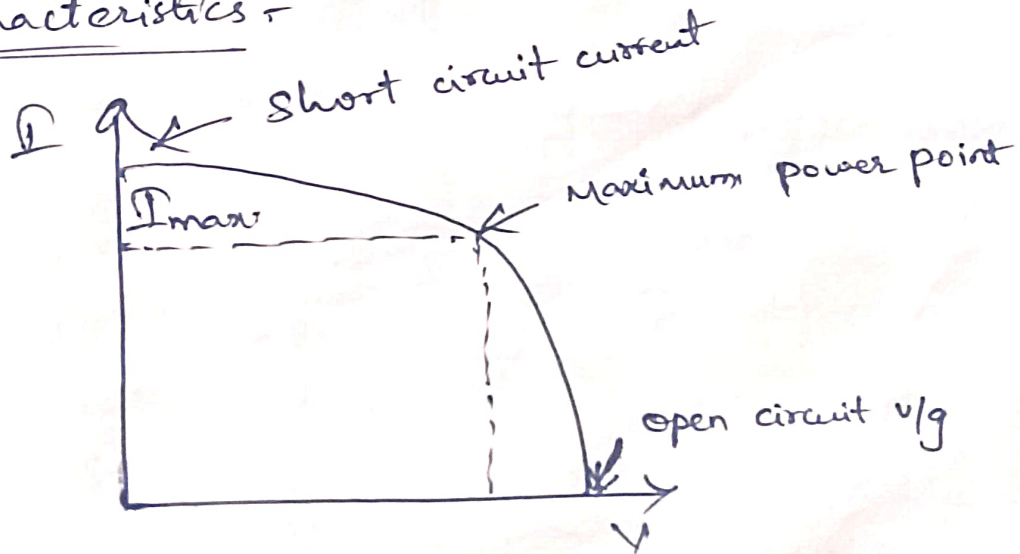


→ The depletion region will have neutral atoms when light falls on this region electron-hole pair generation takes place.

→ Before the pair of e^- & holes the electrical field that we have given will pull the holes towards P-side & electrons towards N-side.

→ As a result when electron moves from N-type to P-type voltage is produced.

V-I characteristics:



Advantages

- No pollution associated with it.
- It must ~~long~~ last for long time.
- No maintenance cost.

Disadvantages:

- It has high cost of installation.
- It has low efficiency.

Applications:

- Supply Electricity for telecommunication repeater stations, water pumps, voltages.



* Field Effect Transistors and Advanced Devices

FET : field effect Transistor

Introduction:

- The field effect transistor is an semiconductor device like a BJT.
- FET is also a three terminal device.
- The three terminal of FET are named as Drain (D), Source (S), and Gate (G) among the three terminals Gate terminal is a controlling terminal.

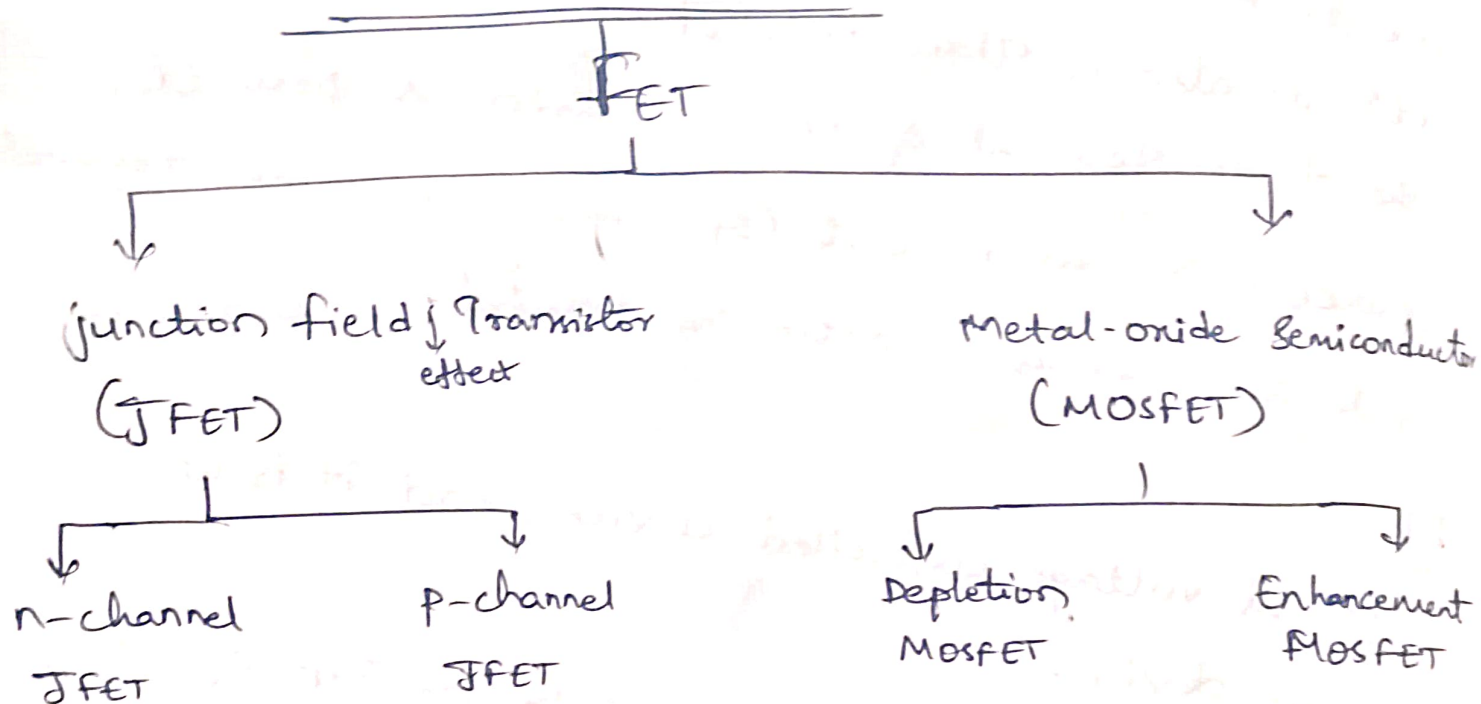
FET :

- It is voltage controlled device, and it is an unipolar device.
- Hence current is carried by only one type of charge particles either electrons or holes. This is called unipolar device.
- Here in BJT Base current controls collector current i.e., Base is i/p & collector is o/p.
- In FET Gate voltage controls drain current i.e., output current (Drain current I_d) is controlled by ^{input} Gate-to-source voltage (V_{gs}).

→ BJT → I_c is controlled by I_b
↓ o/p ↓ i/p

→ FET → I_d is controlled by V_{gs}
↓ o/p ↓ i/p

~~FET~~
FET's are classified into



JFET → Junction field transistor

MOSFET → Metallic oxide semiconductor field effect Transistor.

JFET (Junction field effect Transistor):

→ JFET is a voltage controlled, unipolar transistor where the current flowing from Drain (D) to source is controlled by the Gate-to-source voltage (V_{GS})

terminals of JFET:

- ① Gate (G) → controls the channel
- ② Drain (D) → carriers leave the channel
- ③ Source (S) → carriers enter the channel

→ It is two types of JFET transistor, one is n-channel and another one is p-channel JFET.

→ For an n-channel JFET transistor the arrow which represents the direction of Gate current moves towards the device.

→ For an p-channel JFET transistor the arrow which represents the direction of Gate current moves away from the device.

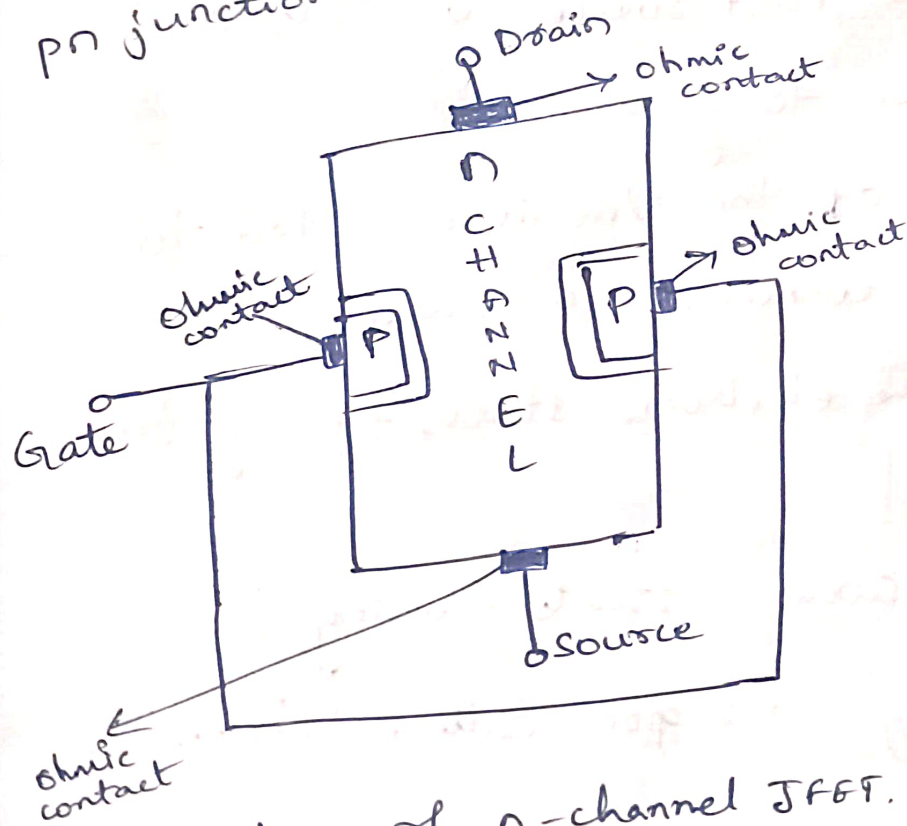
Types of JFET

① n-channel JFET

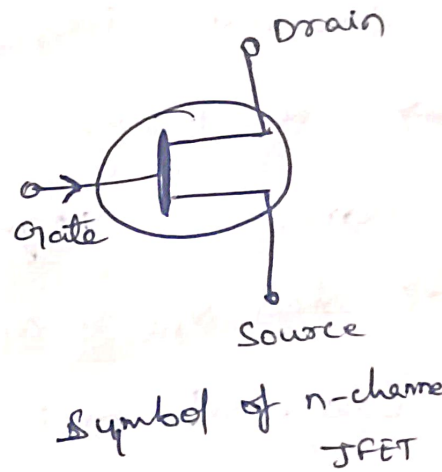
② p-channel JFET

① n-channel JFET :-

- An n-channel JFET contains an n-type material between the drain and source terminals.
- Two p-type materials are embedded along the metal contacts of the gate terminal.
- The presence of two p-type materials forms two pn junctions inside the JFET transistor.



Structure of n-channel JFET.



Working of an n-channel JFET transistor:-

Case (i) $V_{GS} = 0$ and $V_{DS} > 0$

→ Generally in JFET the p-n junction between gate & source is always kept in reverse biased

→ The Gate current $I_G \approx 0$. So V_{GS} is zero when V_{DS} is applied.

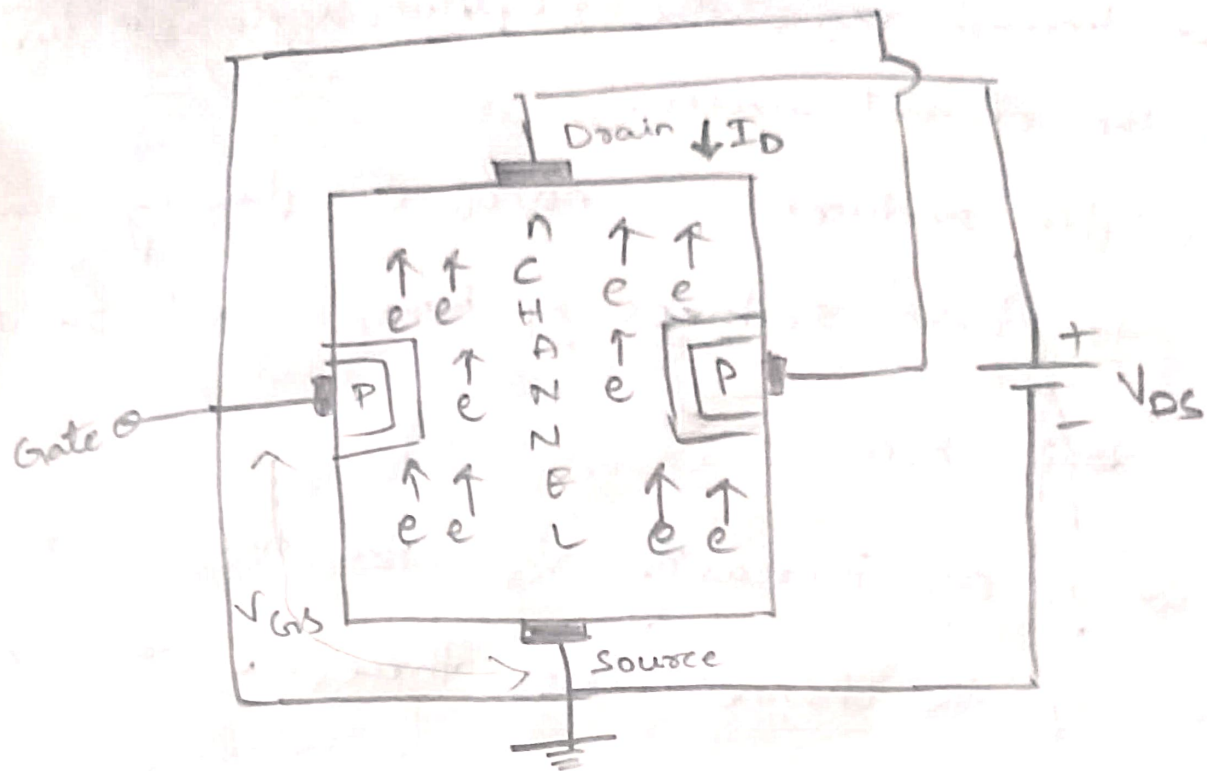
→ V_{GS} is zero the gate and source terminals are shorted i.e., connected to ground.

→ The positive terminal of the V_{DS} is connected to drain & negative is connected to source.

→ when V_{DS} is applied, the electrons start flowing from source to drain.

→ The majority charge carriers start flowing from source to drain through a region called 'channel'.

Channel :- The region b/w source & drain & also the Gate region is called 'channel'.



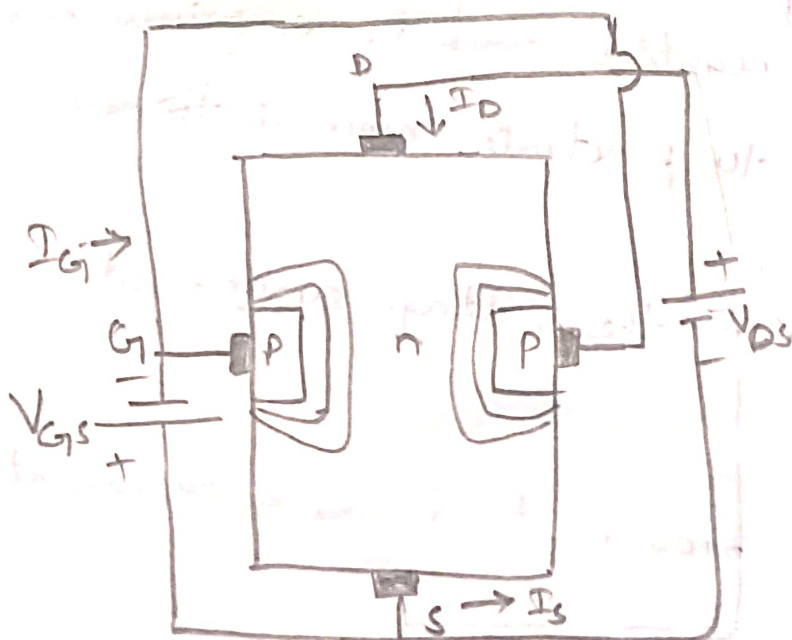
Case Cii) $V_{GS} = -ve$ and $V_{DS} > 0$

- The width of the channel can be controlled by varying the gate voltage.
- Since gate voltage is negative and is in reverse bias causes the depletion region to penetrate more into the channel.
- This penetration depends on the voltage applied at the gate.
- The depletion region is broad at drain & narrow at the source.
- In this case, the negative terminal of the V_{GS} is connected to gate and positive is connected to source.

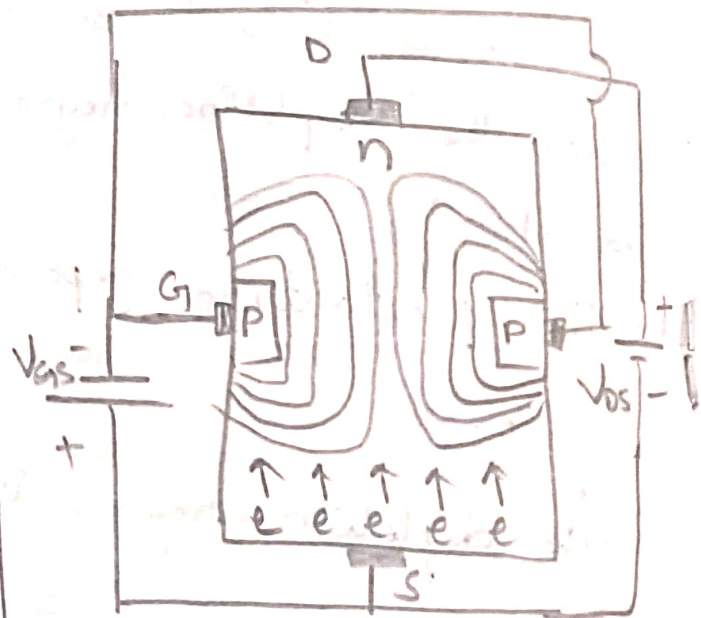
→ If we increase V_{GS} , the depletion region $\uparrow$ in turn reduces the channel width.
 → As width reduces the no. of e^- s flowing from source to drain reduces & hence current flowing from drain reduces. ($V_{GS} \uparrow$ D.R. $\uparrow$ width $\downarrow$ $I \downarrow$ $e^- \downarrow$)

→ If we go on increasing V_{GS} , the depletion region penetrates & the channel closes therefore the current I_D becomes zero.

→ As the devices are controlled by gate voltage it is called as voltage controlled device.

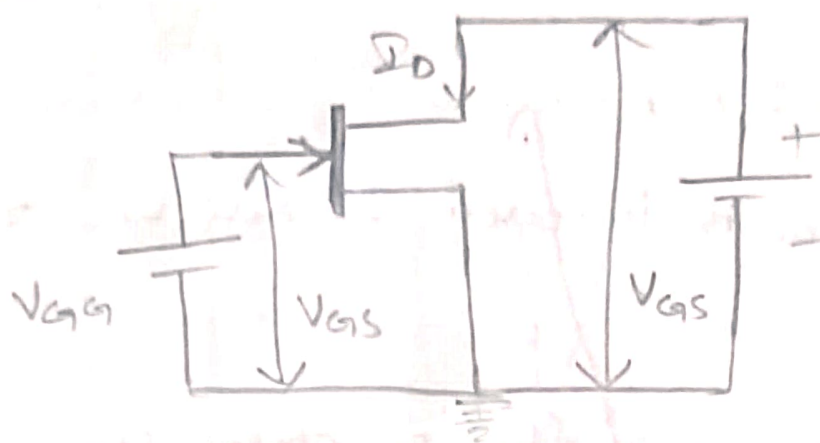


Small negative Gate voltage



Large negative gate voltage

V-I characteristics of FET (n-channel) :



Arrow indicate direction gate current.

The characteristics are classified into two they are drain characteristics and Transfer characteristics.

(i) Drain characteristics :

- The curve drawn between I_D (Drain current) and V_{DS} when $V_{GS} = 0$. The gate is shorted to source when $V_{GS} = 0$ there is no potential therefore $I_D = 0$.
- As V_{DS} increased the drain current I_D increases linearly upto point A that is Knee point.
- I_D increases with increase in drain to source voltage.
- Here drain is increased slowly as compared to ohmic region.
- Here there is an increase in V_{DS} , this in turn increases the reverse bias voltage across the gate junction.
- As a result of this depletion region grows in size thereby reducing the effective width of the channel.

→ All the drain to source v/g corresponding to point the channel width is reduced to a minimum value E_1 is

known as pinch off v/g

→ As further V_{DS} is increased the resistance r_d is increases.

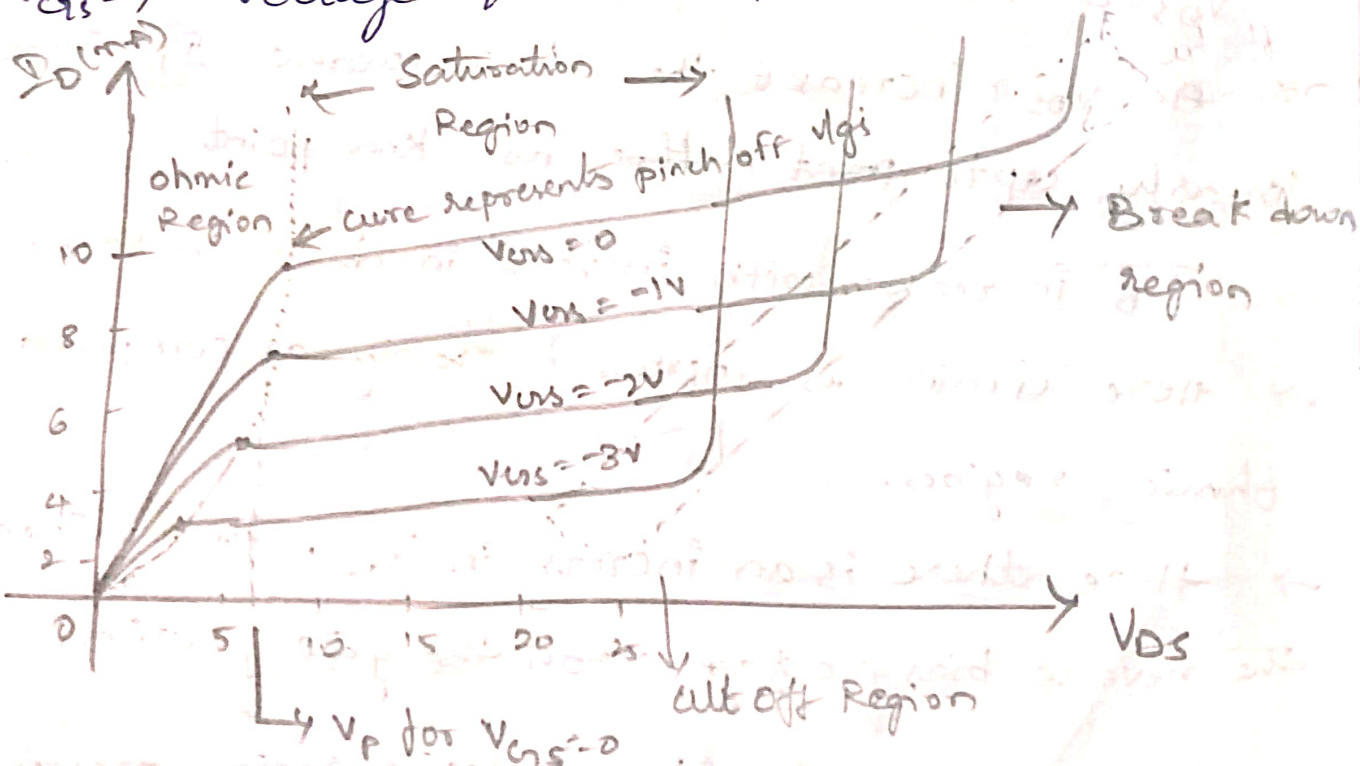
→ therefore there is no flow of charge carriers thus current becomes constant.

$$I_D = I_{DSS} \left[1 - \frac{V_{DS}}{V_P} \right]^2$$

I_{DSS} = Drain current when gate is shorted to source

I_D → Drain current

V_{GS} → voltage b/w Gate & Source.



Three regions in Drain characteristics

- ① Ohmic or Linear Region.
- ② Saturation (Active) region.
- ③ cut-off region

① Ohmic region :-

- when V_{GS} small, the I_D (drain current) increases linearly with V_{GS} .
- The JFET behaves like a resistor.
- channel is fully open.

② Saturation region :-

- As V_{GS} ↑'s, the depletion regions widen, narrowing the channel.
- After a point called $V_{GS}(sat)$ or pinch off V/G (V_P), the curve flattens.
- Here I_D becomes almost constant, if V_{GS} ↑'s, current does not ↑'s much.
- Device works as constant - current source.

③ cut-off Region :-

- when V_{GS} is too negative, the device turns off. $I_D = 0$
- $I_D = 0$
- This happens around $V_{GS} = V_{GS}(off)$.

* Break-down region

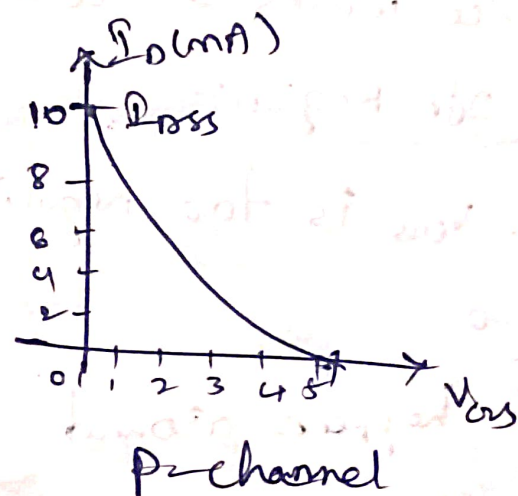
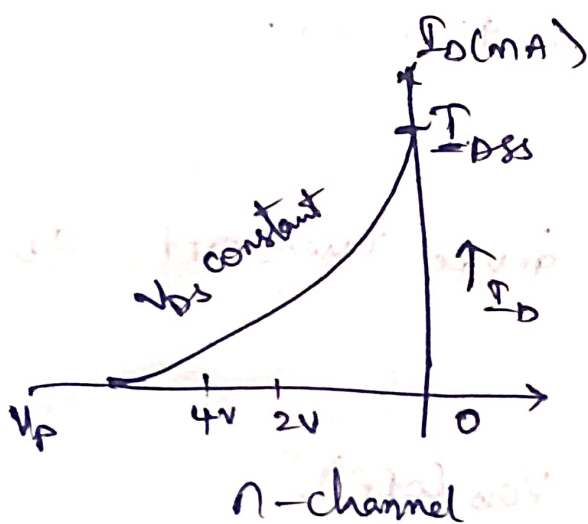
At $V_{DS} \uparrow$ beyond a certain point, the gate-channel junctions can break down, causing a rapid $\uparrow$ of I_D & destruction $\uparrow$ in drain current.

* Transfer characteristics

$\rightarrow$ This is the curve drawn b/w drain current I_D versus gate to source V_{GS} for constant value of V_{DS} .

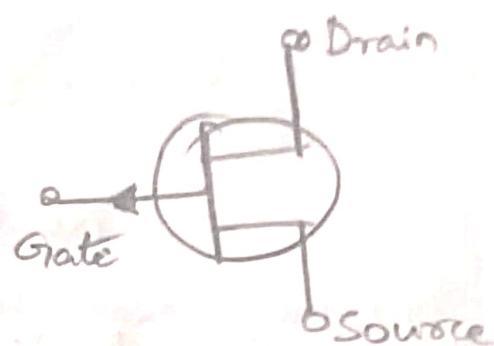
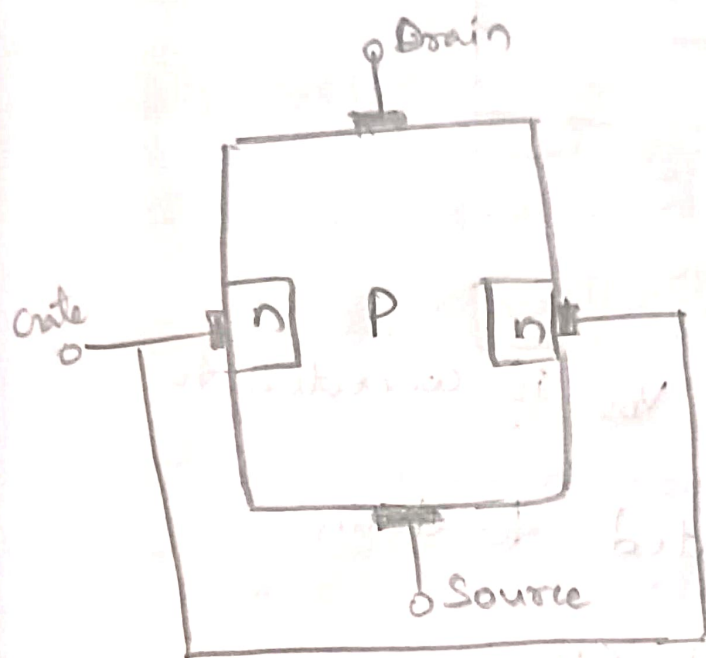
$\rightarrow$ When $V_{GS} = 0$, $I_D = I_{DSS}$ is maximum when $V_{DS} = V_D$ the current $I_D = 0$ this characteristics follows Schottky equation.

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2$$



* channel JFET :

A p-channel JFET contains a p-type material b/w the drain and source terminals. Two n-type materials are embedded along the metal contacts of the gate terminal. The presence of two n-type junctions forms 2 pn junctions inside the JFET transistor.



Symbol of p-channel JFET

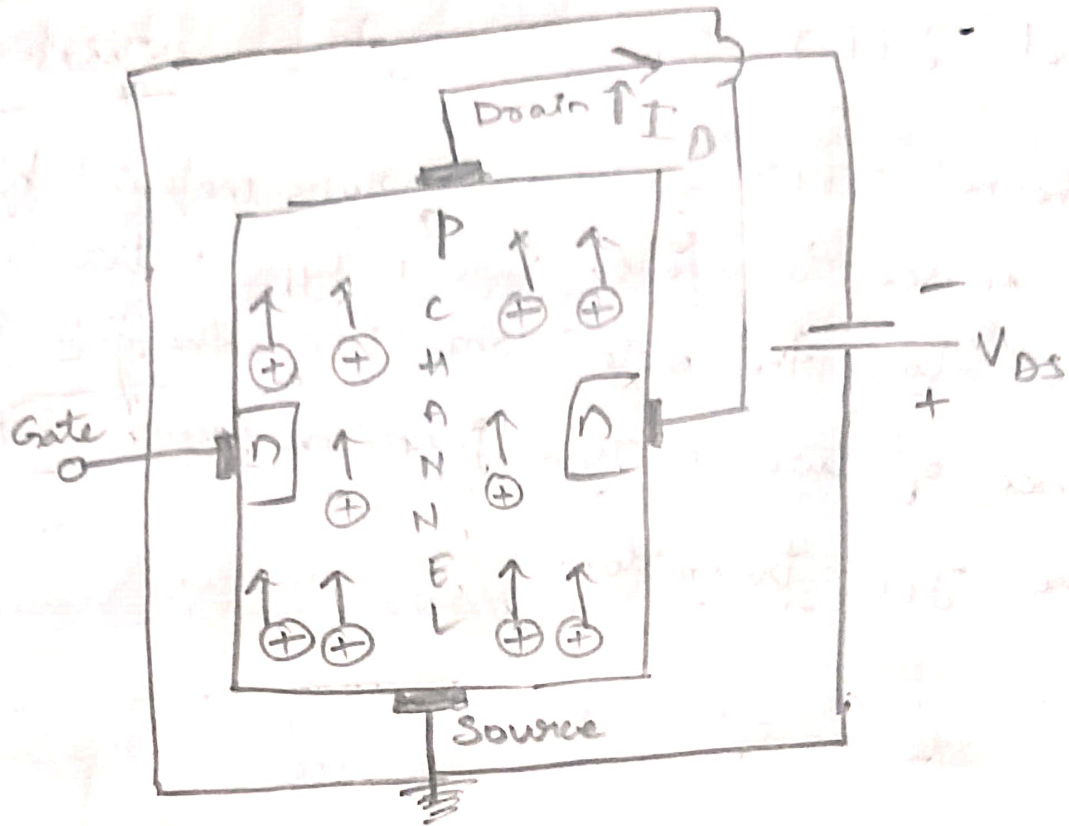
Structure of p-channel JFET

working of a p-channel JFET transistor :

Case (i) $V_{GS} = 0$, $V_{DS} \leq 0$

→ As V_{GS} is zero the gate & source and terminal are shorted i.e. connected to ground.

→ The positive terminal of V_{DS} is connected to source & negative is connected to drain.

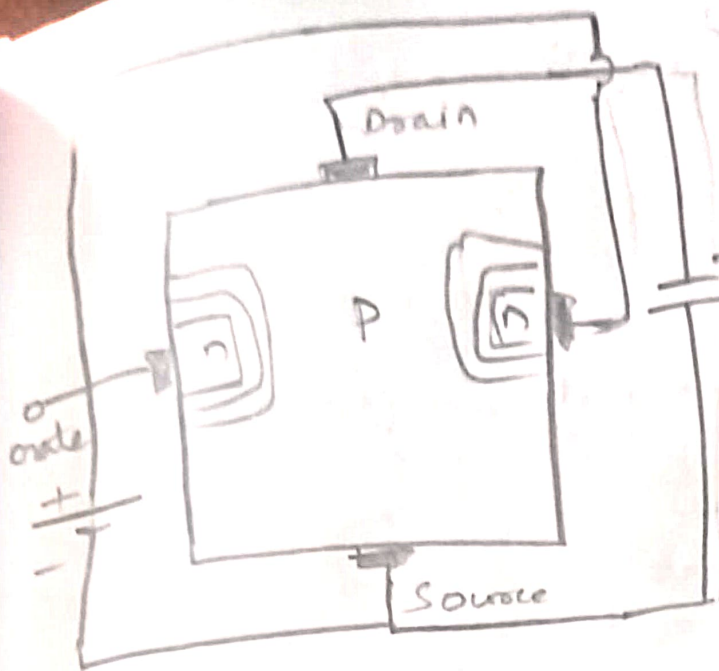


No bias voltage

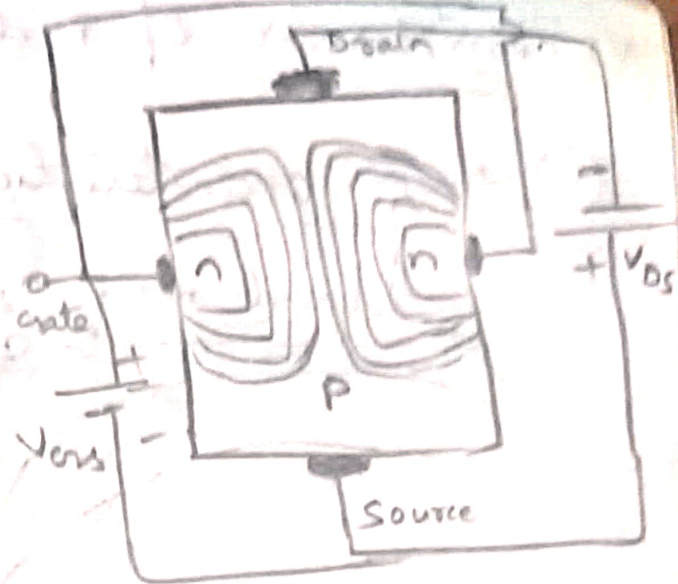
→ The positive terminal of the V_{DS} is connected to source & negative is connected to drain

Case (ii) $V_{GS} = +ve$ and $V_{DS} < 0$

→ In this case, the negative terminal of the V_{DS} is connected to source & positive is connected to gate. Similarly, the positive terminal of V_{DS} is connected to source & negative is connected to drain.



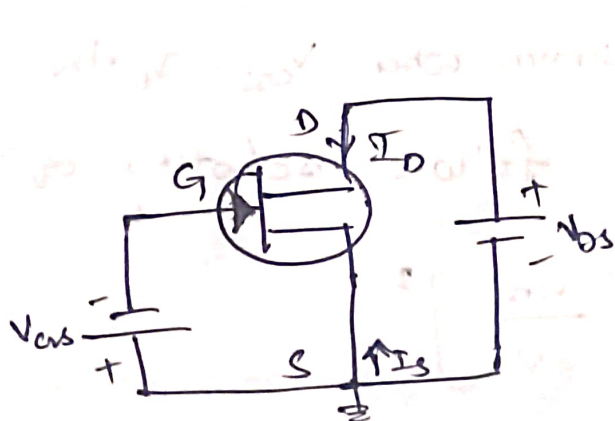
Small positive gate v_g



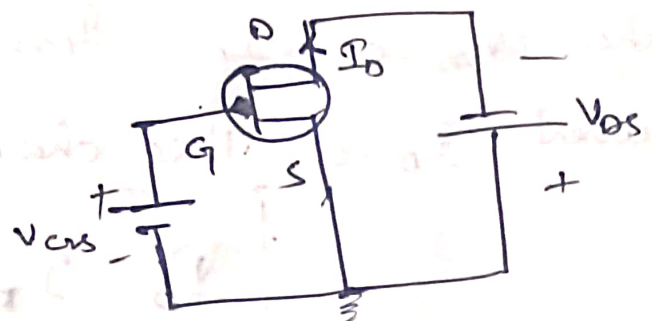
large positive gate v_g

Note: The working of the p-channel JFET will be similar to that of n-channel JFET except 'holes' will be the current carriers instead of 'Electrons'.

Circuit symbols for both N-channel & p-channel JFET



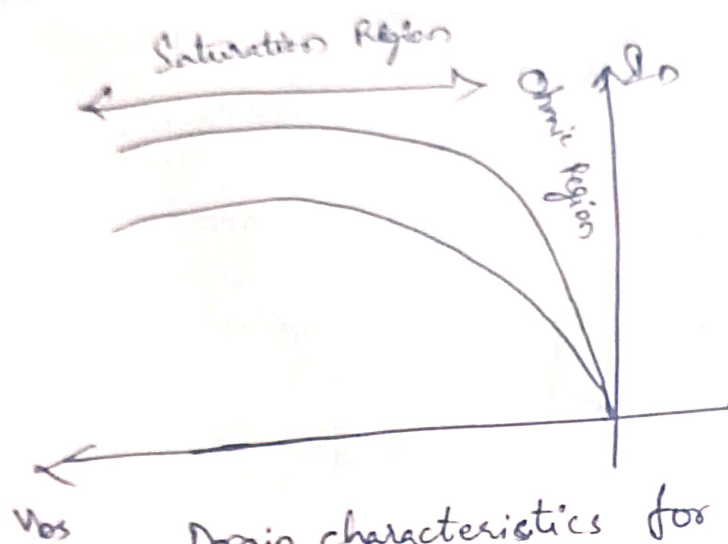
N-channel JFET



P-channel JFET

V_D characteristics of p-channel

① Drain characteristics



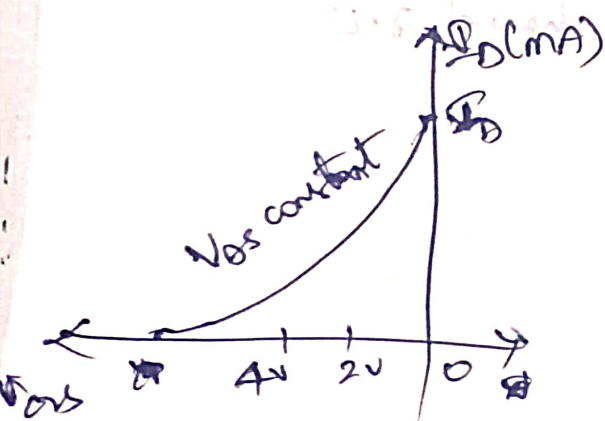
Drain characteristics for p-channel JFET.

② Transfer characteristics

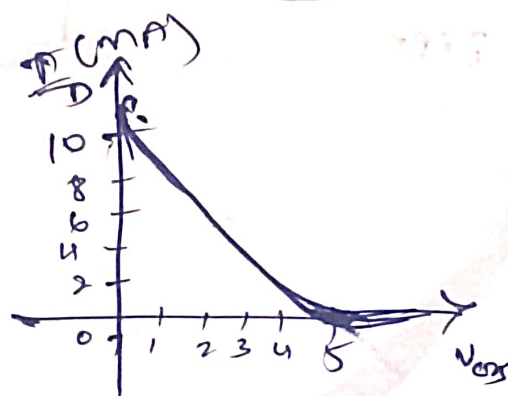
This is the curve drawn b/w drain current I_D versus gate to source V_{GS} for constant value of V_{DS} .

When $V_{GS} = 0$, $I_D = I_{DSS}$ is maximum when $V_{GS} = V_P$ the current $I_D = 0$. This characteristics follow Schottky eqⁿ.

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2$$



n-channel



p-channel

FET parameters:

The main parameters of a FET when connected in common source are.

① Ac drain resistance: $r_d = \frac{\Delta V_{DS}}{\Delta I_D} \Big|_{V_{GS} \text{ constant}}$

This is resistance b/w drain & source terminals.

② Transconductance: The control that the gate has over drain is measured by forward conductance g_f (or) mutual conductance g_m .

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \Big|_{V_{DS} \text{ held constant}}$$

③ Amplification factor: The Amplification factor is denoted as μ .

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \Big|_{I_D \text{ held constant}}$$

* The relation b/w μ , r_d & g_m

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D}, \quad g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

W.K.T $\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}$ rewrite as $\frac{\Delta V_{DS}}{\Delta V_{GS}} \times \frac{I_D}{I_D} \Rightarrow \frac{\Delta V_{DS}}{I_D} \cdot \frac{I_D}{\Delta V_{GS}}$

$\downarrow \quad \downarrow$
 $r_d \quad g_m$

$$\boxed{\mu = r_d \times g_m}$$

* MOSFET = Metal oxide semiconductor - field

effect Transistor :-

→ A MOSFET is a voltage-controlled device used for switching & Amplification.

→ It is similar to JFET, but Gate never touches the channel → gate is insulated by a thin oxide layer (SiO_2).

→ Because of this, Input current is almost zero.

Types of MOSFET:

① Depletion MOSFET ② Enhancement MOSFET.

→ For both has N-channel & P-channel.

① Depletion MOSFET :-

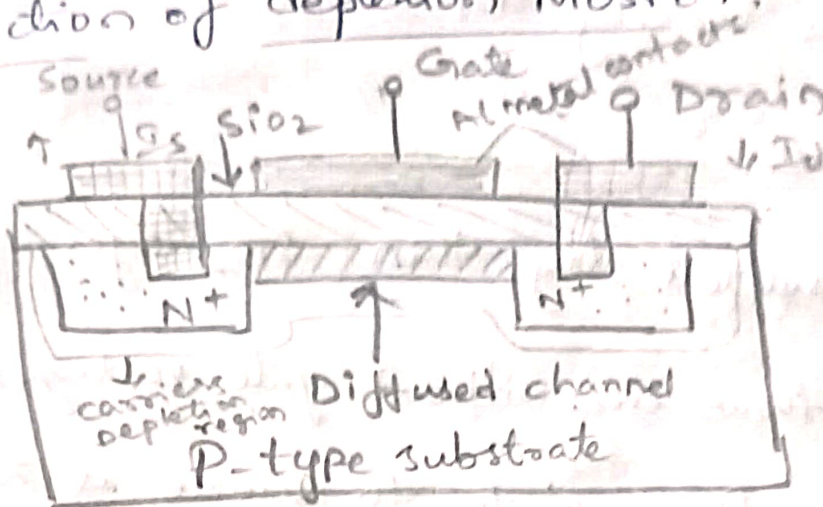
→ The MOSFET has only one P-region which is called substrate and is denoted by SS.

→ The gate insulated from conducting channel by a metal oxide oxide SiO_2 .

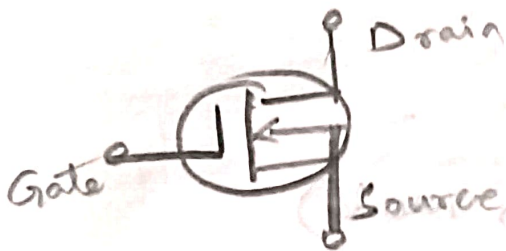
→ In MOSFET both positive & negative voltages are applied on the gate.

- when negative V_g is applied it acts as depletion MOSFET.
- when positive V_g is Applied it acts as Enhancement MOSFET.

Cross section of depletion MOSFET:



It consists of a lightly doped p-region called substrate into which two lightly doped N-regions are diffused they act as source & drain.



N-channel MOSFET

- A depletion MOSFET can work in both electrons & depletion mode (normally on) and enhancement mode.
- Types
- ① N-channel depletion MOSFET
 - ② P-channel depletion MOSFET

→ Here N-channel is most commonly discussed.

Construction:

N-channel depletion MOSFET:

→ N-channel is heavily doped, & N-channel b/w drain & source.

→ Gate is insulated by thin SiO_2 layer.

→ The current flows even without gate voltages.

→ when voltage from gate to source is zero it is normally on state & channel is formed already.

Working:

① $V_{GS} = 0$

it is normally on at $V_{GS} = 0$

② when $V_{GS} = -ve$ (depletion mode)

→ Applying $-ve$ V_G to gate is electrons gets repels.

because gate is $(-ve)$ & electrons also $(-ve)$, so both

can repels. (pushes) them away from the gate).

→ so, width of channel is increases, Current I_D decreases
removing carriers.

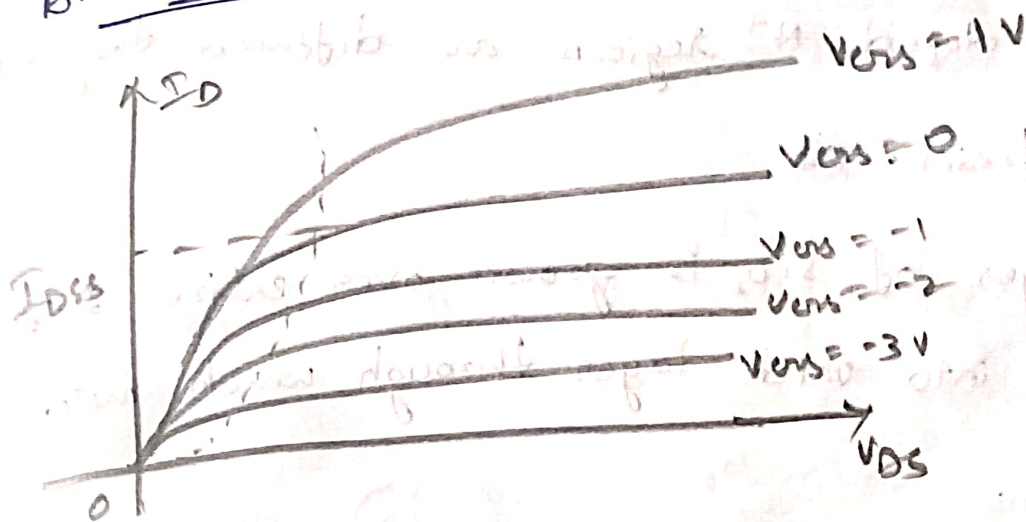
→ Depletion region is increases.

② Enhancement mode ($V_{GS} = +ve$)

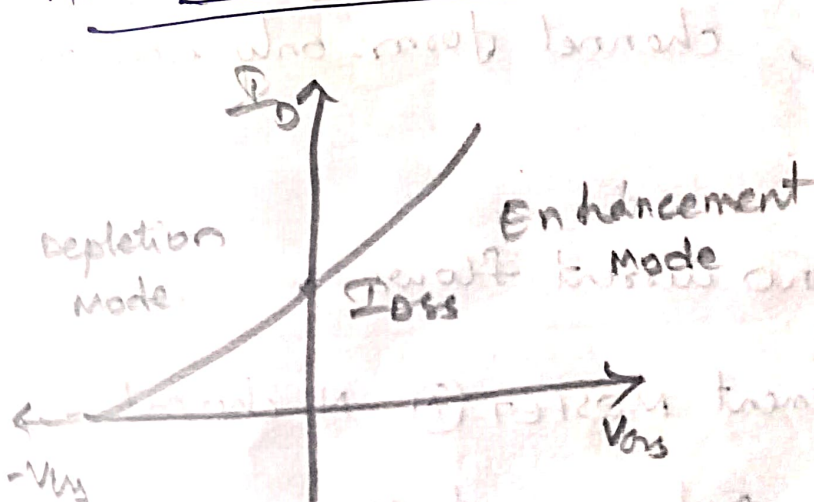
- Apply +ve V_G at gate is attracts more electrons
- so it is towards the gate.
- so, the channel becomes increase or wider, &
- current I_D increases. so it is adding carriers.

characteristics:-

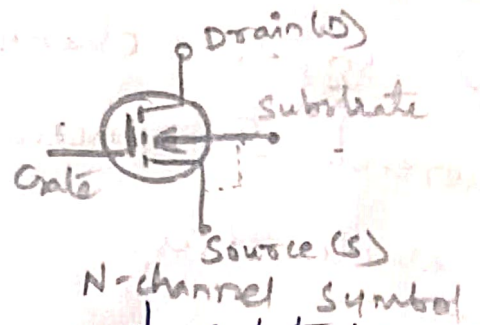
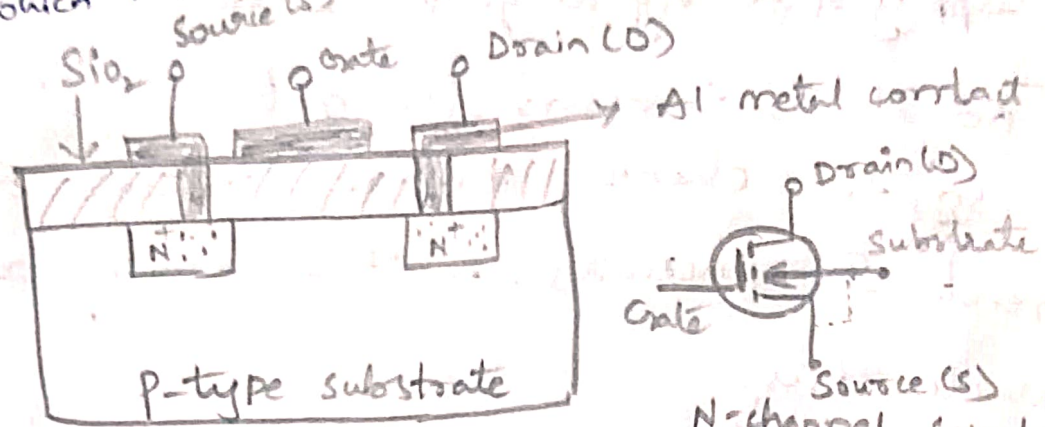
Drain characteristics:-



Transfer characteristics:-

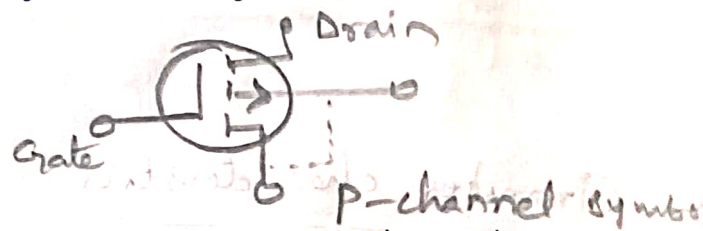


* Enhancement MOSFET :- An Enhancement MOSFET is a type of MOSFET in which the channel does not exist.



→ This consists of lightly doped p-type substrate into which two highly doped N^+ regions are diffused they act like source & drain. No

→ Now a thin layer of SiO_2 is grown over entire surface & holes are cut into oxide layer through which metal contact are made.



Working & construction :-

→ channel does not exist, channel forms only when you apply gate voltages (V_{GS}).

→ without gate voltages, no current flows.

→ Two types of Enhancement MOSFET (1) N-channel enhancement (2) p-channel Enhancement MOSFET.

① N-channel enhancement :-

→ channel forms when V_{GS} is +ve

② P-channel enhancement :- channel forms when V_{GS} is -ve.

→ The semiconductor channel & the SiO_2 layer of the gate form a parallel plate capacitor.

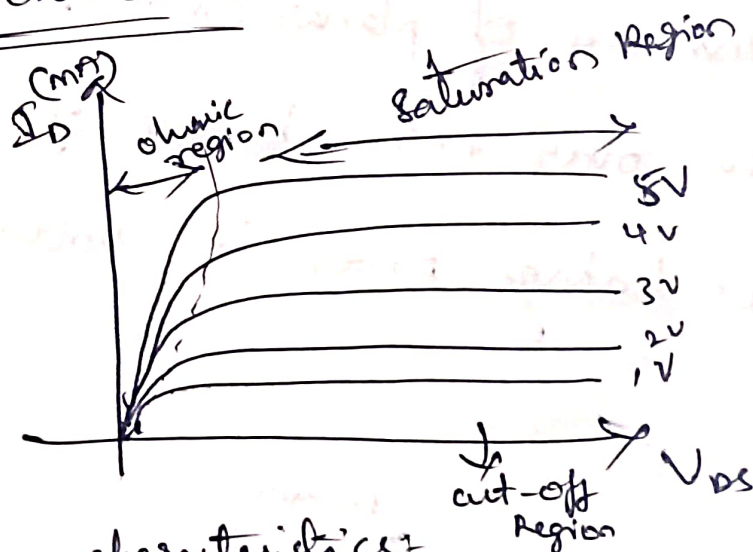
→ when positive potential is applied at gate, with respect to substrate negative charges are induced on p-type substrate consists of e^- & form an inversion layer the inversion layer form an effective N-type channel.

→ Increased the magnitude of induced negative charges in semiconductor increases.

→ Thus the conductivity is increased as the current is enhanced due to positive V_g thus called Enhancement

MOSFET.

Drain characteristics:-

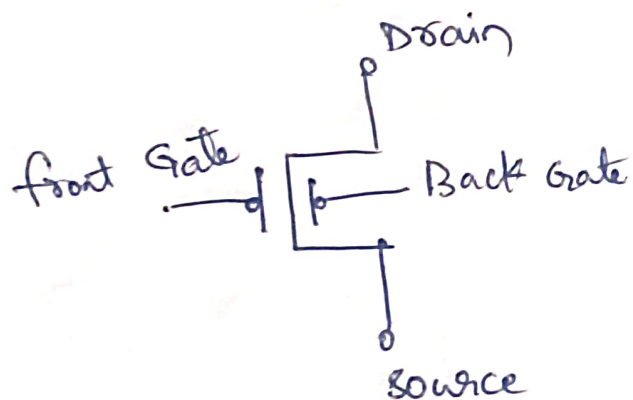


Transfer characteristics

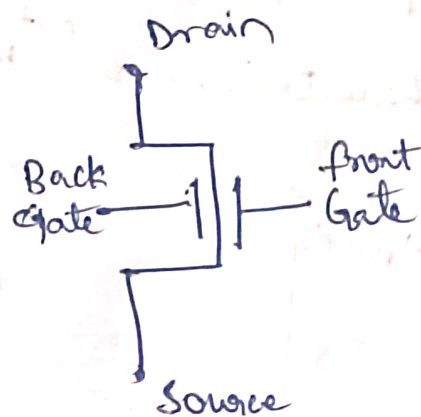


* FinFET - Fin field effect Transistor :-

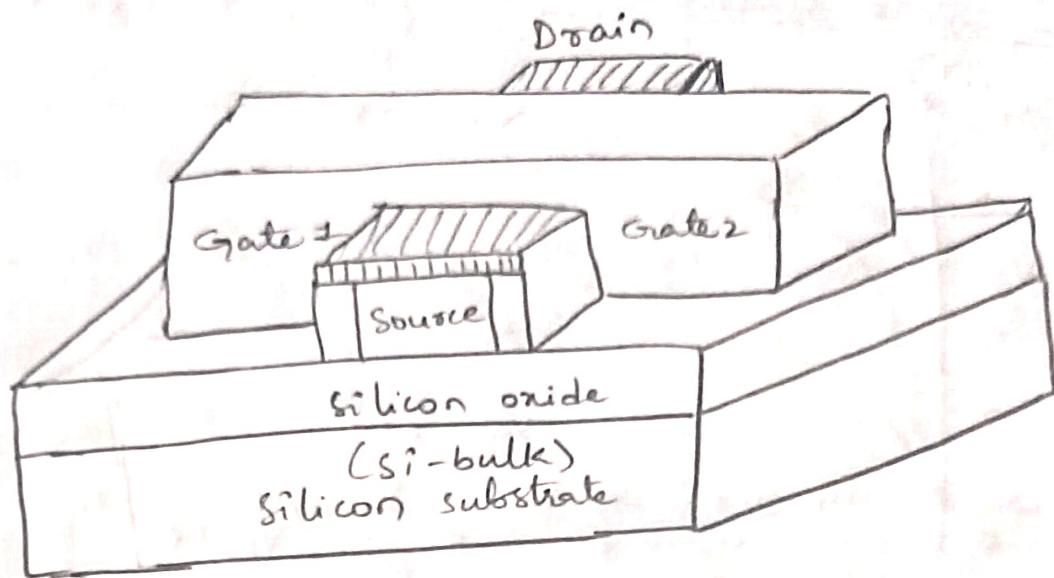
- The finfet (fin field effect transistor) process is a 3D process adopted to overcome the limitations of conventional planar (2D) structures.
- The structure looks like a fish's fin, hence the name is FinFET.
- In a transistor, when V_g is applied to a gate, current flows through a channel from a 'Source' to 'Drain'.
- It is a 3D transistor & widely used in Integrated circuits recently instead of planar CMOS finfet.
- It is used more than other FETs because of its area of performance, lower leakage power, low voltage operation,



P-finfet



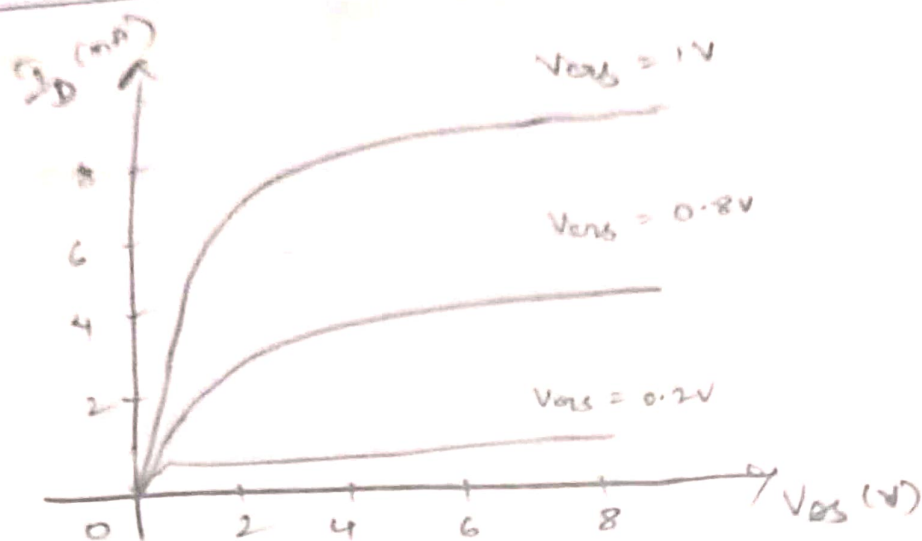
N-finfet



Structure of FINFET

- Working:-
- when gate V_g is applied an Inversion layer forms around the fin.
 - Gate is covers the fin from multiple sides.
 - fin is vertical silicon channel.
 - source & drain is on either side of the fin & substrate or Body is thin fin improves electrostatic control.
 - Here since the gate controls the channel from multiple sides, it can turn the devices ON/OFF more effectively.
 - This reduces leakage & improves performance at low voltages.

V-I characteristics of FinFET:



→ The drain current increases when the drain source v/g is applied.

→ Initially it increases linearly & after that it enters into saturation region where the curve is almost most.

Advantages of finFET:

- low power consumption
- operates at lower v/g
- operating speed is higher.
- lower leakage current

Disadvantages:

- more complex fabrication
- Higher manufacturing cost
- Design complexity.

Applications:

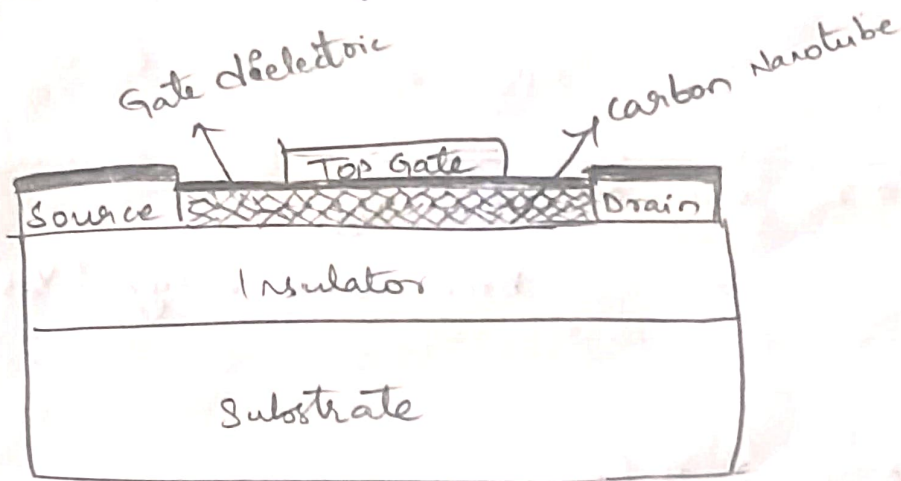
- Modern processors (Intel, AMD, Apple)
- Mobile SoCs
- High-performance & low power ICs.

* CNTFETs:

carbon nanotube field effect Transistor:

- carbon nanotube field-effect transistors (CNTFETs) are advanced devices that use semiconducting carbon nanotubes as the channel material.
- It is a type of transistor that uses a carbon nanotube (CNT) as the channel instead of silicon.
- It is similar to MOSFET, but with a CNT channel
- Source supplies carriers
- Drain collects carriers
- Gate controls current
- Carbon Nanotube acts as the channel
- Gate oxide insulates gate from CNT.

Working:



Structure of CNTFET

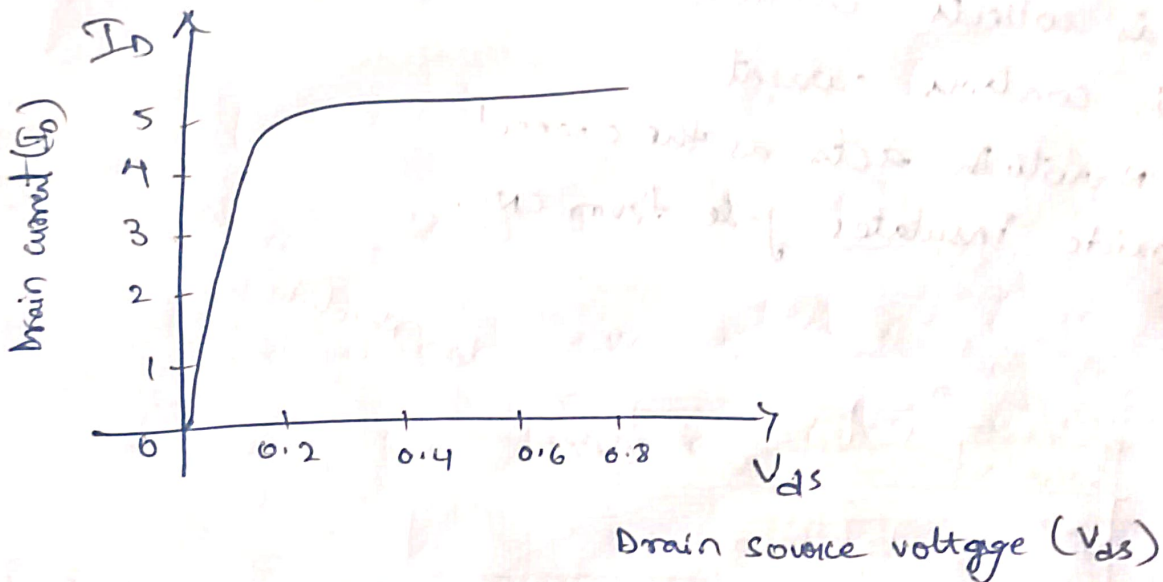
- when gate voltage (V_g) is applied, positive gate applied CNTFETs conducts electrons.
- when negative gate applied, CNTFETs conducts holes and drain current increases.

→ when gate voltage V_g is applied, the electric field controls carrier flow in the CNT.

→ If $V_g > \text{threshold voltage } (V_t)$ then channels forms the current flow.

→ If $V_g < \text{threshold voltage } (V_t)$ then, channels gets 'OFF' no current flow.

V-I characteristics:-



Advantages:-

→ ultra-fast switching

→ Extremely low power.

→ Excellent scaling below 5nm

* Disadvantages:

- CNT Alignment Issues.
- Metallic CNT problem
- High fabrication cost.

Applications:

- Nanoelectronics
- High-speed processors
- Low-power ICs
- Future VLSI technology
- Flexible Electronics.

* Ballistic Transport:

→ Definition:

→ Ballistic transport ^{In CNTFET} is the motion of charge carriers (Electrons or holes) from source to drain without scattering due to phonons impurities or lattice defects.

→ Ballistic occurs when, channel length (L) is less than mean free path of the electron (λ_m) then the transport of electron is called ballistic transport.

→ And we expect that no collisions will take place.

→ In CNTFETs, the carbon nanotube channel length is very small.

(L) channel length $<$ mean free path (L_m) or (λ)

→ Here mean free path (λ) or (L_m) is the Average distance a carrier travels without collision.

→ If $L < \lambda$ carriers reach the drain without scattering.

conditions of Ballistic transport:

① $L < L_m$ & ② $L < L_\phi$

where $L \rightarrow$ length of the conductor

(L_m) or (λ) $\rightarrow$ Mean free path

$L_\phi \rightarrow$ length over which an e^- can travel

before having an Inelastic collision.

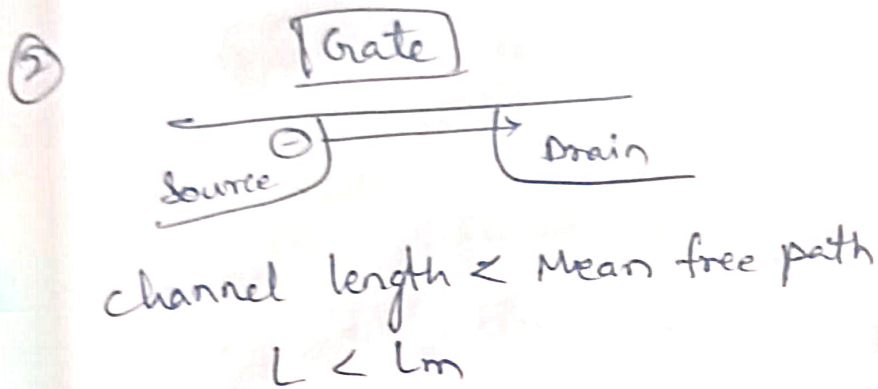
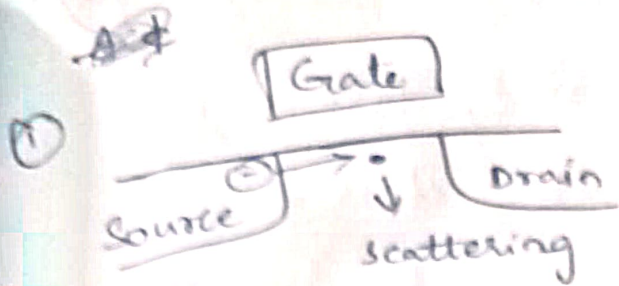
→ Ballistic transport occurs over very small length scales

& is obviously coherent.

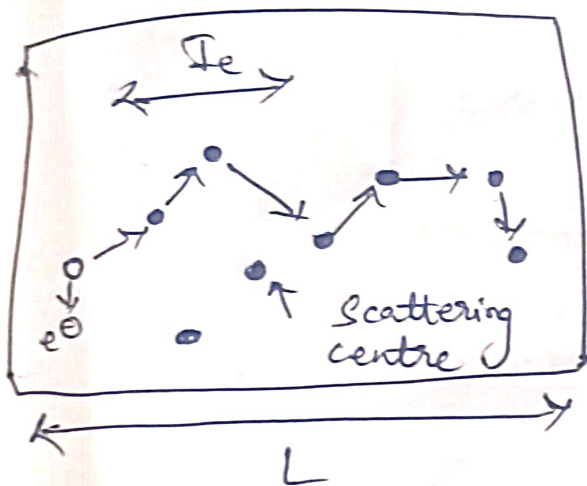
→ The e^- doesn't hit anything as it travels through the material & therefore, there is no momentum or phase

relaxation.

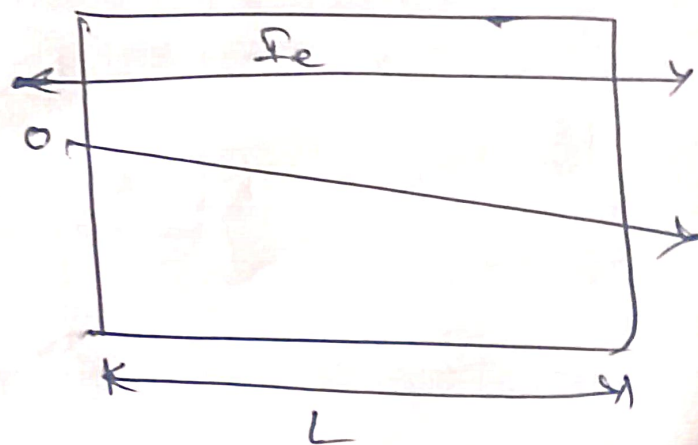
→ Thus, in Ballistic material, the e^- 's wave function can be obtained from Schrodinger's Equation.



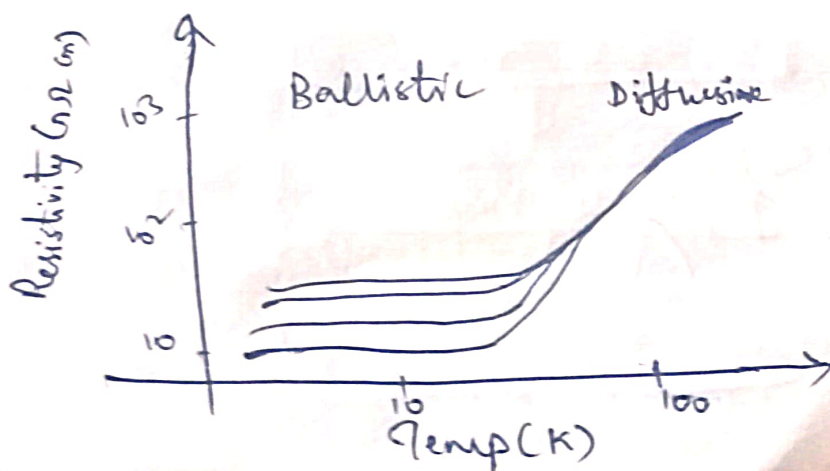
③ Diffusive transport



④ Ballistic transport



V-I characteristics:-



Advantages:

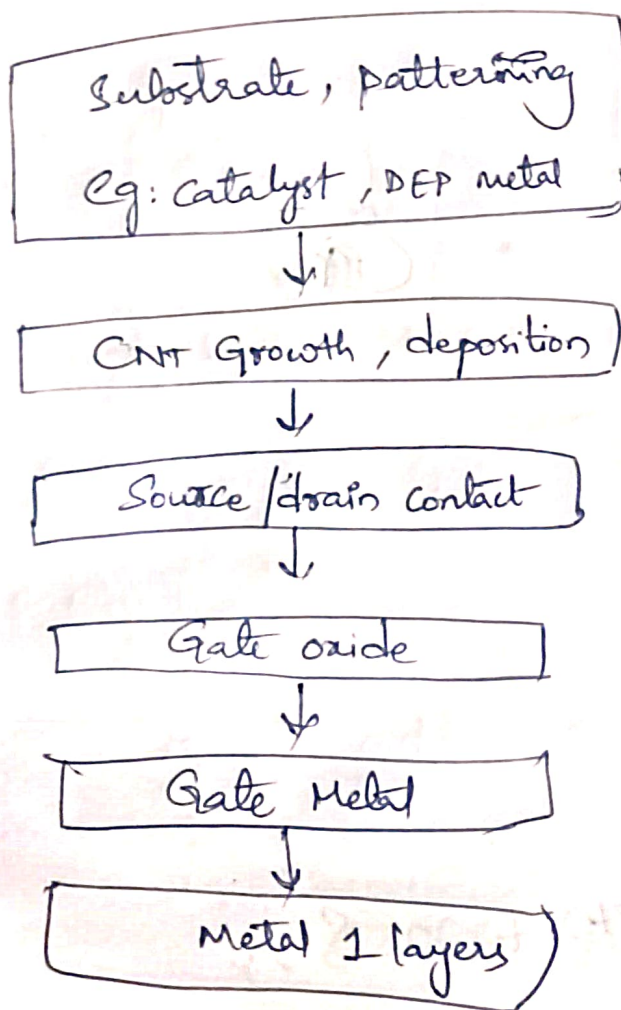
- Very high speed
- Low power dissipation
- High drain current
- Temperature Insensitivity

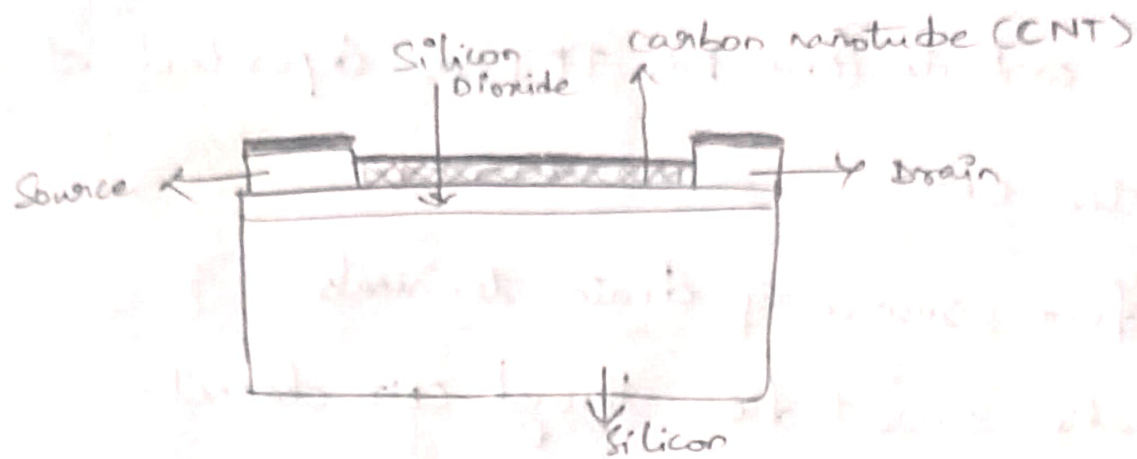
Disadvantages:

- Difficult to Achieve practically.
- fabrication challenges
- Not suitable for large devices

* Fabrication of CNTFET :-

→ The fabrication of CNTFETs typically involves several steps, combining advanced material synthesis with established semiconductor processing techniques.





① Substrate preparation:-

- A Silicon (Si) wafer is taken as the substrate.
- A thick SiO_2 layer is grown on it for insulation.

② Catalyst Deposition:-

- A thin layer of metal catalyst [Fe , Co , or Ni] is deposited on selected areas.
- This is done using photolithography.
- Catalyst is required for the growth of carbon nanotubes.

③ CNT Growth

- CNT are grown using chemical vapor deposition (CVD).
- CNT acts as the channel of the CNTFET.
- It provides ballistic or near-ballistic transport.

④

④ Source and drain formation:-

- Metal contacts (Au, Pd, Ti) are deposited at both ends of the CNT.
- These form source & drain terminals.
- It enables current flow through CNT channel.

⑤ Gate oxide formation:-

- A thin high-K dielectric material (HfO_2 , Al_2O_3) is deposited over CNT.

- It insulates Gate from CNT

✳

⑥ Gate Electrode formation:-

- Gate material (metal or polysilicon) is deposited & patterned.
- It controls the conductivity of CNT channel.
- It can be top Gate, bottom Gate or wrap-around gate.

⑦ Metallization & passivation:-

- Metal Interconnections are added. ✳
- Final protective layer is deposited.
- It connects device to circuit & protects it.

Comparison of CMOS, FinFET, and CNTFET

Aspect	CMOS (planar MOSFET)	NARROW FinFET	CNTFET (Carbon Nanotube FET)
Structure	planar 2D structure, single gate	3D fin-shaped channel, multi-gate	carbon nanotube channel with surrounding gate
Channel material	Silicon	Silicon	Semiconducting CNTs
Gate control	single gate	Double / tri-gate	Excellent - wrap around control
Electrostatic control	Moderate	Strong	Very strong
Short channel effects	High	Reduced	Very low
Sub-threshold Swing	70-90 mV/dec	65-80 mV/dec	≈ 60 mV/dec
Mobility	Moderate	High	Very high
ON current	low-moderate	High	Very high
OFF current	High leakage	High low leakage	Extremely low
Power consumption	High	Low	ultra-low
Operating speed	Moderate	High	Very high
Heat dissipation	Good	Moderate	Excellent
Threshold v/g control	less precise	Better	Very precise
Reliability	High (mature)	Good	Depends on CNT
Manufacturing cost	low	High	very high
Applications	General Electronics	Processors, GPUs, SoCs	Future nanoelectronics.