ELECTRONICS & COMMUNICATION ENGINEERING

B.Tech. II Semester **L/T/P/C**
3/0/0/3

SEMICONDUCTOR DEVICES AND CIRCUITS

Pre-requisite: Fundamentals of Semiconductors.

Course Objectives:
To introduce the concepts of various semiconductor devices like Diodes, Transistors, FET's and MOSFET'S and advanced semiconductor technologies like FinFETs and CNTFETs. Emphasis is placed on developing a strong foundation for analog circuit design and understanding modern device technologies in electronics. To impart the knowledge of various configurations, characteristics and applications of electronic circuits.

Course Outcomes: After this course, the student will be able to

CO1: Acquire the knowledge in semiconductor materials and analyze the complete internal structure of PN junction its capacitances and resistances.
CO2: Design the circuits for the conversion of AC to DC Voltages.
CO3: Acquire knowledge in the structure of Transistor and evaluate different types, operation, characteristics and applications
CO4: Design the dc bias circuitry of BJT.
CO5: Acquire the knowledge and analyze the structure of, FET, MOS (different types, operation, characteristics and applications),FIN FET,CNTFET

Course Articulation Matrix

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	3	3	2	2	1	1					
CO2	3	3	2	2	1						
CO3	3	3	3	2	1						
CO4	3	3	3	2	2						
CO5	3	3	2	2	2	1					

UNIT I

Introduction to semiconductor physics: Formation of P-type and N-type semiconductors, principle and operation of Diode, Volt-Ampere characteristics, Current components in a p-n Diode, Diode equation, Temperature dependence, Static and dynamic resistances, Equivalent circuit, Load line analysis, Diffusion and Transition Capacitances, Break down mechanisms in Diode,

Special Purpose Diodes: Zenar Diode Volt-Ampere characteristics, Zenar Diode as a Regulator.Principle of Operation of – SCR, Tunnel Diode, Varactor Diode, Photo Diode, Solar Cell, LED and Schottky Diode

UNIT II

Rectifiers and Filters: P-N junction diode as a Rectifier - Half Wave Rectifier, Full Wave Rectifier, Bridge Rectifier, Harmonic components in Rectifier Circuits, Filters – Inductor Filters, Capacitor Filters, L- section Filters, π- section Filters(Qualitative treatment).

UNIT III

Bipolar Junction Transistor (BJT): Principle of Operation, Transistor current components, Transistor as an Amplifier, Common Emitter, Common Base and Common Collector configurations and their Characteristics.

UNIT IV

Transistor Biasing and Stabilization - Operating point, DC Load line, Biasing - Fixed Bias, Collector to Base Bias , Collective and Emitter Feedback Bias, Self bias, Bias stability, Stabilization against variations in V_{BE}, Ico, β, Bias Compensation using Diodes and Transistors.

UNIT V

Field Effect Transistor (FET): Construction, Principle of Operation, Pinch-Off Voltage, Volt-Ampere Characteristic, Comparison of BJT and FET.

Metal Oxide Semiconductor Field Effect Transistor (MOSFET): Different types of MOSFET's, Working operation and V-I Characteristics of different types of MOSFET's.

Text Books:

1. R.L. Boylestad and Louis Nashelsky, "Electronic Devices and Circuits", PEI/PHI, 12th Ed, 2015.
2 J. Millman and C. C. Halkias, Satyabratajit, "Electronic Devices and Circuits", TMH, 4th Ed. 2015.
2. Sedra, Adel S., and Kenneth C. Smith. Microelectronic Circuits. Oxford University Press, 7th ed., 2014.

References Books:

1. "Electronic Devices and Circuits", S.Salivahanan and N.Suresh Kumar, TMH, 2015.
2. "Electronic Devices and Circuits", Sanjeev Gupta and Santosh Gupta, Dhanpat Rai Publications 5th Ed.2017
3. Razavi, Behzad. Fundamentals of Microelectronics. Wiley, 2nd ed 2013.
4. Taur, Yuan, and Tak H. Ning. Fundamentals of Modern VLSI Devices. Cambridge University Press, 2nd ed., 2009

UNIT-I
PN Junction Diode

Before we go to learn about the Dode let us know about the materials

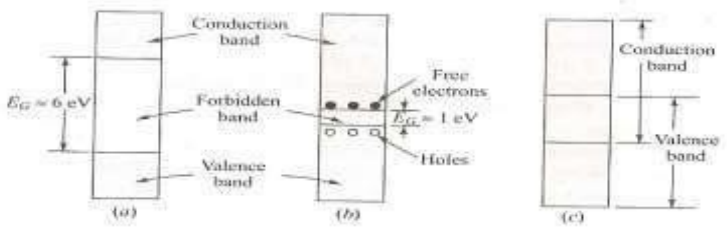


Fig 1 *Energy-band structure of (a) an insulator, (b) a semiconductor, and (c) a metal.*

INSULATOR:

An insulator is a material that offers a very low level of conductivity under Pressure from an applied voltage source. In this material Forbidden energy gap is large (EG 6e.V).So, electron cannot acquire enough energy and hence conduction is not possible. Ex: Diamond is a perfect insulator.

SEMI CONDUCTOR:

A semiconductor is a material that has a conductivity level somewhere in between the extremes of an insulator and a conductor. Energy gap is only about 1ev. Ex: Germanium, Silicon (Energy gap of Germanium is about 0.785 ev and for silicon it is 1.21ev).

CONDUCTOR:

Conductor is a material that will support a generous flow of charge when a voltage source of limited magnitude is applied across its terminals. There is no energy gap in conductors. Conduction band and valence band are overlapped. Ex: Copper, Aluminum.

DOPING:

Adding impurities in a semiconductor is called Doping. Pure semiconductor is called intrinsic semiconductor. Semiconductor with impurities added are called extrinsic semiconductor

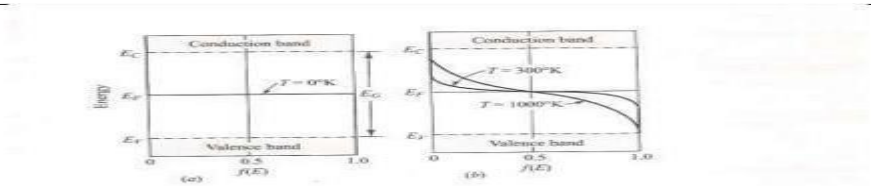


Fig. Fermi-Dirac distribution and energy-band diagram for an intrinsic semiconductor. (a) $T = 0°K$ and (b) $T = 300°K$ and $T = 1000°K$.

EXTRINSIC MATERIALS— *n*- and *p*-type

The characteristics of semiconductor materials can be altered significantly by the addition of certain impurity atoms into the relatively pure semiconductor material. These impurities, although only added to perhaps 1 part in 10 million, can alter the band structure sufficiently to totally change the electrical properties of the material. A semiconductor material that has been subjected to the doping process is called an extrinsic material. There are two extrinsic materials of immeasurable importance to semiconductor device fabrication: *n*-type and *p*-type.

N-Type Material:

Both the *n*- and *p*-type materials are formed by adding a predetermined number of impurity atoms into a germanium or silicon base. The *n*-type is created by introducing those impurities.

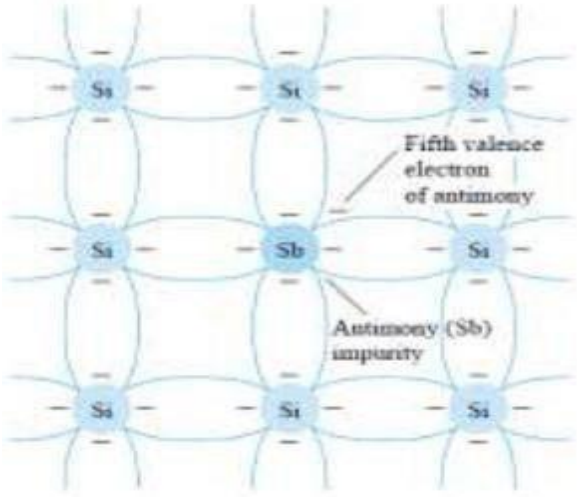


Figure.1 Antimony impurity in n-type material

Fig.1 (using antimony as the impurity in a silicon base) Note that the four covalent bonds are still present. There is, however, an additional fifth electron due to the impurity atom, which is *unassociated* with any particular covalent bond. This remaining electron, loosely bound to its parent (antimony) atom, is relatively free to move within the newly formed *n*-type material. Since the inserted impurity atom has donated a relatively —free‖ electron to the structure: Diffused impurities with five valence electrons are called donor atoms**.** The effect of this doping Process on the relative conductivity can best be described through the use of the energy-band diagram of Fig. 1.1.

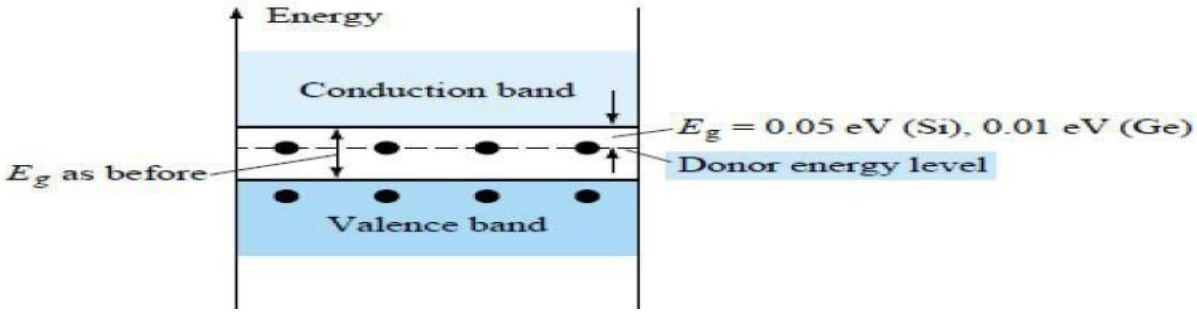
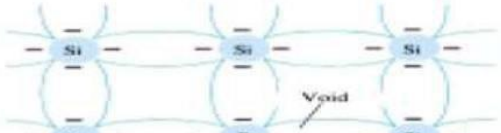


Figure 1.1 Effect of donor impurities on the energy band structure. *P-Type* Material

The *p*-type material is formed by doping a pure germanium or silicon crystal with impurity atoms having *three* valence electrons. The elements most frequently used for this purpose are *boron, gallium,* and *indium.* The effect of one of these elements, boron, on a base of silicon is indicated in Fig. 1.2 Note that there is now an insufficient number of electrons to complete the covalent bonds of the newly formed lattice. The resulting vacancy is called a *hole* and is represented by a small circle or positive sign due to the absence of a negative charge. Since the resulting vacancy will readily *accept* a —free‖ electron: The diffused impurities with three valence electrons are called acceptor atoms.

Majority and Minority Carriers In the intrinsic state, the number of free electrons in Ge or Si is due only to those few electrons in the valence band that have acquired sufficient energy from thermal or light sources to break the covalent bond or to the few impurities that could not be removed. The vacancies left behind in the covalent bonding structure represent our very limited supply of holes. In an *n*-type material, the number of holes has not changed significantly from this intrinsic level. The net result, therefore, is that the number of electrons far outweighs the number of holes. For this reason:



In an n-type material (Fig. 1.13a) the electron is called the majority carrier and the hole the minority carrier.For the *p*-type material the number of holes far outweighs the number of electrons, as shown in Fig. 1.13b. Therefore: In a p-type material the hole is the majority carrier and the electron is the minority carrier. When the fifth electron of a donor atom leaves the parent atom, the atom remaining acquires a net positive charge: hence the positive sign in the donor-ion representation. For similar reasons, the negative sign appears in the acceptor ion.

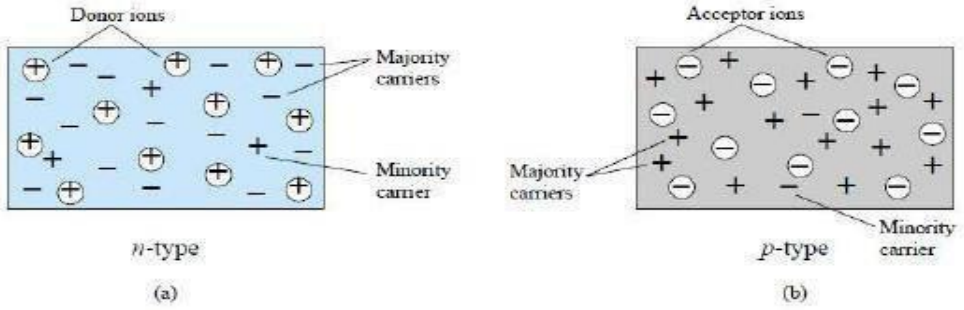


Figure 1.13 (a) *n*-type material; (b) *p*-type material.

Fermi Level in N & P type materials is shown in below Fig:

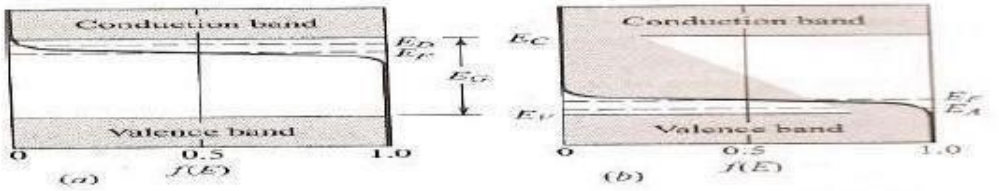


Fig. Positions of Fermi level in (a) n-type and (b) p-type semiconductors.

In N type material Fermi level is just below the conduction band. In P type material Fermi level is just above the valence band. The semiconductor diode is formed by simply bringing these materials together (constructed from the same base—Ge or Si), as shown in Fig. 1.14. At the instant the two materials are—joined‖ the electrons and holes in the region of the junction will combine, resulting in a lack of carriers in the region near the junction. This region of uncovered positive and negative ions is called the depletion region due to the depletion of carriers in this region. Since the diode is a two-terminal device, the application of a voltage across its terminals leaves three possibilities: *no bias* (V_D = 0 V), *forward bias* (V_D >0 V), and *reverse bias* (V_D< 0 V).

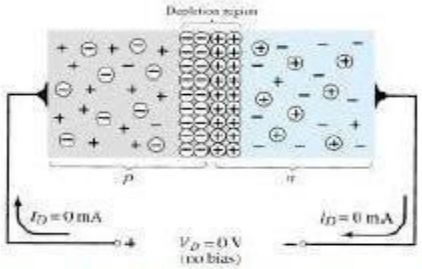


Figure 1.14 *p-n* junction with no external bias.

pplied Bias (*VD* = 0 V)

Under no-bias (no applied voltage) conditions, any minority carriers (holes) in the *n*-type material that find themselves within the depletion region will pass directly into the *p*-type material. The closer the minority carrier is to the junction, the greater the attraction for the layer of negative ions and the less the opposition of the positive ions in the depletion region of the *n* type material. For the purposes of future discussions we shall assume that all the minority carriers of the *n*-type material that find themselves in the depletion region due to their random motion will pass directly into the *p*-type material. Similar discussion can be applied to the minority carriers (electrons) of the *p*-type material. This carrier flow has been indicated in Fig. 1.14 for the minority carriers of each material. The majority carriers (electrons) of the *n*-type material must overcome the attractive forces of the layer of positive ions in the *n*-type material and the shield of negative ions in the *p*-type material to migrate into the area beyond the depletion region of the *p*-type material. However, the number of majority carriers is so large in the *n*-type material that there will invariably be a small number of majority carriers with sufficient kinetic energy to pass through the depletion region into the *p*-type material. Again, the same type of discussion can be applied to the majority carriers (holes) of the *p*-type material. The resulting flow due to the majority carriers is also shown in Fig. 1.14. In the absence of an applied bias voltage, the net flow of charge in any one direction for a semiconductor diode is zero. The symbol for a diode is repeated in Fig. 1.15 with the associated *n*- and *p*-type regions. Note that the arrow is associated with the *p*-type component and the bar with the *n*-type region. As indicated, for *VD*= 0 V, the current in any direction is 0 mA.

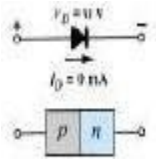


Figure 1.15 No-bias conditions for a semiconductor diode. Reverse-Bias Condition (V_D < 0 V)

If an external potential of *V* volts is applied across the *p*-*n* junction such that the positive terminal is connected to the *n*-type material and the negative terminal is connected to the *p*-type material as shown in Fig. 1.16, the number of uncovered positive ions in the depletion region of the *n*-type material will increase due to the large number of —free‖ electrons drawn to the positive potential of the applied voltage. For similar reasons, the number of uncovered negative ions will increase in the *p*-type material. The net effect, therefore, is a widening of the depletion region. This widening of the depletion region will

establish too great a barrier for the majority carriers to overcome, effectively reducing the majority carrier flow to zero as shown in Fig. 1.16.

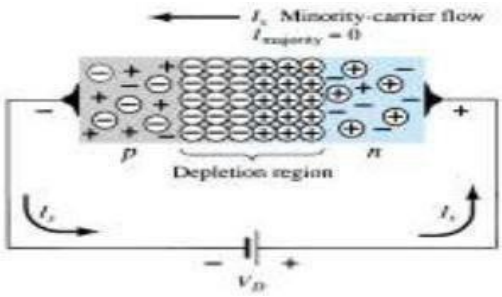


Figure 1.16 Reverse-biased *p-n* junction.

The number of minority carriers, however, that find themselves entering the depletion region will not change, resulting in minority-carrier flow vectors of the same magnitude indicated in Fig. 1.14 with no applied voltage the current that exists under reverse-bias conditions is called the reverse saturation current and is represented by Io.

Forward-Bias Condition (V_D > 0 V)

A *forward-bias* or —on‖ condition is established by applying the positive potential to the *p*-type material and the negative potential to the *n*-type material as shown in Fig. 1.18. A semiconductor diode is forward-biased when the association p-type and positive and n-type and negative has been established.

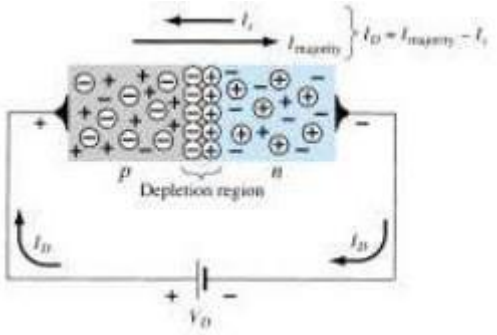


Figure 1.18 Forward-biased *p-n junction*

The application of a forward-bias potential V_D will —pressure‖ electrons in the *n*-type material and holes in the *p*-type material to recombine with the ions near the boundary and reduce the width of the depletion region as shown in Fig. 1.18. The resulting minority-carrier flow of electrons from the *p*-type material to the *n*-type material (and of holes from the *n*-type material to the *p*-type material) has not changed in magnitude (since the conduction level is controlled primarily by the limited number of impurities in the material), but the reduction in the width of the depletion region has resulted in a heavy majority flow across the junction.

An electron of the *n*-type material now seems to be a reduced barrier at the junction due to the reduced depletion region and a strong attraction for the positive potential applied to the *p*-type material. As the applied bias increases in magnitude the depletion region will continue to decrease in width until a flood of electrons can pass through the junction, resulting in an exponential rise in current as shown in the forward-bias region of the characteristics of Fig. 1.19. Note that the vertical scale of Fig. 1.19 is measured in mill amperes and the horizontal scale in the forward-bias region has a maximum of 1 V. typically, therefore, the voltage across a forward-biased diode will be less than 1 V.

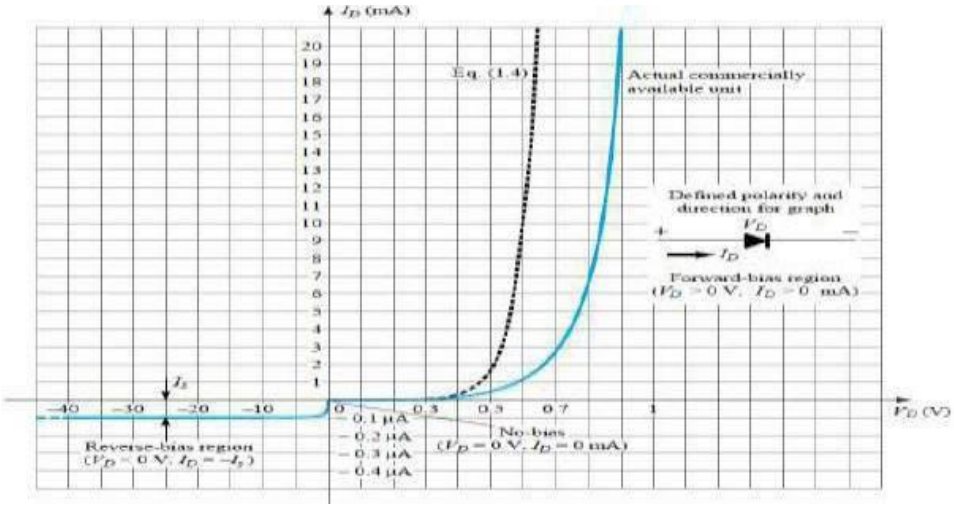


Figure 1.19 Silicon semiconductor diode characteristics

DIODE TERMINAL CHARACTERISTICS

Equation for diode junction current:

$$i_D = I_o(e^{v_D/\eta V_T} - 1) \quad \text{A}$$

Where

- $V_T = k_T/q$; V
- V_D_ diode terminal voltage, Volts
- Io _ temperature-dependent saturation current, μA
- T _ absolute temperature of p-n junction,
- K _ Boltzmann's constant 1.38x 10 -23J/K)
- q _ electron charge 1.6x10-19 C
- η = empirical constant, 1 for Ge and 2 for Si

Temperature Effects

Temperature can have a marked effect on the characteristics of a silicon semiconductor diode a shown in Fig. 1.24. It has been found experimentally that the reverse saturation current Io will just about double in magnitude for every 10°C increase in temperature.

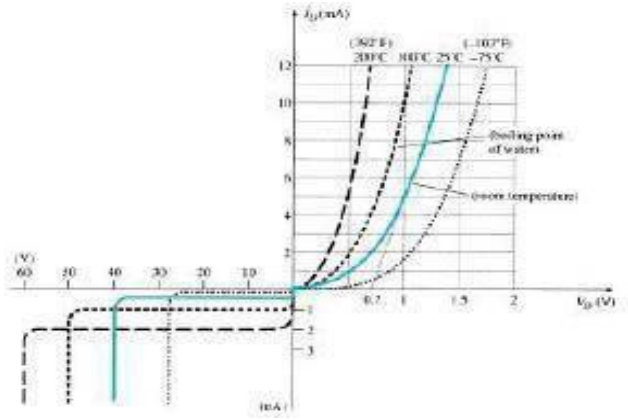


Figure 1.24 Variation in diode characteristics with temperature change.

It is not uncommon for a germanium diode with an *Io* in the order of 1 or 2 A at 25°C to have a leakage current of 100 A _ 0.1 mA at a temperature of 100°C. Typical values of *Io* for silicon are much lower than that of germanium for similar power and current levels. The result is that even at high temperatures the levels of *Io* for silicon diodes do not reach the same high levels obtained for germanium—a very important reason that silicon devices enjoy a significantly higher level of development and utilization in design. Fundamentally, the open-circuit equivalent in the reverse bias region is better realized at any temperature with silicon than with germanium. The increasing levels of *Io* with temperature account for the lower levels of threshold voltage, as shown in Fig. 1.24. Simply increase the level of *Io* in and not rise in diode current. Of course, the level of *TK* also will be increase, but the increasing level of *Io* will overpower the smaller percent change in *TK*. As the temperature increases the forward characteristics are actually becoming more —ideal.

Static resistance and dynamic resistance.

DC or Static Resistance:

The application of a dc voltage to a circuit containing a semiconductor diode will result in an operating point on the characteristic curve that will not change with time. The resistance of the diode at the operating point can be found simply by finding the Corresponding levels of V_D and I_D as shown in Fig. 1.25 and applying the following Equation:

$$R_D = \frac{V_D}{I_D}$$

The dc resistance levels at the knee and below will be greater than the resistance levels obtained for the vertical rise section of the characteristics. The resistance levels in the reverse-bias region will naturally be quite high. Since ohmmeters typically employ a relatively constant-current source, the resistance determined will be at a preset current level (typically, a few mill amperes).

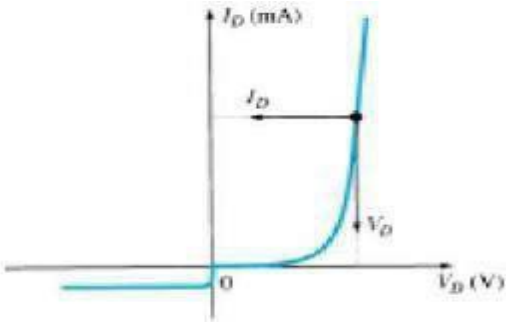


Figure 1.25 determining the dc resistance of a diode at a particular operating point. AC or Dynamic Resistance

It is obvious from Eq. 1.5 that the dc resistance of a diode is independent of the shape of the characteristic in the region surrounding the point of interest. If a sinusoidal rather than dc input is applied, the situation will change completely. The varying input will move the instantaneous operating point up and down a region of the characteristics and thus defines a specific change in current and voltage as shown in Fig. 1.27. With no applied varying signal, the point of operation would be the *Q*-point appearing on Fig. 1.27 determined by the applied dc levels. The designation *Q-point* is derived from the word *quiescent,* which means —still or unvarying.

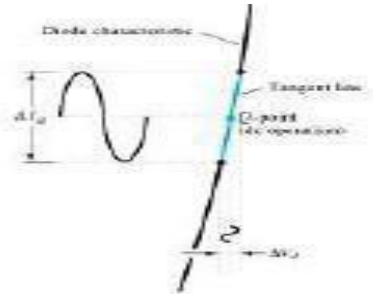


Figure 1.27 defining the dynamic or ac resistance.

Straight line drawn tangent to the curve through the *Q*-point as shown in Fig. 1.28 will define a Particular change in voltage and current that can be used to determine the *ac* or *dynamic* resistance for this region of the diode characteristics. In equation form,

$$r_d = \frac{\Delta V_d}{\Delta I_d}$$ where Δ signifies a finite change in the quantity. (1.6)

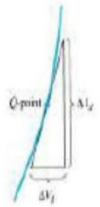


Figure 1.28 determining the ac resistance at a *Q*-point

Diode Equivalent Circuits:

An equivalent circuit is a combination of elements properly chosen to best represent the actual terminal characteristics of a device, system, or such in a particular operating region. In other words, once the equivalent circuit is defined, the device symbol can be removed from a schematic and the equivalent circuit inserted in its place without severely affecting the actual behavior of the system. The result is often a network that can be solved using traditional circuit analysis techniques.

Piecewise-Linear Equivalent Circuit

One technique for obtaining an equivalent circuit for a diode is to approximate the characteristics of the device by straight-line segments, as shown in Fig. 1.31. The resulting equivalent circuit is naturally called the *piecewise-linear equivalent circuit.* It should be obvious from Fig. 1.31 that the straight-line segments do not result in an exact duplication of the actual characteristics, especially in the knee region. However, the resulting segments are sufficiently close to the actual curve to establish an equivalent circuit that will provide an excellent first approximation to the actual behavior of the device.

The ideal diode is included to establish that there is only one direction of conduction through the device, and a reverse-bias condition will result in the open circuit state for the device. Since a silicon semiconductor diode does not reach the conduction state until V_D reaches 0.7 V with a forward bias (as shown in Fig. 1.31), a battery *VT* opposing the conduction direction must appear in the equivalent circuit as shown in Fig. 1.32. The battery simply specifies that the voltage across the device must be greater than the threshold battery voltage before conduction through the device in the direction dictated by the ideal diode can be established. When conduction is established the resistance of the diode will be the specified value of r_{av}.

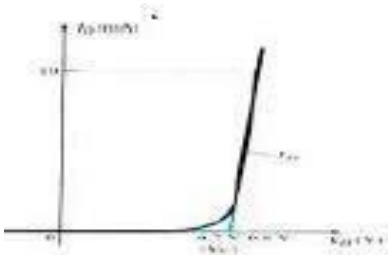


Figure 1.31 defining the piecewise-linear equivalent circuit using straight-line segments to approximate the characteristic curve.

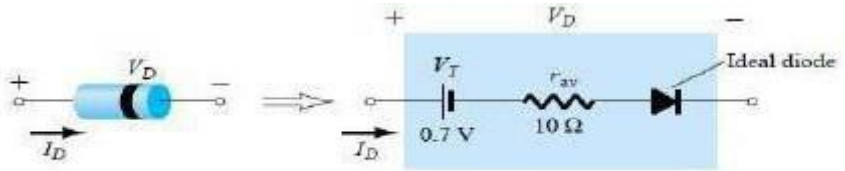


Figure 1.32 Components of the piecewise-linear equivalent circuit.

The approximate level of *rav* can usually be determined from a specified operating point on the specification sheet. For instance, for a silicon semiconductor diode, if I_F _ 10 mA (a forward conduction current for the diode) at *VD* _ 0.8 V, we know for silicon that a shift of 0.7 V is required before the characteristics rise.

$$r_{av} = \left.\frac{\Delta V_d}{\Delta I_d}\right|_{\text{pt. to pt.}} = \frac{0.8\text{ V} - 0.7\text{ V}}{10\text{ mA} - 0\text{ mA}} = \frac{0.1\text{ V}}{10\text{ mA}} = \mathbf{10\ \Omega}$$

Simplified Equivalent Circuit

For most applications, the resistance r_{av} is sufficiently small to be ignored in comparison to the other elements of the network. The removal of r_{av} from the equivalent circuit is the same as applying that the characteristics of the diode. Under dc conditions has a drop of 0.7 V across it in the conduction state at any level of diode current.

Ideal Equivalent Circuit

Now that *r*av has been removed from the equivalent circuit let us take it a step further and establish that a 0.7-V level can often be ignored in comparison to the applied voltage level. In this case the equivalent circuit will be reduced to that of an ideal diode as shown in Fig. 1.34 with its characteristics.

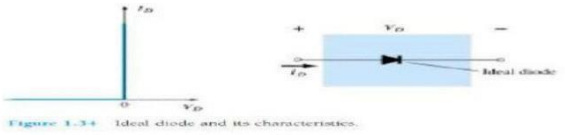
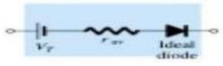
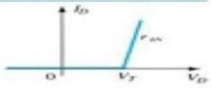
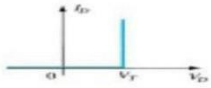
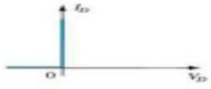


Figure 1.34 Ideal diode and its characteristics.

TABLE 1.3 Diode Equivalent Circuits (Models)

Type	Conditions	Model	Characteristics
Piecewise-linear model			
Simplified model	$R_{network} \gg r_{av}$		
Ideal device	$R_{network} \gg r_{av}$ $E_{network} \gg V_T$		

TRANSITION AND DIFFUSION CAPACITANCE

Electronic devices are inherently sensitive to very high frequencies. Most shunt capacitive effects that can be ignored at lower frequencies because the reactance $XC=1/2\pi fC$ is very large (open-circuit equivalent). This, however, cannot be ignored at very high frequencies. *XC* will become sufficiently small due to the high value of *f* to introduce a low-reactance—shorting‖ path. In the *p-n* semiconductor diode, there are two capacitive effects to be considered. In the reverse bias region we have the transition- or depletion-region capacitance (CT), while in the forward bias region we have the diffusion (CD) or storage capacitance.Recall that the basic equation for the capacitance of a parallel-plate capacitor is defined by $C=\epsilon A/d$, where ϵ is the permittivity of the dielectric (insulator) between the plates of area *A* separated by a distance *d*. In the reverse bias region there is a depletion region (free of carriers) that behaves essentially like an insulator between the layers of opposite charge. Since the depletion width (*d*) will increase with increased reverse-bias potential, the resulting transition capacitance will decrease. The fact that the capacitance is dependent on the applied reverse-bias potential has application in a number of electronic systems. Although the effect described above will also be present in the forward-bias region, it is overshadowed by a capacitance effect directly dependent on the rate at which charge is injected into the regions just outside the depletion region. The capacitive effects described above are represented by a capacitor in parallel with the ideal diode, as shown in Fig. 1.38. For low- or mid-frequency applications (except in the power area), however, the capacitor is normally not included in the diode symbol.

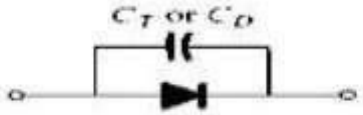


Figure 1.38 Including the effect of the transition or diffusion capacitance on the semiconductor diode.

Break down mechanisms in semiconductor diodes.

Zener Region: There is a point where the application of too negative a voltage will result in a sharp change in the characteristics, as shown in Fig. 1.22. The current increases at a very rapid rate in a direction opposite to that of the positive voltage region. The reverse-bias potential that results in this dramatic change in characteristics is called the *Zener potential* and is given the symbol VZ. As the voltage across the diode increases in the reverse-bias region, the velocity of the minority carriers responsible for the reverse saturation current *Io* will also increase. Eventually, their velocity and associated kinetic energy will be sufficient to release additional carriers through collisions with otherwise stable atomic structures. That is, an *ionization* process will result whereby valence electrons absorb sufficient energy to leave the parent atom. These additional carriers can then aid the ionization process to the point where a high *avalanche* current is established and the *avalanche breakdown* region determined.

The avalanche region (*VZ*) can be brought closer to the vertical axis by increasing the doping levels in the *p*- and *n*-type materials. However, as *VZ* decreases to very low levels, such as _5 V, another mechanism, called *Zener breakdown*, will contribute to the sharp change in the characteristic. It occurs because there is a strong electric field in the region of the junction that can disrupt the bonding forces within the atom and —generate‖ carriers. Although the Zener breakdown mechanism is a significant contributor only at lower levels of *VZ*, this sharp change in the characteristic at any level is called the *Zener region* and diodes employing this unique portion of the characteristic of a *p-n* junction are called *Zener diodes.*

The maximum reverse-bias potential that can be applied before entering the Zener region is called the peak inverse voltage (referred to simply as the PIV rating) or the peak reverse voltage (denoted by PRV rating). If an application requires a PIV rating greater than that of a single unit, a number of diodes of the same characteristics can be connected in series. Diodes are also connected in parallel to increase the current-carrying capacity.

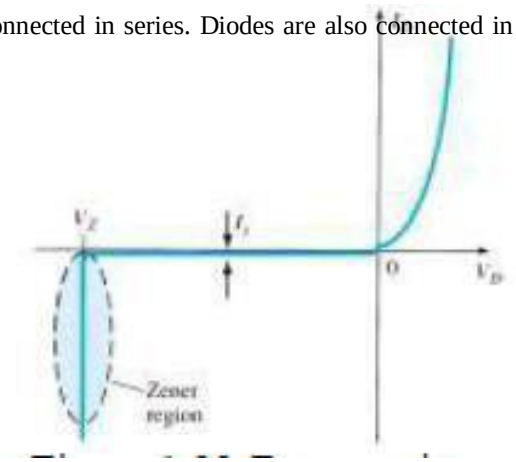


Figure 1.22 Zener region.

ZENER DIODE

The characteristic drops in an almost vertical manner at a reverse-bias potential denoted V_Z .The fact that the curve drops down and away from the horizontal axis rather than up and away for the positive V_D region reveals that the current in the Zener region has a direction opposite to that of a forward-biased diode.

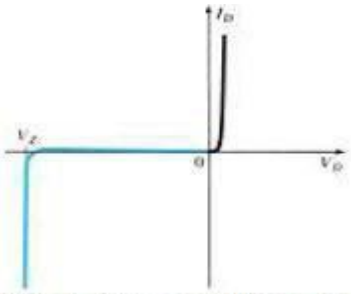


Fig.1.47 zener diode characteristics

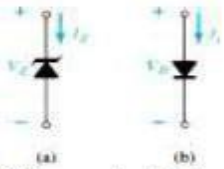
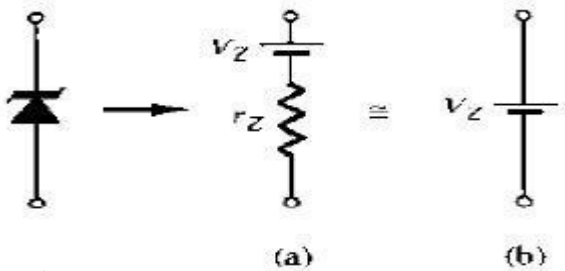


Figure 1.48 Conduction direction:
(a) Zener diode; (b) semiconductor diode

This region of unique characteristics is employed in the design of *Zener diodes*, which have the graphic symbol appearing in Fig. 1.48a. Both the semiconductor diode and zener diode are presented side by side in Fig. 1.48 to ensure that the direction of conduction of each is clearly understood together with the required polarity of the applied voltage. For the semiconductor diode the —on‖ state will support a current in the direction of the arrow in the symbol. The location of the Zener region can be controlled by varying the doping levels. An increase in doping, producing an increase in the number of added impurities, will decrease the Zener potential. Zener diodes are available having Zener potentials of 1.8 to 200 V with power ratings from 14 _ to 50 W. Because of its higher temperature and current capability, silicon is usually preferred in the manufacture of Zener diodes.



The complete equivalent circuit of the Zener diode in the Zener region includes a small dynamic resistance and dc battery equal to the Zener potential, as shown in Fig. 1.49.

Problems

1. A PN Junction diode has a reverse saturation current of 30 A at a temperature of 125 C At the same temperature find the dynamic resistance for 0.2V bias in forward and reverse bias

Solution: -

$V = 0.7V,\ I = 2\ mA,\ T = 300^{\circ}K,\ V_T = 26\ mv.$

$V = 0.75v,\ I = ?$

Case (i) I $I = I_0\left(e^{\frac{V}{\eta V_T}} - 1\right)$

$= 2\times10^{-3} = I_0\left(e^{\frac{0.7}{26\times10^{-3}}} - 1\right)$

$= I_0\ (e^{26.923} - 1) \approx I_0\ (e^{26.923})$

$I_0 = \frac{2\times10^{-3}}{e^{26.923}}$

Case (ii) $I = I_0\left(e^{\frac{V}{\eta V_T}} - 1\right)$

$I_0 = \frac{2\times10^{-3}}{e^{26.923}}\left(e^{\frac{0.75}{26\cdot10^{-3}}}\right)$

$= \left(\frac{2\times10^{-3}}{e^{26.923}}\right)e^{28.846}$

$= 2\times10^{-3}\ e^{28.486-26.923}$

$= 2\times10^{-3}\ e^{1.563}$

$= 2\times10^{-3}\ 6.843$

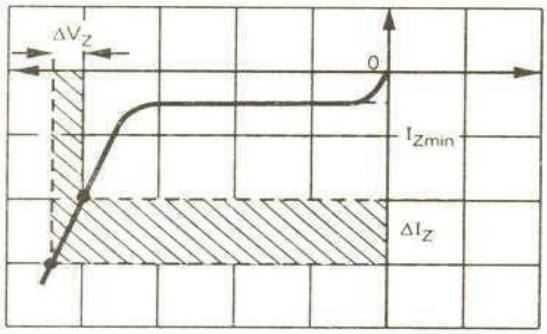
$\simeq 13.686\ mA$

Varactor Diode:

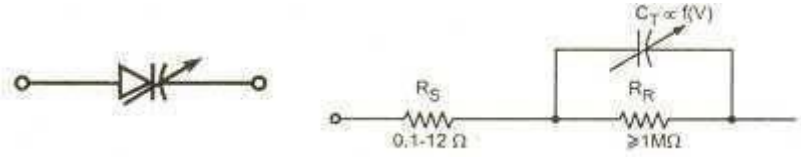
In both alloy junction diode and grown junction diode as the magnitude of the reverse bias increases, the width 'w' of the transition region increases, and the junction capacitance c(t) reduces.The voltage- variable nature of transition capacitance of reverse-biased pn- junction may be utilized in several applications such as

- In voltage tuning of an LC resonant.
- Self balancing bridge circuits.
- In parametric amplifiers etc.
- FM radio and TV receivers, AFC circuits.
- Used in adjustable band pass filters.

This special diode is made especially for the above applications which are biased on the voltage- variable capacitance are called "Varactor diode" or "Varicap" or "Voltacap".



Varactor diode symbol and circuit models are shown below.



- Rs: Body series resistance.
- C(t): Barrier capacitance.
- R_r : Reverse diode resistance.
- Typically, at a reverse bias of 4v
- C(t)= 20pF, R(s)=8.5 ohms, R(r)>1M (usually neglected)

Tunnel diode:

A normal pn-junction has an impurity concentration of about 1 part in 10^8. With this amount of doping, the width of depletion layer, which constitutes the potential barrier of the junction, is of the order of 5 microns ($5x10^{-4}$ cm).If the concentration of impurity atoms is greatly increased, say 1 part in 10^3 the device characteristics are completely changed. The new diode was announced in 1958 by Leo Esaki. This diode is called 'Tunnel diode' or 'Esaki diode'.The barrier potential VB is related with the width of the depletion region with the following equation. As the depletion width decreases there is a large probability that an electron will penetrate through the barrier. This quantum mechanical behavior is referred to as tunneling and hence these high impurity density pn-junction devices are called Tunnel diodes. This phenomenon is called as 'tunneling'.

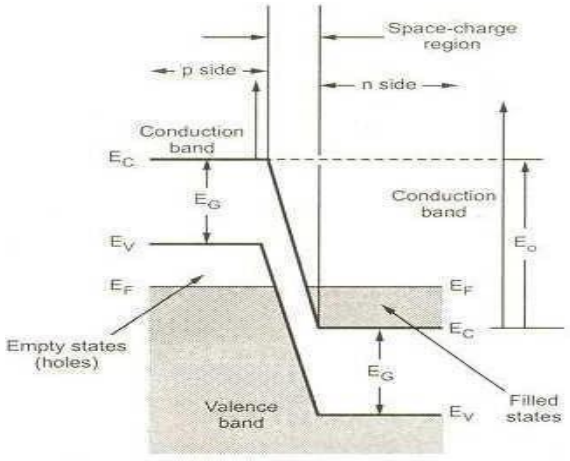


Fig. energy band in a heavily doped pn-diode under open circuited condition.

The Fermi level E_f in the p-side is at the same energy as the Fermi level Ef in the n-side. Note that there are no filled states on one side of the junction which are at the same energy as empty allowed states on the other side. Hence there can be no flow of charge in either direction across the junction, and the current is zero for an open circuited diode.

The volt-ampere characteristic:

If a reverse bias voltage is applied to the tunnel diode, the height of the barrier is increased above the open-circuit value EO. Hence the n-side levels must shift downward with respect to the p-side levels as shown in the figure below.

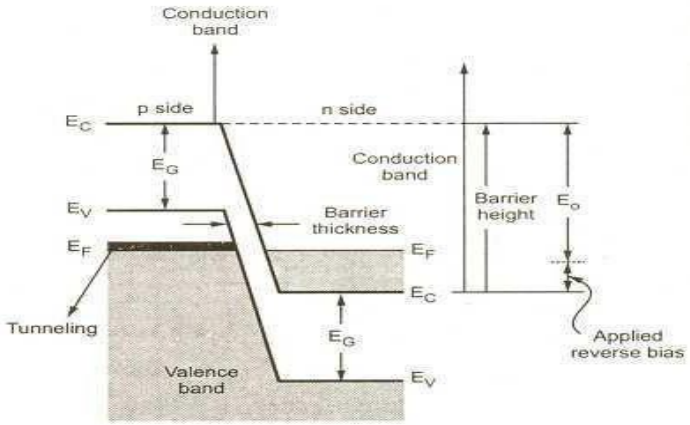


Fig. Under applied reverse bias

We now observe that there are some energy states in the valance band of the p-side which lie at the same level as allowed empty states in the conduction band of the n-side. Hence these electrons will tunnel from the p to the n-side, giving rise to a reverse diode current. As the magnitude of the reverse bias increase, causing the reverse current to increase. Consider if a forward bias is applied to the diode so that the potential barrier is decreased below Eo. Hence the n-side levels must shift upward with respect to those on the p-side.

The energy band diagrams for a heavily doped under forward bias conditions are shown in figure below.

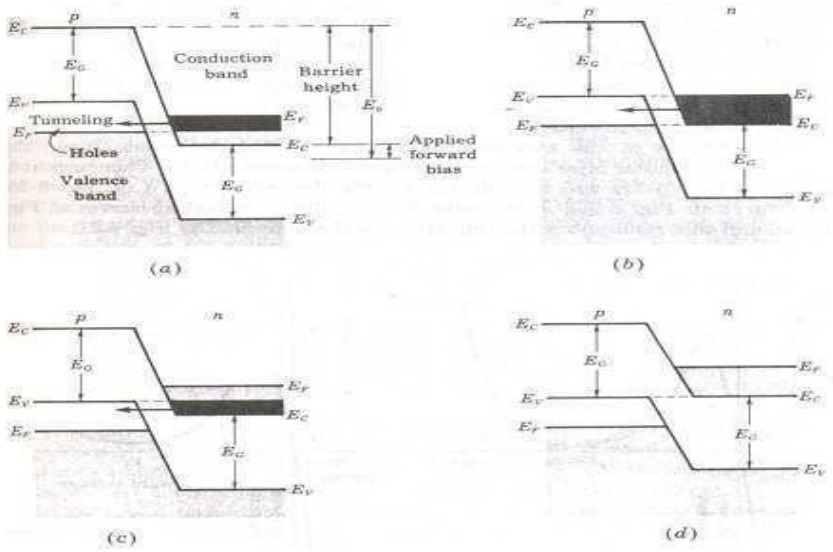


Fig. As the bias is increased, the band structure changes progressively from (a) to (d).

From fig (a) we can observe that the electrons will tunnel from the n to the p material giving rise to the forward current. As the forward bias is increased further, the maximum number of electrons can leave from occupied states on the right side of the junction, and tunnel through the barrier to the empty states on the left side of the junction giving rise to the peak current Ip. If still more forward bias is applied, fig© is obtained and the tunneling current decreases. Finally if the forward bias is larger there is no9 empty allowed states on one side of the junction at the same energy as occupied states on the other side, the tunneling current must drop to zero.
The v-I characteristics of tunnel diode is shown in fig.

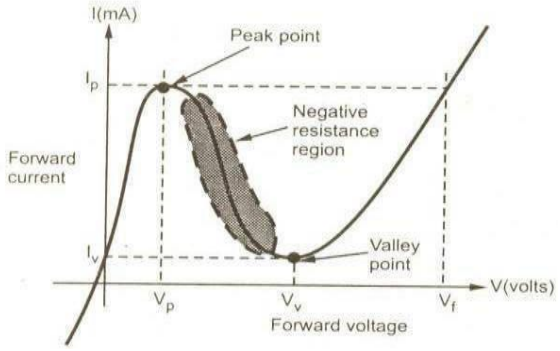
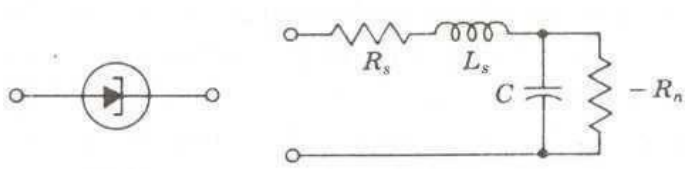


Fig.-1 Characteristics of a tunnel diode.

The tunnel diode exhibits a negative resistance characteristics between peak current Ip and valley current Iv. The tunnel diode is excellent conductor in the reverse bias conditions. By applying small forward bias voltage to the tunnel diode the current increases and reaches to the maximum level. The maximum for small forward bias voltage is called as 'peak current (Ip)'.The corresponding voltage to the peak current is called 'peak voltage (V_p)'. If forward bias voltage is increased beyond the peak voltage the current starts decreasing and reaches to the maximum level. This minimum value of the current is called as "valley current (I_v)". The corresponding voltage to the valley current is called as "valley voltage (Vv)"If forward bias voltage is increased beyond valley voltage it exhibits the same characteristics as ordinary diode.The tunnel diode symbol and small-signal model are shown in fig. below.

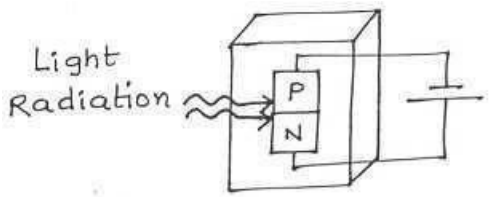


Applications of Tunnel diode:

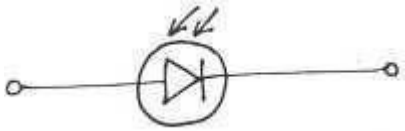
1. It is used as a very high speed switch, since tunneling takes place at the speed of light.
2. It is used as a high frequency oscillator.

Photodiode:

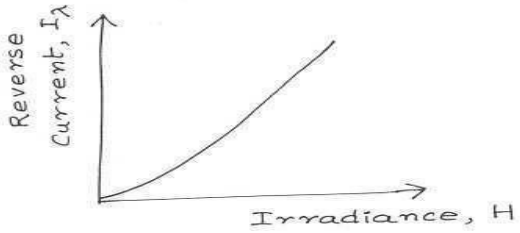
The photodiode is a device that operates in reverse diode. The photodiode has a small transparent window that allows light to strike one surface of the pn-junction, keeping the remaining sides unilluminated.



The symbol of photodiode is shown in figure below.



A photodiode differs from a rectifier diode in that when its pn -junction is exposed to light, the reverse current increases with the light intensity. When there is no incident light the reverse current, I , is almost negligible and is called the dark current. An increase in the amount of light intensity, expressed as irradiance (mW/cm^2), produces an increase in the reverse current.



Therefore, $R_R = V_R / I = 10v/55\ \mu a = 182K\Omega$

Hence the photodiode can be used as a variable-resistance device controlled by light intensity.

The volt-ampere characteristics of photodiode are shown in figure.

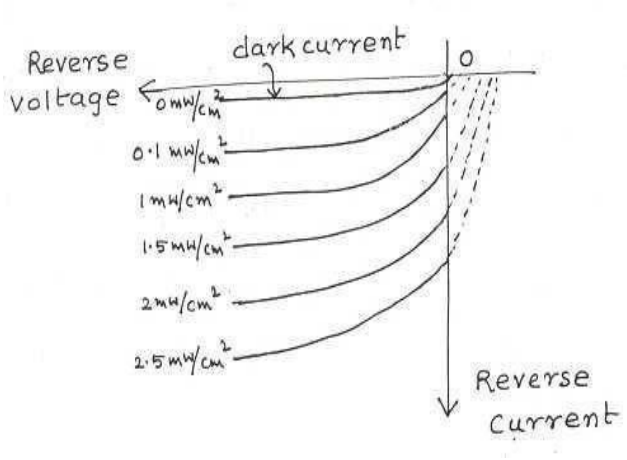


Fig. V-I characteristics of photo diode.

Advantages of Photo diodes:

1. It can be used as variable-resistance device.
2. Highly sensitive to the light.
3. The speed of operation is very high.

Disadvantages of Photo diodes:

1. The dark current is temperature dependent.

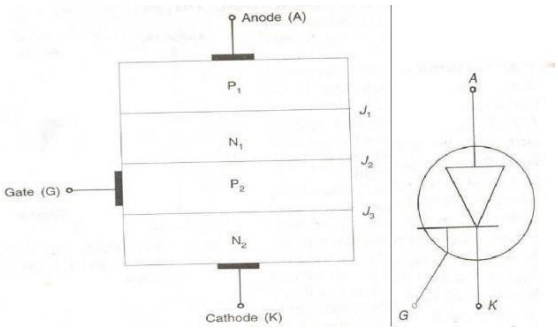
Applications of photodiode:

1) Photodiodes are commonly used in alarm systems and counting systems.
2) Used in demodulators.
3) Used in encoders.
4) Used in light detectors.
5) Used in optical communication systems.

SCR (SILICON CONTROLLED RECTIFIER)

The basic structure and circuit symbol of SCR is shown in figure below.It is a four layer three terminal device in which the end p-layer acts as anode, the end n-layer acts as anode, the end n-layer acts as cathode and p-layer nearer to cathode acts as gate.

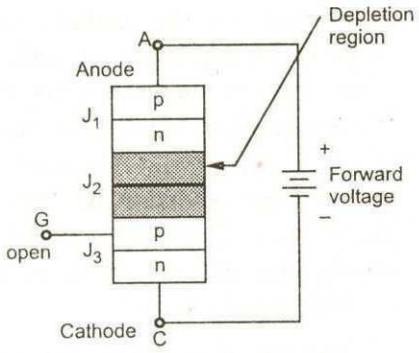
As leakage current in silicon is very small compared to germanium, SCR's are made of silicon and not germanium.



(a) Basic Structure (b) Circuit symbol

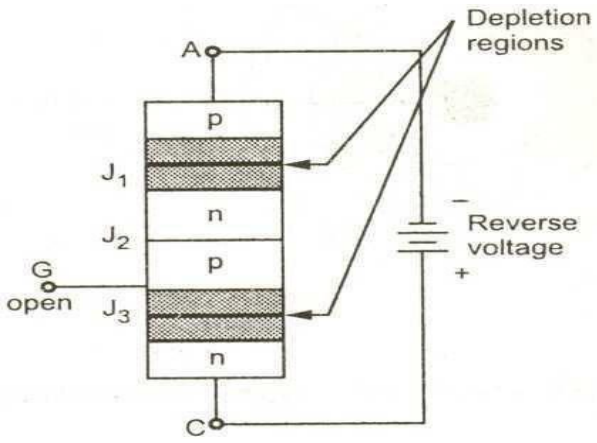
Operation of SCR: The operation of SCR is divided into two categories,

When gate is open: Consider that the anode is positive with respect to cathode and gate is open.The junctions J1 and J3 are forward biased and junctions J2 is reverse biased. There is depletion region around J2 and only leakage current flows which is negligibly small. Practically the SCR is said to be 'OFF'. This is called forward blocking state of SCR and voltage applied to anode and cathode with anode positive is called *forward voltage.* This is shown in figure (a) below.



J1, J3 Forward biased. J2 Reverse biased.

With gate open, if cathode is made positive with respect to anode, the junctions J1, J3 become reverse biased and J2 forward biased. Still the current flowing is leakage current, which can be neglected as it is very small. The voltage applied to make cathode positive is called reverse voltage and SCR is said to be in reverse blocking state. This is shown in the figure (b) below.



J1, J3 Reverse biased. J2 Forward biased Fig. Operation of SCR when gate is open (a), (b).

b When gate is closed: Consider that the voltage is applied between gate and cathode when the SCR is in forward blocking state. The gate is made positive with respect to the cathode. The electrons from n-type cathode, which are majority in number, cross the junction J3 to reach to positive of battery. While holes from p-type move towards the negative of battery. This constitutes the gate current. This current increases the anode current as some of the electrons cross junction J2. As anode current increases, more electrons cross the junction J2 and the anode current further increases. Due to regenerative action, within short time, the junction J2 breaks

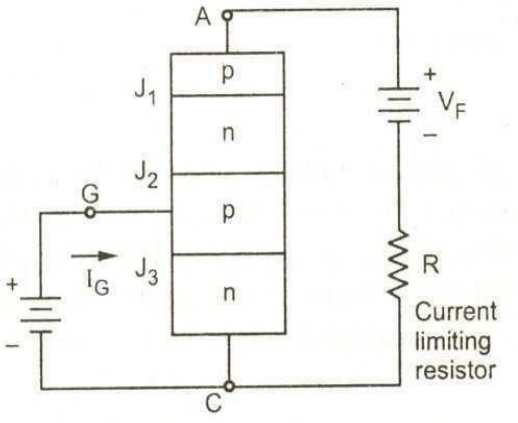


Fig. Operation of SCR when gate is closed

and SCR conducts heavily. The connections are shown in the figure. The resistance R is required to limit the current. Once the SCR conducts, the gate loses its control.

Characteristics of SCR:

The characteristics are divided into two sections:

i) Forward characteristics

ii) Reverse characteristics

i) **Forward characteristics:**

It shows a forward blocking region, when IG=0. It also shows that when forward voltage increases up to VBO, the SCR turns ON and high current results. It also shows that, if gate bias is used then as gate current increases, less voltage is required to turn ON the SCR. If the forward current falls below the level of the holding current IH, then depletion region begins to develop around J2 and device goes into the forward blocking region.When SCR is turned on from OFF state, the resulting forward current is called *latching current* IL. The latching current is slightly higher than the holding current

ii) **Reverse characteristics:**

If the anode to cathode voltage is reversed, then the device enters into the reverse blocking region. The current is negligibly small and practically neglected.If the reverse voltage is increases, similar to the diode, at a particular value avalanche breakdown occurs and a large current flows through the device. This is called reverse breakdown and the voltage at which this happens is called reverse breakdown voltage

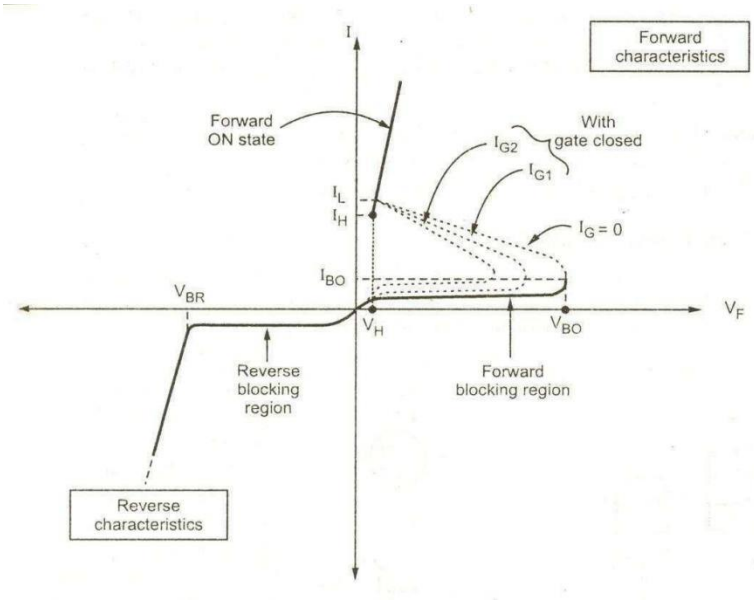
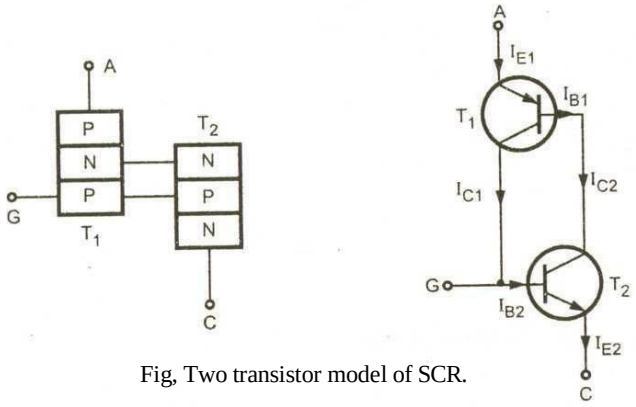


Fig. Characteristics of SCR.

Two Transistor Analogies:

The easiest way to understand how SCR works it ot visualize it separately into two halves, as shown in the figure. The left half is a p-n-p transistor and right half is n-p-n transistor. This is also called two transistor model of SCR.The collector current of T1 becomes base current of T2 and collector current of T2 becomes base current of T1.



Fig, Two transistor model of SCR.

UNIT - II

RECTIFIERS AND FILTERS

Introduction:

For the operation of most of the electronics devices and circuits, a d.c. source is required. So it is advantageous to convert domestic a.c. supply into d.c. voltages. The process of converting a.c. voltage into d.c. voltage is called as rectification.This is achieved with i) Step-down Transformer, ii) Rectifier, iii) Filter and iv) Voltage regulator circuits.

These elements constitute d.c. regulated power supply shown in the figure below.

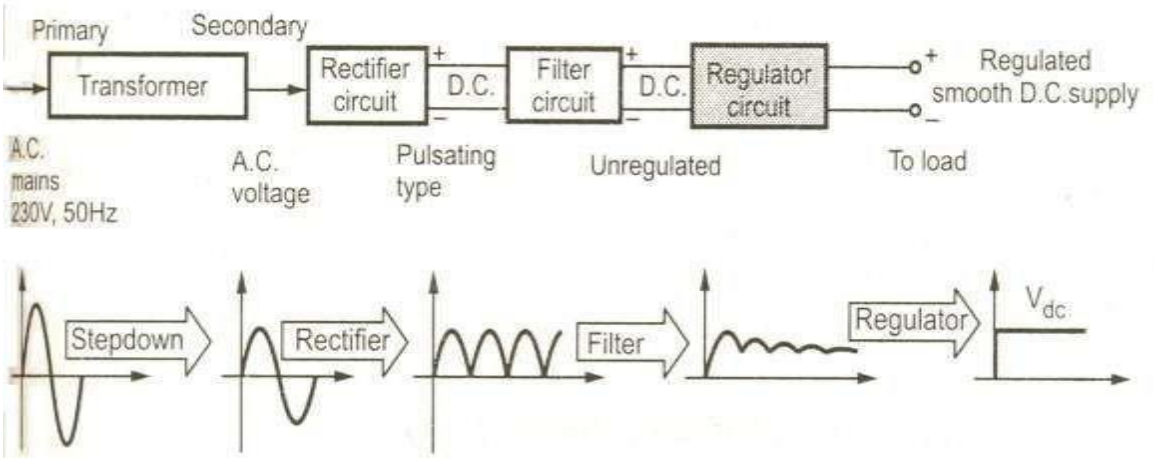


Fig. Block diagram of Regulated D.C. Power Supply

The block diagram of a regulated D.C. power supply consists of step-down transformer, rectifier, filter, voltage regulator and load.

An ideal regulated power supply is an electronics circuit designed to provide a predetermined d.c. voltage Vo which is independent of the load current and variations in the input voltage ad temperature.

If the output of a regulator circuit is a AC voltage then it is termed as voltage stabilizer, whereas if the output is a DC voltage then it is termed as voltage regulator.

The elements of the regulated DC power supply are discussed as follows:

TRANSFORMER:

A transformer is a static device which transfers the energy from primary winding to secondary winding through the mutual induction principle, without changing the frequency. The transformer winding to which the supply source is connected is called the primary, while the winding connected to the load is called secondary.

If N_1,N_2 are the number of turns of the primary and secondary of the transformer then $\alpha = \frac{N_2}{N_1}$ is called the turns ratio of the transformer.

The different types of the transformers are

1) Step-Up Transformer
2) Step-Down Transformer
3) Centre-tapped Transformer

The voltage, current and impedance transformation ratios are related to the turns ratio of the transformer by the following expressions.

Voltage transformation ratio : $\frac{V_2}{V_1} = \frac{N_2}{N_1}$

Current transformation ratio : $\frac{I_2}{I_1} = \frac{N_1}{N_2}$

Impedance transformation ratio : $\frac{Z_L}{Z_{in}} = \left(\frac{N_2}{N_1}\right)^2$

RECTIFIER:

Any electrical device which offers a low resistance to the current in one direction but a high resistance to the current in the opposite direction is called rectifier. Such a device is capable of converting a sinusoidal input waveform, whose average value is zero, into a unidirectional waveform, with a non-zero average component.

A rectifier is a device which converts a.c. voltage (bi-directional) to pulsating d.c. voltage (Uni-directional).

Important characteristics of a Rectifier Circuit:

1. **Load currents:** They are two types of output current. They are average or d.c. current and RMS currents.

   i) **Average or DC current:** The average current of a periodic function is defined as the area of one cycle of the curve divided by the base.

   It is expressed mathematically as $I_{dc} = \frac{1}{2\pi}\int_0^{2\pi} id(\omega t)$; where $i = \mathrm{I_m}\sin\omega t$

   ii) **Effective (or) R.M.S. current:** The effective (or) R.M.S. current squared of a periodic function of time is given by the area of one cycle of the curve which represents the square of the function divided by the base.

   It is expressed mathematically as $I_{rms} = \left(\frac{1}{2\pi}\int_0^{2\pi} i^2 d(\omega t)\right)^{\frac{1}{2}}$

2. **Load Voltages:** There are two types of output voltages. They are average or D.C. voltage and R.M.S. voltage.

   i) **Average or DC Voltage:** The average voltage of a periodic function is defined as the areas of one cycle of the curve divided by the base.
   It is expressed mathematically as

   $$V_{dc} = \frac{1}{2\pi}\int_0^{2\pi} Vd(\omega t);\ \text{Where}\ V = V_{\mathrm{m}}\sin\omega t$$

   (or) $V_{dc} = I_{dc} \times R_L$

   ii) **Effective (or) R.M.S Voltage:** The effective (or) R.M.S voltage squared of a periodic function of time is given by the area of one cycle of the curve which represents the square of the function divided by the base.

   $$V_{rms} = \left(\frac{1}{2\pi}\int_0^{2\pi} V^2 d(\omega t)\right)^{\frac{1}{2}} \qquad V_{rms} = I_{rms} \times R_L$$

3. Ripple Factor (γ) : It is defined as ration of R.M.S. value of a.c. component to the d.c. component in the output is known as "Ripple Factor".

$$\gamma = \frac{V'_{rms}}{V_{dc}}$$

$$V'_{rms} = \sqrt{V_{rms}^2 - V_{dc}^2}$$

$$\therefore \gamma = \sqrt{\left(\frac{V_{rms}}{V_{dc}}\right)^2 - 1}$$

4. Efficiency (η) : It is the ratio of d.c output power to the a.c. input power. It signifies, how efficiently the rectifier circuit converts a.c. power into d.c. power.

It is given by $$\eta = \frac{P_{dc}}{P_{ac}}$$

5. Peak Inverse Voltage (PIV): It is defined as the maximum reverse voltage that a diode can withstand without destroying the junction.

6. Regulation: The variation of the d.c. output voltage as a function of d.c. load current is called regulation. The percentage regulation is defined as

$$\% \text{ Regulation} = \frac{V_{no-load} - V_{full-load}}{V_{full-load}} \times 100\%$$

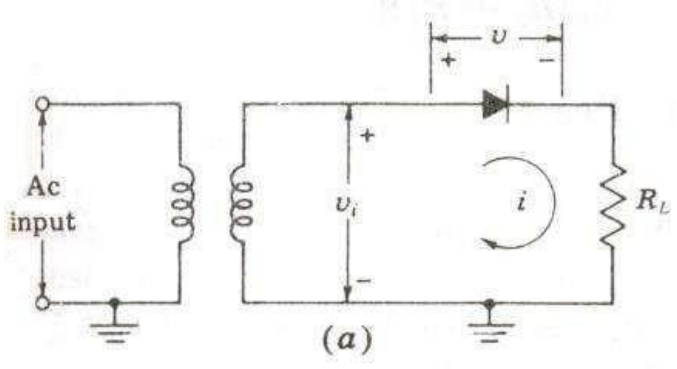
For an ideal power supply, % Regulation is zero.

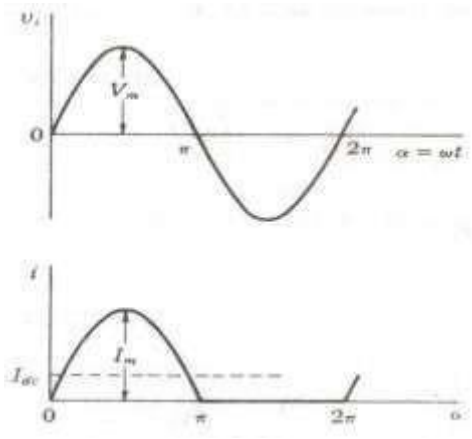
Using one or more diodes in the circuit, following rectifier circuits can be designed.

1. Half - Wave Rectifier
2. Full – Wave Rectifier
3. Bridge Rectifier

HALF-WAVE RECTIFIER:

A Half – wave rectifier is one which converts a.c. voltage into a pulsating voltage using only one half cycle of the applied a.c. voltage. The basic half-wave diode rectifier circuit along with its input and output waveforms is shown in figure below.





The half-wave rectifier circuit shown in above figure consists of a resistive load; a rectifying element i.e., p-n junction diode and the source of a.c. voltage, all connected is series. The a.c. voltage is applied to the rectifier circuit using step-down transformer.

The input to the rectifier circuit, $V = V_m \sin \omega t$ Where Vm is the peak value of secondary a.c. voltage

Operation:

For the positive half-cycle of input a.c. voltage, the diode D is forward biased and hence it conducts. Now a current flows in the circuit and there is a voltage drop across R_L. The waveform of the diode current (or) load current is shown in figure.

For the negative half-cycle of input, the diode D is reverse biased and hence it does not conduct. Now no current flows in the circuit i.e., i=0 and Vo=0. Thus for the negative half-cycle no power is delivered to the load.

Analysis:

In the analysis of a HWR, the following parameters are to be analyzed.

i)	DC output current	ii)	DC Output voltage
iii)	R.M.S. Current	iv)	R.M.S. voltage
v)	Rectifier Efficiency (η)	vi)	Ripple factor (γ)
vii)	Regulation	viii)	Transformer Utilization Factor (TUF)
ix)	Peak Factor (P)		

Let a sinusoidal voltage V_i be applied to the input of the rectifier.

Then $V = V_m \sin \omega t$ Where Vm is the maximum value of the secondary voltage.

Let the diode be idealized to piece-wise linear approximation with resistance R_f in the forward direction i.e., in the ON state and R_r (=∞) in the reverse direction i.e., in the OFF state.

Now the current „i" in the diode (or) in the load resistance R_L is given by

$i = I_m \sin \omega t$ for $0 \le \omega t \le \pi$

i=0 for $\pi \le \omega t \le 2\pi$

where $I_m = \dfrac{V_m}{R_f + R_L}$

i) Average (or) DC Output Current (I_{av} or I_{dc}):

The average dc current I_{dc} is given by

$$I_{dc} = \frac{1}{2\pi}\int_0^{2\pi} id(\omega t)$$

$$= \frac{1}{2\pi}\left[\int_0^{\pi} I_m \sin\omega t\, d(\omega t) + \int_{\pi}^{2\pi} 0 \times d(\omega t)\right]$$

$$= \frac{1}{2\pi}\left[I_m(-\cos\omega t)^{\pi}_{0}\right]$$

$$= \frac{1}{2\pi}\left[I_m(+1-(-1))\right]$$

$$= \frac{I_m}{\pi} = 0.318\ I_m$$

Substituting the value of I_m, we get $I_{dc} = \frac{V_m}{\pi(R_f + R_L)}$

If $R_L >> R_f$ then $I_{dc} = \frac{V_m}{\pi R_L} = 0.318\ \frac{V_m}{R_L}$

ii) Average (or) DC Output Voltage (V_{av} or V_{dc}):

The average dc voltage is given by

$$V_{dc} = I_{dc} \times R_L = \frac{I_m}{\pi} \times R_L = \frac{V_m R_L}{\pi(R_f + R_L)}$$

$$\Rightarrow V_{dc} = \frac{V_m R_L}{\pi(R_f + R_L)}$$

If $R_L >> R_f$ then $V_{dc} = \frac{V_m}{\pi} = 0.318\ I_m \qquad \therefore V_{dc} = \frac{V_m}{\pi}$

iii) R.M.S. Output Current (I_{rms}):

The value of the R.M.S. current is given by

$$I_{rms} = \left[\frac{1}{2\pi}\int_0^{2\pi} i^2 d(\omega t)\right]^{\frac{1}{2}}$$

$$= \left[\frac{1}{2\pi}\int_0^{\pi} I_m^2 \sin^2\omega t.d(\omega t) + \frac{1}{2\pi}\int_{\pi}^{2\pi} 0.d(\omega t)\right]^{\frac{1}{2}}$$

$$= \left[\frac{I_m^2}{2\pi} \int_0^{\pi} \left(\frac{1-\cos\omega t}{2} \right) d(\omega t) \right]^{\frac{1}{2}}$$

$$= \left[\frac{I_m^2}{4\pi} \left\{ (\omega t) - \frac{1}{2} \sin \omega t \right\}_0^{\pi} \right]^{\frac{1}{2}}$$

$$= \left[\frac{I_m^2}{4\pi} \left\{ \pi - 0 - \frac{\sin 2\pi}{2} + \sin 0 \right\} \right]^{\frac{1}{2}}$$

$$= \left(\frac{I_m^2}{4} \right)^{\frac{1}{2}} = \frac{I_m}{2}$$

$$\therefore I_{rms} = \frac{I_m}{2} \quad I_{rms} = \frac{V_m}{2\left(R_f + R_L\right)}$$

iv) R.M.S. Output Voltage (V_{rms}):

R.M.S. voltage across the load is given by

$$V_{rms} = I_{rms} \times R_L = \frac{V_m R_L}{2\left(R_f + R_L\right)} = \frac{V_m}{2\left(1 + \frac{R_f}{R_L}\right)}$$

If $R_L >> R_f$ then $V_{rms} = \frac{V_m}{2}$

v) Rectifier efficiency (η):

The rectifier efficiency is defined as the ration of d.c. output power to the a.c. input power i.e.,

$$\therefore \eta = \frac{P_{dc}}{P_{ac}}$$

$$P_{dc} = I_{dc}^2 R_L = \frac{I_m^2 R_L}{\pi^2}$$

$$P_{ac} = I_{rms}^2 \left(R_L + R_f\right) = \frac{I_m^2}{4}\left(R_L + R_f\right)$$

$$\therefore \eta = \frac{P_{dc}}{P_{ac}} = \frac{I_m^2 R_L}{\pi^2} \times \frac{4}{I_m^2\left(R_L + R_f\right)} = \frac{4}{\pi^2}\left(\frac{R_L}{R_L + R_f}\right)$$

$$\Rightarrow \eta = \frac{4}{\pi^2} \times \frac{1}{\left(1 + \frac{R_f}{R_L}\right)} = \frac{0.406}{1 + \frac{R_f}{R_L}}$$

$$\Rightarrow \%\eta = \frac{40.6}{1 + \frac{R_f}{R_L}}$$

Theoretically the maximum value of rectifier efficiency of a half-wave rectifier is 40.6% when $\frac{R_f}{R_L} = 0$.

vi) Ripple Factor (γ):

The ripple factor γ is given by

$$\gamma = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1} \qquad \textbf{(or)} \qquad \gamma = \sqrt{\left(\frac{V_{rms}}{V_{dc}}\right)^2 - 1}$$

$$\therefore \gamma = \sqrt{\left(\frac{I_m/2}{I_m/\pi}\right)^2 - 1} = \sqrt{\left(\frac{\pi}{2}\right)^2 - 1} \textbf{ = 1.21}$$

$$\Rightarrow \gamma = 1.21$$

vii) Regulation:

The variation of d.c. output voltage as a function of d.c. load current is called *regulation.*

The variation of V_{dc} with I_{dc} for a half-wave rectifier is obtained as follows:

$$I_{dc} = \frac{I_m}{\pi} = \frac{V_m/\pi}{R_f + R_L}$$

But $V_{dc} = I_{dc} \times R_L$

$$V_{dc} = \frac{V_m}{\pi}\left[\frac{R_L}{R_f + R_L}\right] = \frac{V_m}{\pi}\left[1 - \frac{R_f}{R_f + R_L}\right]$$

$$= \frac{V_m}{\pi} - I_{dc}R_f$$

$$\therefore V_{dc} = \frac{V_m}{\pi} - I_{dc}R_f$$

This result shows that V_{dc} equals $\frac{V_m}{\pi}$ at no load and that the dc voltage decreases linearly with an increase in dc output current. The larger the magnitude of the diode forward resistance, the greater is this decrease for a given current change.

viii) Transformer Utilization Factor (UTF):

The d.c. power to be delivered to the load in a rectifier circuit decides the rating of the transformer used in the circuit. So, transformer utilization factor is defined as

$$\therefore TUF = \frac{P_{dc}}{P_{ac(rated)}}$$

The factor which indicates how much is the utilization of the transformer in the circuit is called Transformer Utilization Factor (TUF).

The a.c. power rating of transformer **= V_{rms} I_{rms}**

The secondary voltage is purely sinusoidal hence its rms value is $\frac{1}{\sqrt{2}}$ times maximum while the current is half sinusoidal hence its rms value is $\frac{1}{2}$ of the maximum.

$$\therefore P_{ac(rated)} = \frac{V_m}{\sqrt{2}} \times \frac{I_m}{2} = \frac{V_m I_m}{2\sqrt{2}}$$

The d.c. power delivered to the load $= I_{dc}^2 R_L = \left(\frac{I_m}{\pi}\right)^2 R_L$

$$\therefore TUF = \frac{P_{dc}}{P_{ac(rated)}}$$

$$= \frac{\left(\frac{I_m}{\pi}\right)^2 R_L}{\frac{V_m I_m}{2\sqrt{2}}} = \frac{2\sqrt{2}}{\pi^2} \cdot \frac{I_m^2 \cdot R_L}{V_m I_m} \qquad \left(\because V_m \approx I_m R_L\right)$$

$$= \frac{2\sqrt{2}}{\pi^2} \cdot \frac{I_m R_L}{I_m R_L}$$

$$= 0.287$$

$$\therefore TUF = 0.287$$

The value of TUF is low which shows that in half-wave circuit, the transformer is not fully utilized.

If the transformer rating is 1 KVA (1000VA) then the half-wave rectifier can deliver 1000 X 0.287 = 287 watts to resistance load.

ix) Peak Inverse Voltage (PIV):

It is defined as the maximum reverse voltage that a diode can withstand without destroying the junction. The peak inverse voltage across a diode is the peak of the negative half-cycle. For half-wave rectifier, PIV is **V_m**.

x) Form factor (F):

The Form Factor F is defined as

F = rms value / average value

$$F = \frac{\mathrm{Im}/2}{\mathrm{Im}/\pi}$$

$$F = \frac{0.5\,\mathrm{Im}}{0.318\,\mathrm{Im}} = 1.57$$

xi) Peak Factor (P):

The peak factor P is defined as

P= Peak Value / rms value $= \frac{V_m}{V_m/2} = 2$ **P = 2**

Disadvantages of Half-Wave Rectifier:

1. The ripple factor is high.
2. The efficiency is low.
3. The Transformer Utilization factor is low.

Because of all these disadvantages, the half-wave rectifier circuit is normally not used as a power rectifier circuit.

Problems from previous external question paper:

1. A diode whose internal resistance is 20Ω is to supply power to a 100Ω load from 110V(rms) source pf supply. Calculate (a) peak load current (b) the dc load current (c) the ac load current (d) the percentage regulation from no load to full load.

Solution:

Given a half-wave rectifier circuit R_f=20Ω, R_L=100Ω

Given an ac source with rms voltage of 110V, therefore the maximum amplitude of sinusoidal input is given by

$$\mathbf{V_m} = \sqrt{2} \times V_{rms} = \sqrt{2} \times 110 = \mathbf{155.56V}.$$

(a) Peak load current : $\mathrm{I_m} = \frac{V_m}{R_f + R_L} \Rightarrow \mathrm{I_m} = \frac{155.56}{120} = \mathbf{1.29A}$

(b) The dc load current : $\mathrm{I}_{dc} = \frac{I_m}{\pi} = \mathbf{0.41A}$

(c) The ac load current : $\mathrm{I}_{rms} = \frac{I_m}{2} = \mathbf{0.645A}$

(d) $V_{no\text{-}load}$: $\frac{V_m}{\pi} = \frac{155.56}{\pi} = \mathbf{49.51\ V}$

$V_{full\text{-}load}$: $V_{dc} = \frac{V_m}{\pi} - I_{dc} R_f = \mathbf{41.26\ V}$

% Regulation $= \frac{V_{no-load} - V_{full-load}}{V_{full-load}} \times 100 = \mathbf{19.97\%}$

2. A diode has an internal resistance of 20Ω and 1000Ω load from 110V(rms) source pf supply. Calculate (a) the efficiency of rectification (b) the percentage regulation from no load to full load.

Solution:

Given a half-wave rectifier circuit R_f=20Ω, R_L=1000Ω

Given an ac source with rms voltage of 110V, therefore the maximum amplitude of sinusoidal input is given by

$$\mathbf{V_m} = \sqrt{2} \times V_{rms} = \sqrt{2} \text{ x } 110 = 155.56\text{V}.$$

(a) % Efficiency (η) = $\dfrac{40.6}{1+\dfrac{20}{100}} = \dfrac{40.6}{1.02}$ **= 39.8%.**

(b) Peak load current : $I_m = \dfrac{V_m}{R_f + R_L} = \dfrac{155.56}{1020} = 0.1525$ A

= 152.5 mA

The dc load current : $I_{dc} = \dfrac{I_m}{\pi}$ = **48.54 mA**

$\mathbf{V_{no\text{-}load}}$ **=** $\dfrac{V_m}{\pi} = \dfrac{155.56}{\pi}$ **= 49.51 V**

$\mathbf{V_{full\text{-}load}}$ **=** $\dfrac{V_m}{\pi} - I_{dc} R_f$ **= 49.51 – (48.54 x10^{-3} x 20)**

= 49.51 – 0.97 = 48.54 V

% Regulation **=** $\dfrac{V_{no-load} - V_{full-load}}{V_{full-load}} \times 100$

$= \dfrac{49.51 - 48.54}{48.54} \times 100$ **= 1.94 %**

3. An a.c. supply of 230V is applied to a half-wave rectifier circuit through transformer of turns ration 5:1. Assume the diode is an ideal one. The load resistance is 300Ω. Find (a) dc output voltage (b) PIV (c) maximum, and (d) average values of power delivered to the load.

Solution: (a) The transformer secondary voltage = 230/5 = 46V.

Maximum value of secondary voltage, $V_m = \sqrt{2}$ x 46 = 65V.

Therefore, dc output voltage, $V_{dc} = \dfrac{V_m}{\pi} = \dfrac{65}{\pi}$ **= 20.7 V**

(b) PIV of a diode : V_m = **65V**

(c) Maximum value of load current, $I_m = \dfrac{V_m}{R_L} = \dfrac{65}{300}$ **= 0.217 A**

Therefore, maximum value of power delivered to the load,

$\mathbf{P_m} = I_m^2 \text{ x } R_L = (0.217)^2 \text{ x } 300 =$ **14.1W**

(d) The average value of load current, $I_{dc} = \frac{V_{dc}}{R_L} = \frac{20.7}{300}$ **= 0.069A**

Therefore, average value of power delivered to the load,

$$\mathbf{P_{dc}} = I_{dc}^2 \times R_L = (0.069)^2 \times 300 = \mathbf{1.43W}$$

FULL – WAVE RECTIFIER

A full-wave rectifier converts an ac voltage into a pulsating dc voltage using both half cycles of the applied ac voltage. In order to rectify both the half cycles of ac input, two diodes are used in this circuit. The diodes feed a common load R_L with the help of a center-tap transformer.

A center-tap transformer is the one which produces two sinusoidal waveforms of same magnitude and frequency but out of phase with respect to the ground in the secondary winding of the transformer. The full wave rectifier is shown in the figure below.

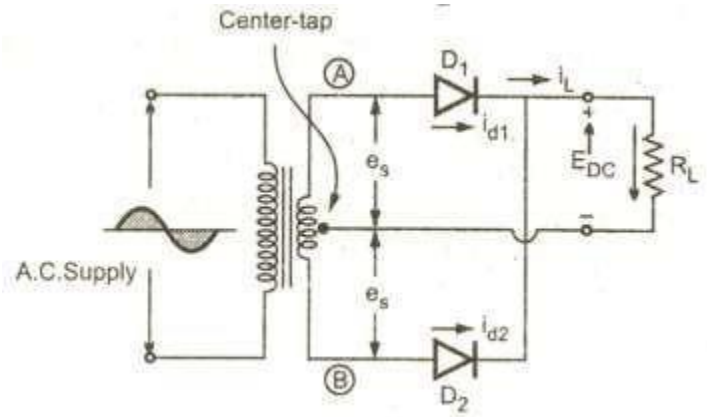


Fig. Full-Wave Rectifier.

The individual diode currents and the load current waveforms are shown in figure below:

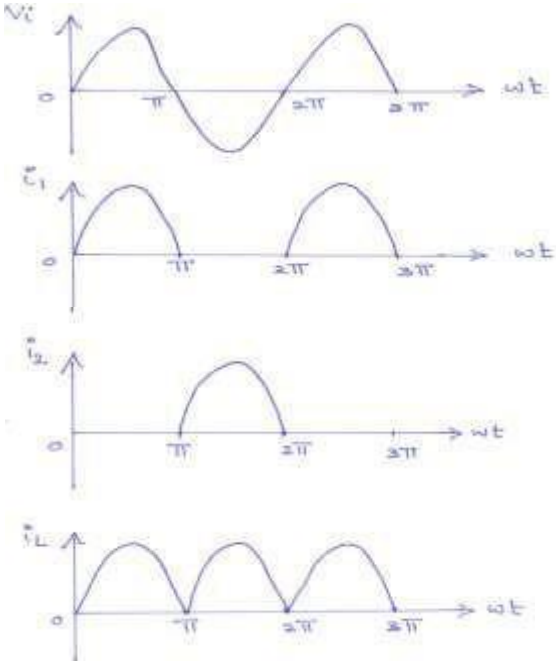


Fig. The input voltage, the individual diode currents and the load current waveforms.

Operation:

During positive half of the input signal, anode of diode D_1 becomes positive and at the same time the anode of diode D_2 becomes negative. Hence D_1 conducts and D_2 does not conduct. The load current flows through D_1 and the voltage drop across R_L will be equal to the input voltage.

During the negative half cycle of the input, the anode of D_1 becomes negative and the anode of D_2 becomes positive. Hence, D_1 does not conduct and D_2 conducts. The load current flows through D_2 and the voltage drop across R_L will be equal to the input voltage.

It is noted that the load current flows in the both the half cycles of ac voltage and in the same direction through the load resistance.

Analysis:

Let a sinusoidal voltage V_i be applied to the input of a rectifier. It is given by $V_i=V_m \sin\omega t$ The current i_1 though D_1 and load resistor R_L is given by

$i_1 = I_m \sin\omega t$ for $0 \le \omega t \le \pi$

$i_1 = 0$ for $\pi \le \omega t \le 2\pi$ Where $I_m = \dfrac{V_m}{R_f + R_L}$

Similarly, the current i_2 through diode D_2 and load resistor R_L is given by

$i_2 = 0$ for $0 \le \omega t \le \pi$

$i_2 = I_m \sin\omega t$ for $\pi \le \omega t \le 2\pi$

Therefore, the total current flowing through R_L is the sum of the two currents i_1 and i_2.

i.e., $i_L = i_1 + i_2$.

i) Average (or) DC Output Current (I_{av} or I_{dc}):

The average dc current I_{dc} is given by

$$I_{dc} = \frac{1}{2\pi}\int_0^{2\pi} i\, d(\omega t) \quad \frac{1}{2\pi}\int_0^{2\pi} i\, d(\omega t)$$

$$= \frac{1}{2\pi}\left[\int_0^{\pi} I_m \sin\omega t\, d(\omega t) + 0 + 0 + \int_{\pi}^{2\pi} I_m \sin\omega t\, d(\omega t)\right]$$

$$= \frac{I_m}{\pi} + \frac{I_m}{\pi}$$

$$= \frac{2I_m}{\pi} = 0.318\ I_m$$

$$\therefore I_{dc} = \frac{2I_m}{\pi}$$

Substituting the value of I_m, we get $I_{dc} = \dfrac{2}{\pi}\dfrac{V_m}{(R_f + R_L)}$

This is double that of a Half-Wave Rectifier.

ii) Average (or) DC Output Voltage (V_{av} or V_{dc}):

The dc output voltage is given by

$$V_{dc} = I_{dc} \times R_L = \frac{2 I_m R_L}{\pi}$$

$$\Rightarrow V_{dc} = \frac{2}{\pi} \frac{V_m R_L}{R_f + R_L}$$

If $R_L >> R_f$ then $V_{dc} = \frac{2V_m}{\pi}$

iii) R.M.S. Output Current (I_{rms}):

The value of the R.M.S. current is given by

$$I_{rms} = \left[\frac{1}{2\pi} \int_0^{2\pi} i^2 \, d(\omega t) \right]^{\frac{1}{2}}$$

$$= \left[\frac{1}{2\pi} \int_0^{\pi} i_1^2 d(\omega t) + \frac{1}{2\pi} \int_{\pi}^{2\pi} i_2^2 d(\omega t) \right]^{\frac{1}{2}}$$

$$= \left[\frac{1}{2\pi} \int_0^{\pi} I_m^2 \sin^2 \omega t . d(\omega t) + \frac{1}{2\pi} \int_{\pi}^{2\pi} I_m^2 \sin^2 \omega t . d(\omega t) \right]^{\frac{1}{2}}$$

$$= \left[\frac{I_m^2}{2\pi} \int_0^{\pi} \left(\frac{1 - \cos 2\omega t}{2} \right) d(\omega t) + \frac{I_m^2}{2\pi} \int_{\pi}^{2\pi} \left(\frac{1 - \cos 2\omega t}{2} \right) d(\omega t) \right]^{\frac{1}{2}}$$

$$= \left\{ \frac{I_m^2}{4\pi} \left[\omega t - \frac{\sin 2\omega t}{\omega t} \right]_0^{\pi} + \frac{I_m^2}{4\pi} \left[\omega t - \frac{\sin 2\omega t}{\omega t} \right]_{\pi}^{2\pi} \right\}^{\frac{1}{2}}$$

$$= \left\{ \frac{I_m^2}{4\pi} [(\pi - 0) - (0)] + \frac{I_m^2}{4\pi} [(2\pi - 0) - (\pi - 0)] \right\}^{\frac{1}{2}}$$

$$= \left[\frac{I_m^2}{4\pi} \times \pi + \frac{I_m^2}{4\pi} \times \pi \right]^{\frac{1}{2}} = \left(2 \times \frac{I_m^2}{4} \right)^{\frac{1}{2}} = \frac{I_m}{\sqrt{2}}$$

$$\therefore I_{rms} = \frac{I_m}{\sqrt{2}} \quad \text{(or)} \quad I_{rms} = \frac{V_m}{\sqrt{2}(R_f + R_L)}$$

iv) R.M.S. Output Voltage (V_{rms}):

R.M.S. voltage across the load is given by

$$V_{rms} = I_{rms} \times R_L = \frac{V_m}{\sqrt{2}\left(R_f + R_L\right)} \times R_L$$

$$\Rightarrow V_{rms} = \frac{V_m}{\sqrt{2}\left(1 + \frac{R_f}{R_L}\right)}$$

If $R_L >> R_f$ then $V_{rms} = \frac{V_m}{\sqrt{2}}$

v) Rectifier efficiency (η):

The rectifier efficiency is defined as the ration of d.c. output power to the a.c. input power

i.e., $\therefore \eta = \frac{P_{dc}}{P_{ac}}$

$$P_{dc} = I_{dc}^2 R_L = \frac{4I_m^2 R_L}{\pi^2}$$

$$P_{ac} = I_{rms}^2 \left(R_L + R_f\right) = \frac{I_m^2}{2}\left(R_L + R_f\right)$$

$$\therefore \eta = \frac{P_{dc}}{P_{ac}} = \frac{4I_m^2 R_L}{\pi^2} \times \frac{2}{I_m^2\left(R_L + R_f\right)}$$

$$= \frac{8}{\pi^2}\left(\frac{R_L}{R_L + R_f}\right) = \frac{8}{\pi^2\left(1 + \frac{R_f}{R_L}\right)} = \frac{0.812}{1 + \frac{R_f}{R_L}}$$

$$\Rightarrow \%\eta = \frac{81.2}{1 + \frac{R_f}{R_L}}$$

Theoretically the maximum value of rectifier efficiency of a full-wave rectifier is 81.2% when $\frac{R_f}{R_L} = 0$. Thus full-wave rectifier has efficiency twice that of half-wave rectifier.

vi) Ripple Factor (γ) :

The ripple factor, γ is given by

$$\therefore \gamma = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1} \qquad \textbf{(or)} \qquad \therefore \gamma = \sqrt{\left(\frac{V_{rms}}{V_{dc}}\right)^2 - 1}$$

$$\therefore \gamma = \sqrt{\left(\frac{I_m}{\sqrt{2}} \times \frac{\pi}{2I_m}\right)^2 - 1} = \sqrt{\left(\frac{\pi}{2\sqrt{2}}\right)^2 - 1} = \textbf{0.48}$$

$$\Rightarrow \gamma = 0.48$$

vii) <u>Regulation:</u>

The variation of V_{dc} with I_{dc} for a full-wave rectifier is obtained as follows:

$$V_{dc} = I_{dc} \times R_L$$

$$= \frac{2I_m}{\pi} R_L \qquad \left(\because I_{dc} = \frac{2I_m}{\pi}\right)$$

$$= \frac{2V_m R_L}{\pi\left(R_L + R_f\right)}$$

$$= \frac{2V_m}{\pi}\left[1 - \frac{R_f}{R_f + R_L}\right] \qquad = \frac{2V_m}{\pi} - I_{dc} R_f$$

$$\therefore V_{dc} = \frac{2V_m}{\pi} - I_{dc} R_f$$

The percentage regulation of the Full-wave rectifier is given by

$$\% \text{ Regulation} = \frac{V_{no-load} - V_{full-load}}{V_{full-load}} \times 100$$

$$= \frac{\frac{2V_m}{\pi} - \left(\frac{2V_m}{\pi} - I_{dc} R_f\right)}{\frac{2V_m}{\pi} - I_{dc} R_f} \times 100 \qquad = \frac{I_{dc} R_f}{I_{dc} R_L} \times 100$$

$$\Rightarrow \% \text{ Regulation} = \frac{R_f}{R_L} \times 100$$

viii) Transformer Utilization Factor (UTF):

The average TUF in full-wave rectifying circuit is determined by considering the primary and secondary winding separately. There are two secondaries here. Each secondary is associated with one diode. This is just similar to secondary of half-wave rectifier. Each secondary has TUF as 0.287.

TUF of primary = P_{dc} / Volt-Amp rating of primary

$$\therefore (TUF)_P = \frac{I_{dc}^2 . R_L}{\frac{I_m}{\sqrt{2}} . \frac{V_m}{\sqrt{2}}} = \frac{\left(\frac{I_m}{2}\right)^2 . RL}{\frac{V_m I_m}{2}}$$

$$= \frac{4I_m^2}{\pi^2} . \frac{2R_L}{2I_m\left(R_f + R_L\right)} = \frac{8}{\pi^2}\left(\frac{1}{1+\frac{R_f}{R_L}}\right)$$

If $R_L >> R_f$ then (TUF)p = $\frac{8}{\pi^2}$ = 0.812.

$$\therefore (TUF)_{av} = P_{dc} / \text{ V-A rating of transformer}$$

$$= \frac{(TUF)p + (TUF)s + (TUF)s}{3}$$

$$= \frac{0.812 + 0.287 + 0.287}{3} = 0.693$$

$$\therefore (TUF) = \mathbf{0.693}$$

ix) Peak Inverse Voltage (PIV):

Peak Inverse Voltage is the maximum possible voltage across a diode when it is reverse biased. Consider that diode D_1 is in the forward biased i.e., conducting and diode D_2 is reverse biased i.e., non-conducting. In this case a voltage V_m is developed across the load resistor R_L. Now the voltage across diode D_2 is the sum of the voltages across load resistor R_L and voltage across the lower half of transformer secondary V_m. Hence PIV of diode $D_2 = V_m + V_m = 2V_m$.

Similarly PIV of diode D_1 is $2V_m$.

x) Form factor (F):

The Form Factor F is defined as F = rms value / average value

$$F = \frac{Im/\sqrt{2}}{2Im/\pi} = \frac{0.707 I_m}{0.63 I_m} = 1.12$$ **F=1.12**

xi) Peak Factor (P):

The peak factor P is defined as

P= Peak Value / rms value $= \frac{I_m}{I_m/\sqrt{2}} = \sqrt{2} = 1.414$ **P = 1.414**

Problems from previous External Question Paper:

4) A Full-Wave rectifier circuit is fed from a transformer having a center-tapped secondary winding. The rms voltage from wither end of secondary to center tap is 30V. if the diode forward resistance is 5Ω and that of the secondary is 10Ω for a load of 900Ω,
Calculate:

i) Power delivered to load,
ii) % regulation at full-load,
iii) Efficiency at full-load and
iv) TUF of secondary.

Solution: Given V_{rms} = 30V, R_f =5Ω, Rs=10Ω, R_L=900Ω

But $V_{rms} = \frac{V_m}{\sqrt{2}} \Rightarrow V_m = 30 \times \sqrt{2}$ = 42.426 V.

$$I_m = \frac{V_m}{R_f + R_S + R_L} = \frac{30\sqrt{2}}{5 + 10 + 900} = 46.36 \text{ mA.}$$

$$I_{dc} = \frac{2I_m}{\pi} = \frac{2 \times 46.36}{\pi} = 29.5\text{mA}$$

i) Power delivered to the load = $I_{dc}^2 R_L = \left(29.5 \times 10^{-3}\right)^2 \times 900$ **= 0.783W**

ii) % Regulation at full-load = $\frac{V_{no-load} - V_{full-load}}{V_{full-load}} \times 100$

$V_{no-load} = \frac{2V_m}{\pi} = \frac{2 \times 42.426}{\pi}$ **= 27.02 V.**

$V_{full-load} = I_{dc} R_L$ = 29.5 x 10^{-3} x 900 = 26.5 V

% Regulation = $\frac{27.02 - 26.5}{26.5} \times 100$ **= 1.96 %**

iii) Efficiency of Rectification = $\frac{81.2}{1 + \frac{R_f + R_S}{R_L}} = \frac{81.2}{1 + \frac{15}{900}}$ **= 79.8%**

iv) TUF of secondary = DC power output / secondary ac rating

Transformer secondary rating = V_{rms} I_{rms} = $30 \times \frac{46.36}{\sqrt{2}} \times 10^{-3}$ W

$P_{dc} = I_{dc}^2 R_L$

$\therefore TUF = \frac{0.783}{30 \times \frac{46.36}{\sqrt{2}} \times 10^{-3}}$ **= 0.796**

5) A Full-wave rectifier circuit uses two silicon diodes with a forward resistance of 20Ω each. A dc voltmeter connected across the load of 1kΩ reads 55.4volts. Calculate

i) I_{RMS},
ii) Average voltage across each diode,
iii) Ripple factor, and
iv) Transformer secondary voltage rating.

Solution:

Given R_f =20Ω, R_L=1kΩ, V_{dc} = 55.4V

For a FWR $V_{dc} = \frac{2V_m}{\pi}$ $\quad \therefore V_m = \frac{55.4\times\pi}{2}$ **= 86.9 V**

$$I_m = \frac{V_m}{R_f + R_L}$$ **=0.08519A**

i) $I_{rms} = \frac{I_m}{\sqrt{2}}$ = 0.06024A

ii) V= 86.9/2 = 43.45V

iii) Ripple factor

$$\gamma = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$$, $I_{dc} = \frac{2I_m}{\pi}$ **=0.05423A** $I_{rms} = \frac{I_m}{\sqrt{2}}$ **=0.06024A**

$$\therefore \gamma = 0.48$$

iv) Transformer secondary voltage rating: $V_{rms} = \frac{V_m}{\sqrt{2}} = \frac{86.9}{\sqrt{2}}$ **= 61.49 Volts.**

6) A 230V, 60Hz voltage is applied to the primary of a 5:1 step down, center tapped transformer used in the Full-wave rectifier having a load of 900Ω. If the diode resistance and the secondary coil resistance together has a resistance of 100Ω. Determine:

i) dc voltage across the load,
ii) dc current flowing through the load,
iii) dc power delivered to the load, and
iv) ripple voltage and its frequency.

Solution: Given $V_{p(rms)}$ = 230V

$$\frac{N_2}{N_1} = \frac{2V_{S(rms)}}{V_{P(rms)}} \qquad \Rightarrow \frac{1}{5} = \frac{2V_{S(rms)}}{230}$$

$$\Rightarrow V_{S(rms)}$$ = 23V

Given R_L =900Ω, R_f + Rs =100Ω

$$I_m = \frac{V_{sm}}{R_f + R_S + R_L} = \frac{\sqrt{2}V_{s(rms)}}{R_f + R_S + R_L} = \frac{\sqrt{2}\times 23}{900+100}$$ **= 0.03252 Amp.**

$$\therefore I_{dc} = \frac{2I_m}{\pi} = \frac{2\times 0.03252}{\pi}$$ **= 0.0207 Amp.**

i) $V_{DC} = I_{DC} R_L = 0.0207 \times 100 =$ **18.6365 Volts.**

ii) $I_{DC} =$ **0.0207 Amp.**

iii) $P_{dc} = I_{dc}^2 R_L$ (or) $V_{DC} I_{DC} =$ **0.3857 Watts.**

iv) $PIV = 2V_{sm} = 2 \times \sqrt{2} \times 23 =$ **65.0538 Volts**

v) Ripple factor $= 0.482 = \frac{V_{r(rms)}}{V_{DC}}$

Therefore, ripple voltage = $V_{r(rms)}$ = 0.482 x 18.6365

= 8.9827 Volts.

Frequency of ripple = 2f = 2x60 = **120 Hz**

Bridge Rectifier

The full-wave rectifier circuit requires a center tapped transformer where only one half of the total ac voltage of the transformer secondary winding is utilized to convert into dc output. The need of the center tapped transformer in a Full-wave rectifier is eliminated in the bridge rectifier. The bridge rectifier circuit has four diodes connected to form a bridge. The ac input voltage us applied to diagonally opposite ends of the bridge. The load resistance is connected between the other two ends of the bridge. The bridge rectifier circuits and its waveforms are shown in figure.

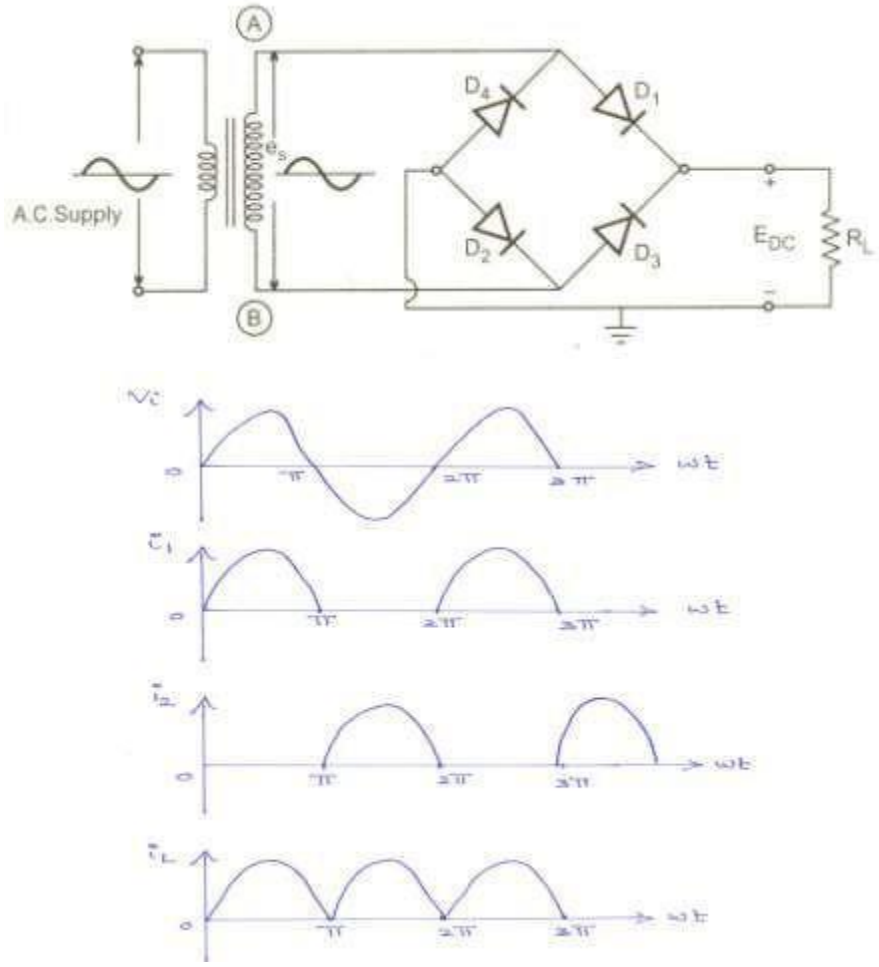


Fig. and waveforms

Operation:

For the positive half cycle of the input ac voltage diodes D_1 and D_3 conduct, whereas diodes D_2 and D_4 do not conduct. The conducting diodes will be in series through the load resistance R_L, so the load current flows through the R_L.

During the negative half cycle of the input ac voltage diodes D_2 and D_4 conduct, whereas diodes D_1 and D_3 do not conduct.

The conducting diodes D_2 and D_4 will be in series through the load resistance R_L and the current flows through the R_L, in the same direction as in the previous half cycle. Thus a bidirectional wave is converted into a unidirectional wave.

Analysis:

The average values of output voltage and load current, the rms values of voltage and current, the ripple factor and rectifier efficiency are the same as for as center tapped full-wave rectifier.

Hence,

$$V_{dc} = \frac{2V_m}{\pi}$$

$$I_{dc} = \frac{2I_m}{\pi} \qquad I_m = \frac{V_m}{R_f + R_L}$$

$$V_{rms} = \frac{V_m}{\sqrt{2}} \qquad I_{rms} = \frac{I_m}{\sqrt{2}}$$

Since the each half cycle two diodes conduct simultaneously

$$\gamma = 0.48$$

$$\eta = \frac{81.2}{1 + \frac{2R_f}{R_L}}$$

The transformer utilization factor (TUF) of primary and secondary will be the same as there is always through primary and secondary.

TUF of secondary = P_{dc} / V-A rating of secondary

$$= \frac{I_{dc}^2 R_L}{V_{rms} I_{rms}} = \frac{\left(\frac{2I_m}{\pi}\right)^2 R_L}{\left(\frac{V_m}{\sqrt{2}}\right)\left(\frac{I_m}{\sqrt{2}}\right)} = \mathbf{0.812}$$

TUF in case of secondary of primary of FWR is 0.812

$$\therefore (TUF)_{av} = \frac{(TUF)p + (TUF)s}{2}$$

$$= \frac{0.812 + 0.812}{2} = \mathbf{0.812}$$

$$\therefore TUF = \mathbf{0.812}$$

The reverse voltage appearing across the reverse biased diodes is $2V_m$, but two diodes are sharing it, therefore the PIV rating of the diodes is V_m.

Advantages of Bridge rectifier circuit:

1) No center-tapped transformer is required.
2) The TUF is considerably high.
3) PIV is reduced across the diode.

Disadvantages of Bridge rectifier circuit:

The only disadvantage of bridge rectifier is the use of four diodes as compared to two diodes for center-tapped FWR. This reduces the output voltage.

Problems:

7. A bridge rectifier uses four identical diodes having forward resistance of 5Ω and the secondary voltage of $30V_{(rms)}$. Determine the dc output voltage for I_{DC}=200mA and the value of the ripple voltage.

Solution: $V_{s(rms)}$=30V, R_S=5Ω, R_f=5Ω, I_{DC}=200mA

Now $I_{DC} = 2\frac{I_m}{\pi}$

$$\therefore I_m = \frac{200\times10^{-3}\times\pi}{2} = 0.3415 \text{ Amp.}$$

But $$I_m = \frac{V_{sm}}{R_S + 2R_f + R_L} = \frac{\sqrt{2}V_{s(rms)}}{R_S + 2R_f + R_L}$$

$$\Rightarrow 0.3415 = \frac{\sqrt{2}\times 30}{5+(2\times5)+R_L}$$

$\Rightarrow R_L = 120.051\Omega \approx 120\Omega$

$V_{DC} = I_{DC} R_L = 200 \times10^{-3} \times120 = 24$Volts

Ripple factor = $\frac{V_{r(rms)}}{V_{dc}}$

For Bridge rectifier, ripple factor = 0.482

$\therefore V_{r(rms)}$ = rms value of ripple voltage

= Vdcx0.482

= 24x0.482

=11.568 Volts

8. In a bridge rectifier the transformer is connected to 220V, 60Hz mains and the turns ratio of the step down transformer is 11:1. Assuming the diode to be ideal, find:

i) I_{dc}
ii) voltage across the load
iii) PIV assume load resistance to be 1kΩ

Solution: $\frac{N_2}{N_1} = \frac{1}{11}$, $V_{p(rms)}$ = 220V, f=60Hz, R_L= 1kΩ

$$\frac{N_2}{N_1} = \frac{V_{S(rms)}}{V_{P(rms)}} \qquad \Rightarrow \frac{1}{11} = \frac{V_{S(rms)}}{220} \Rightarrow V_{S(rms)} = \frac{220}{11} = 20V$$

$$V_{sm} = \sqrt{2}Vs(rms)$$

i) $I_m = \frac{V_{sm}}{R_L} = \frac{28.2842}{1\times10^{-3}} = 28.2842$ mA

$$\therefore I_{dc} = \frac{2I_m}{\pi} = \textbf{18 mA}$$

ii) $V_{dc} = I_{dc} R_L = 18x10^{-3}Xx10^{-3} =$ **18 Volts**

iv) PIV = V_{sm} = **28.2842 Volts**

Comparison of Rectifier circuits:

Sl. No.	Parameter	Half-Wave Rectifier	Full-Wave Rectifier	Bridge Rectifier
1.	Number of diodes	1	2	4
2.	Average dc current, I_{dc}	$\frac{I_m}{\pi}$	$\frac{2I_m}{\pi}$	$\frac{2I_m}{\pi}$
3.	Average dc voltage, V_{dc}	$\frac{V_{sm}}{\pi}$	$\frac{2V_{sm}}{\pi}$	$\frac{2V_{sm}}{\pi}$
4.	RMS current, I_{rms}	$\frac{I_m}{2}$	$\frac{I_m}{\sqrt{2}}$	$\frac{I_m}{\sqrt{2}}$
5.	DC Power output, P_{dc}	$\frac{I_m^2 R_L}{\pi^2}$	$\frac{4I_m^2 R_L}{\pi^2}$	$\frac{4I_m^2 R_L}{\pi^2}$
6.	AC Power input, P_{AC}	$\frac{I_m^2\left(R_L + R_f + R_S\right)}{4}$	$\frac{I_m^2\left(R_f + R_S + R_L\right)}{2}$	$\frac{I_m^2\left(2R_f + R_S + R_L\right)}{2}$
7.	Max. rectifier efficiency (η)	40.6%	81.2%	81.2%
8.	Ripple factor (γ)	1.21	0.482	0.482
9.	PIV	V_m	$2V_m$	$2V_m$
10.	TUF	0.287	0.693	0.812
11.	Max. load current (I_m)	$\frac{V_{sm}}{R_S + R_f + R_L}$	$\frac{V_{sm}}{R_S + R_f + R_L}$	$\frac{V_{sm}}{R_S + 2R_f + R_L}$

The Harmonic components in Rectifier circuits:

An analytical representation of the output current wave in a rectifier is obtained by means of a Fourier series. The result of such an analysis for the half-wave rectifier circuit leads to the following expression for the current waveform.

$$i = \mathrm{I}_m \left[\frac{1}{\pi} + \frac{1}{2}\sin\omega t - \frac{2}{\pi} \sum_{K=2,4,6.....} \frac{\cos\omega t}{(K+1)(K-1)} \right]$$

The lowest angular frequency present in this expression is that of the primary source of the a.c. power. Except for this single term of angular frequency (ω), all other terms in the above expression are even harmonics of the power frequency.

We know that the full-wave circuit consists essentially of two half-wave circuits which are so arranged that one circuit conducts during one half cycle and the second operates during the second half cycle. That is, the currents are functionally related by the expression $i_1(\alpha) = i_2(\alpha + \pi)$.

Therefore the total load current is $i=i_1+i_2$.

The expression for the output current waveform of the full wave rectifier circuit is of the form

$$i = \mathrm{I}_m \left[\frac{2}{\pi} - \frac{4}{\pi} \sum_{K=2,4,6.....} \frac{\cos K\omega t}{(K+1)(K-1)} \right]$$

In the above equation, we observe that the fundamental angular frequency (ω) has been eliminated from the equation. The lowest frequency in the output is being 2ω, which is a second harmonic term. This offers a definite advantage in the effectiveness of filtering of the output.

FILTERS

The output of a half-wave (or) full-wave rectifier circuit is not pure d.c., but it contains fluctuations (or) ripple, which are undesired. To minimize the ripple content in the output, filter circuits are used. These circuits are connected between the rectifier and load. Ideally, the output of the filter should be pure d.c. practically, the filter circuit will try to minimize the ripple at the output, as far as possible. Basically, the ripple is ac, i.e., varying with time, while dc is a constant w.r.t. time.

Hence in order to separate dc from ripple, the filter circuit should use components which have widely different impedance for ac and dc. Two such components are inductance and capacitance. Ideally, the inductance acts as a short circuit for dc, but it has large impedance for ac.

Similarly, the capacitor acts as open for dc if the value of capacitance is sufficiently large enough. Hence, in a filter circuit, the inductance is always connected in series with the load, and the capacitance is connected in parallel to the load.

Definition of a Filter:

Filter is an electronic circuit composed of a capacitor, inductor (or) combination of both and connected between the rectifier and the load so as to convert pulsating dc to pure dc.

The different types of filters are:

1) Inductor Filter,
2) Capacitor Filter,
3) LC (or) L-Section Filter, and
4) CLC (or) ∏-section Filter.

Inductor Filter:

Half-Wave rectifier with series Inductor Filter:

The Inductor filter for half-wave rectifier is shown in figure below.

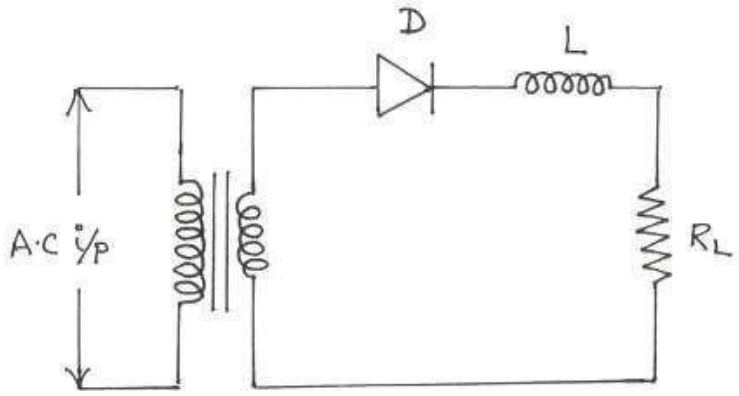


Fig. Series Inductor filter for HWR.

In this filter the inductor (choke) is connected in series with the load. The operation of the inductor filter depends upon the property of the inductance to oppose any change of current that may flow through it.

Expression for ripple factor:

For a half-wave rectifier, the output current is given by,

$$i = I_m \left[\frac{1}{\pi} + \frac{1}{2}\sin\omega t - \frac{2}{\pi} \sum_{\substack{K=even \\ K\neq 0}} \frac{\cos\omega t}{(K+1)(K-1)} \right]$$

$$i = \frac{I_m}{\pi} + \frac{I_m}{2}\sin\omega t - \frac{2I_m}{\pi}\left[\frac{\cos 2\omega t}{3} + \frac{\cos 4\omega t}{15} + ...\right] \quad \text{..... (1)}$$

Neglecting the higher order terms, we have

$$I_{dc} = \frac{I_m}{\pi} = \frac{V_m}{\pi R_L} \quad \text{..... (2)}$$

If I_1 be the rms value of fundamental component of current, then

$$I_{dc} = \frac{I_m}{2\sqrt{2}} = \frac{V_m}{2\sqrt{2}\left(R_L + j\omega L\right)} = \frac{V_m}{2\sqrt{2}\left(R_L^2 + j\omega^2 L^2\right)^{\frac{1}{2}}} \quad \text{.....(3)}$$

At operating frequency, the reactance offered by inductance „L" is very large compared to R_L (i.e., $\omega L >> R_L$) and hence R_L can be neglected.

$$\therefore I_1 = \frac{V_m}{2\sqrt{2}\omega L} \quad \text{.....(4)}$$

If I_2 be rms value of second harmonic,

Then $$\therefore I_2 = \frac{2I_m}{3\sqrt{2}\pi} = \frac{2V_m}{3\sqrt{2}\pi\left[R^2 + 4\omega^2 L^2\right]^{\frac{1}{2}}} = \frac{V_m}{3\sqrt{2}\pi\omega L} \quad \left(\because R_L << \omega L\right) \text{..... (5)}$$

If I_{ac} be the rms value of all current components, then $I_{ac} = \sqrt{I_1^2 + I_2^2}$

Now, $\gamma = \frac{V_{ac}}{V_{dc}} \approx \frac{I_{ac}R_L}{I_{dc}R_L} = \frac{I_{ac}}{I_{dc}}$

$$= \frac{\sqrt{\left(\frac{V_m}{2\sqrt{2}\omega L}\right)^2 + \left(\frac{V_m}{2\sqrt{2}\pi\omega L}\right)^2}}{\frac{V_m}{\pi R_L}}$$

$$= \frac{\frac{V_m}{\omega L}\sqrt{\frac{1}{8} + \frac{1}{18\pi^2}}}{\frac{V_m}{\pi R_L}} \qquad = \frac{\pi R_L}{\omega L}\sqrt{\frac{1}{8} + \frac{1}{18\pi^2}}$$

$$= \frac{1.13R_L}{\omega L} \qquad \therefore \gamma = \frac{1.13R_L}{\omega L} \qquad \text{.....(6)}$$

Full-wave rectifier with series inductor filter:

A FWR with series inductor filter is shown in figure.

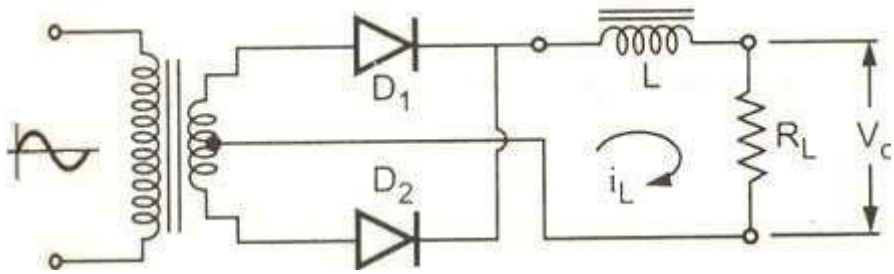


FIG. FWR with series inductor filter.

The inductor offers high impedance to a.c. variations. The inductor blocks the a.c. component and allows only t
he dc component to reach the load.

To analyze the inductor filter for a FWR, the Fourier series can be written as

$$V_O = \frac{2V_m}{\pi} - \frac{4V_m}{\pi}\left[\frac{1}{3}\cos 2\omega t + \frac{1}{15}\cos 6\omega t + \ldots\ldots\right] \qquad \text{.....(1)}$$

The dc component is $\frac{2V_m}{\pi}$

Assuming the third and higher terms contribute little output voltage is

$$V_O = \frac{2V_m}{\pi} - \frac{4V_m}{3\pi}\cos 2\omega t \qquad \text{.....(2)}$$

For the sake of simplicity, the diode drop and diode resistance are neglected because they introduce a little error. Thus for dc component, the current $I_m = \frac{V_m}{R_L}$. For ac component, the impedance of L and R_L will be in series and is given by,

$Z = \sqrt{R_L^2 + (2\omega L)^2}$, frequency of ac component = 2ω

$= \sqrt{R_L^2 + 4\omega^2 L^2}$

Thus for ac component $I_m = \dfrac{V_m}{\sqrt{R_L^2 + 4\omega^2 L^2}}$

The current flowing in a FWR is given by, $i = \dfrac{2I_m}{\pi} - \dfrac{4I_m}{3\pi}\cos 2\omega t$ .....(3)

Substituting the value of I_m for dc and ac equation (3), we get,

$$i = \frac{2V_m}{\pi R_L} - \frac{4V_m}{3\pi\sqrt{R_L^2 + 4\omega^2 L^2}}\cos(2\omega t - \phi) \quad \text{.....(4)}$$

Where Φ is the angle by which the load current lags behind the voltage. This is given by

$$\phi = \tan^{-1}\left(\frac{2\omega L}{R_L}\right) \quad \text{.....(5)}$$

Expression for Ripple Factor:

$$\gamma = \frac{I_{r,rms}}{I_{dc}}$$

From equation (4), $I_{dc} = \dfrac{2V_m}{\pi R_L}$, $I_{r,rms} = \dfrac{4V_m}{3\pi\sqrt{2}\sqrt{R_L^2 + 4\omega^2 L^2}}$

$$\therefore \gamma = \frac{\dfrac{4V_m}{3\pi\sqrt{2}} \cdot \dfrac{1}{\sqrt{R_L^2 + 4\omega^2 L^2}}}{\dfrac{2V_m}{\pi R_L}} \qquad \therefore \gamma = \frac{2}{3\sqrt{2}} \cdot \frac{1}{\sqrt{1 + \left(\dfrac{4\omega^2 L^2}{R_L^2}\right)}}$$

If $\dfrac{4\omega^2 L^2}{R_L^2} >> 1$, then $\gamma = \dfrac{1}{3\sqrt{2}} \cdot \dfrac{R_L}{\omega_L} = 0.236\dfrac{R_L}{\omega_L}$.

$$\therefore \gamma = \frac{R}{3\sqrt{2}\omega_L} \cdots\cdots\cdots\cdots \text{(6)}$$

The expression shows that ripple varies inversely as the magnitude of the inductance, Also, the ripple is smaller for smaller values of R_L i.e., for high currents.

When $R_L \to \infty$ the value of γ is given by $\gamma = \dfrac{2}{3\sqrt{2}}$ = 0.471 (close to the value 0.482 of rectifier). Thus the inductor filter should be used when R_L is consistently small.

Problems:

9. A full-wave rectifier with a load resistance of 15kΩ uses an inductor filter of 15H. The peak value of the applied voltage is 250V and the frequency is 50 cycles/second. Calculate the dc load current, ripple factor and dc output voltage.

Solution: The rectified output voltage across load resistance R_L up to second harmonic is

$$V_O = \frac{2V_m}{\pi} - \frac{2V_m}{\pi}\cos\omega t$$

Therefore, DC component of output voltage is given by $V_{dc} = \frac{2V_m}{\pi}$

$$\therefore I_{dc} = \frac{V_{dc}}{R_L} = \frac{2V_m}{\pi R_L}$$

$$= \frac{2\times 250}{\pi \times 15\times 10^3} = 10.6 \times 10^{-3}\ \text{A} = 10.6\ \text{mA}$$

$V_{dc} = I_{dc} R_L = (2.12\text{x}10^{-3})\ (15\text{x}10^3) = 31.8$ V.

Peak value of ripple voltage = $\frac{4V_m}{3\pi}$

$$\therefore V_{ac} = \frac{1}{\sqrt{2}}\frac{4V_m}{3\pi}$$

Now $I_{ac} = \frac{\frac{1}{\sqrt{2}}\cdot\frac{4V_m}{3\pi}}{\sqrt{R_L^2 + (2\omega L)^2}} = \frac{2\sqrt{2}V_m}{3\pi\sqrt{R_L^2 + (2\omega L)^2}}$

$$= \frac{2\times 1.414\times 250}{3\times 3.14\sqrt{\left(15\times 10^3\right) + \left(4\times 3.14\times 50\times 15\right)^2}}$$

$= 4.24\text{x}10^{-3}$ A **= 4.24 mA**

So, ripple factor, $\gamma = \frac{I_{ac}}{I_{dc}} = \frac{4.24mA}{10.6mA}$ = **0.4**

10. A dc voltage of 380 volt with a peak ripple voltage not exceeding 7volt is required to supply a 500Ω load. Find out if only inductor is used for filtering purpose in full-wave rectifier circuit,

i) inductance required and
ii) input voltage required, if transformer ratio is 1:1.

Solution:

i) Given that peak ripple = 7V

Therefore, $7 = \sqrt{2}\ V_{rms} \Rightarrow V_{rms} = \frac{7}{\sqrt{2}} = 4.95$V

Now $\gamma = \frac{V_{rms}}{V_{dc}} = \frac{4.95}{380} = 0.013$

In case of inductor filter

$$\gamma = \frac{1}{3\sqrt{2}}\frac{R_L}{\omega_L} \Rightarrow L = \frac{1}{3\sqrt{2}}\frac{R_L}{\omega_\gamma}$$

$$\Rightarrow L = \frac{1}{1335} \times \frac{R_L}{\omega_\gamma} \qquad (\therefore f=50Hz)$$

$$\Rightarrow L = \frac{500}{1335 \times 0.013} = \textbf{28.8 Henry}$$

ii) $V_{dc} = \frac{2V_m}{\pi} = 0.636V_m$

$$\therefore V_m = \frac{V_{dc}}{0.636} = \frac{380}{0.636} = \textbf{597.4 V}$$

This is maximum voltage on half secondary. So, the voltage across complete secondary = 2x 597.4 = **1195V**

∴ Input voltage = 1195V because turns ratio is 1:1.

Capacitor Filter:

Half-wave rectifier wit capacitor filter:

The half-wave rectifier with capacitor input filter is shown in figure below:

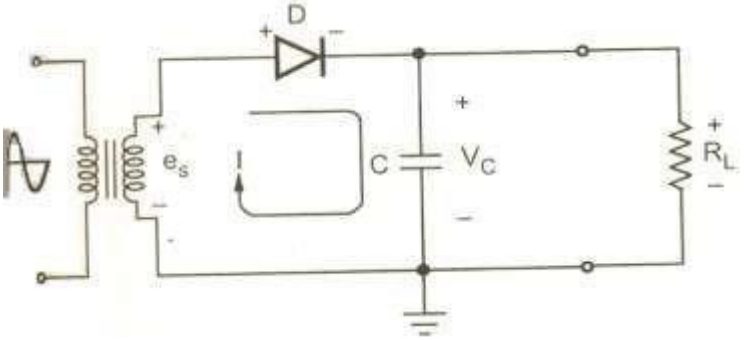


Fig. HWR with capacitor filter.

The filter uses a single capacitor connected in parallel with the load R_L. In order to minimize the ripple in the output, the capacitor C used in the filter circuit is quite large of the order of tens of microfarads.

The operation of the capacitor filter depends upon the fact that the capacitor stores energy during the conduction period and delivers this energy to the load during non-conduction period.

Operation:

During, the positive quarter cycle of the ac input signal, the diode D is forward biased and hence it conducts. This quickly charges the capacitor C to peak value of input voltage V_m. Practically the capacitor charge (V_m-Vγ) due to diode forward voltage drop.

When the input starts decreasing below its peak value, the capacitor remains charged at V_m and the ideal diode gets reverse biased. This is because the capacitor voltage which is cathode voltage of diode becomes more positive than anode.

Therefore, during the entire negative half cycle and some part of the next positive half cycle, capacitor discharges through R_L. The discharging of capacitor is decided by R_LC, time constant which is very large and hence the capacitor discharge very little from V_m.

In the next positive half cycle, when the input signal becomes more than the capacitor voltage, he diode becomes forward biased and charges the capacitor C back to V_m. The output waveform is shown in figure below:

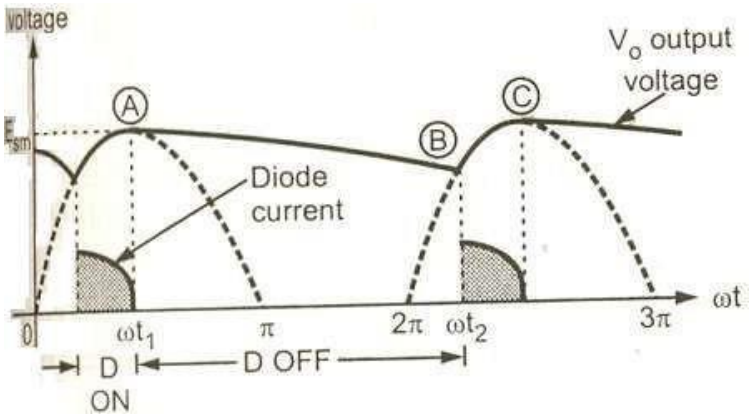
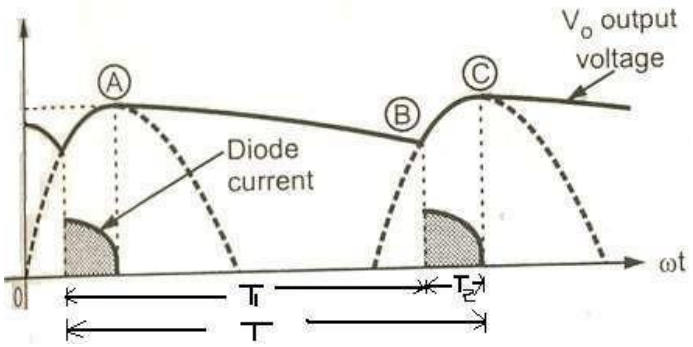


Fig. HWR output with capacitor filter.

The discharging if the capacitor is from A to B, the diode remains non-conducting. The diode conducts only from B to C and the capacitor charges.

Expression for Ripple factor:



Let, T = time period of the ac input voltage

T_1 = time for which the diode is non conducting.

T_2 = time for which diode is conducting.

Let V_r be the peak to peak value of the ripple voltage which is assumed to be triangular waveform. It is known mathematically that the rms value of such a triangular waveform is

$$V'_{rms} = \frac{V_r}{2\sqrt{3}}$$

During the time interval T_1, the capacitor C is discharging through the load resistance R_L. Therefore the charge lost is **$Q = C V_r$**

But, $i = \frac{dQ}{dt}$ $\quad\quad$ $\therefore Q = \int_0^{T_1} i\,dt = I_{dc} . T_1$

As integration gives average (or) dc value,

Hence $I_{dc} . T_1 = C . V_r$

$$\therefore V_r = \frac{I_{dc} T_1}{C}$$

But $T_1 + T_2 = T$ $\quad\quad$ Normally, $T_1 >> T_2$,

$$\therefore T_1 + T_2 \approx T_1 \Rightarrow T_1 = T$$

$$\therefore V_r = \frac{I_{dc} \cdot T}{C} = \frac{I_{dc}}{f \cdot C} \qquad \left(\therefore T = \frac{1}{f}\right)$$

But $Idc = \frac{V_{dc}}{R_L}$, $\left[V_{dc} = V_m - \frac{V_r}{2}, = V_m - \frac{I_{dc}}{2fc}\right]$

$$\therefore V_r = \frac{V_{dc}}{fCR_L}$$

Ripple factor, $\gamma = \frac{V'_{rms}}{V_{dc}} \qquad \Rightarrow \gamma = \frac{V_r}{2\sqrt{3} \cdot V_{dc}} = \frac{V_{dc}}{2\sqrt{3} fCR_L \cdot V_{dc}}$

$$\gamma \Rightarrow \frac{1}{2\sqrt{3} fCR_L}$$

The product of CR_L is the time constant of the filter circuit.

Surge current in Half-wave rectifier using capacitor filter:

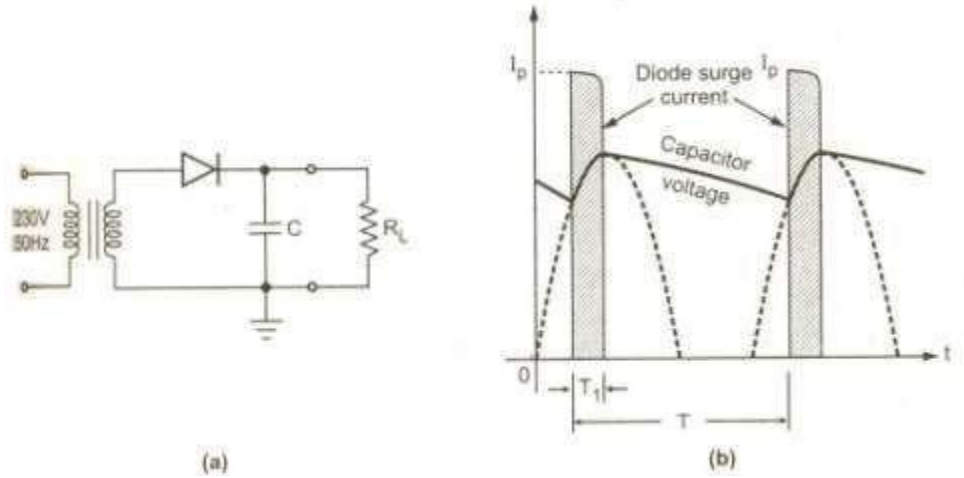


Fig. Surge current in HWR using capacitor filter

In half-wave rectifier, the diode is forward biased only for short period of time and conducts only during this time interval to charge the filter capacitance. The instant at which the diode gets forward biased, the capacitor instantaneously acts as short circuit and a surge current flow through a diode.

When the diode is non-conducting, the capacitor discharges through load resistance R_L. Thus total amount of charge that flows through conducting diode (or) diodes to recharge the capacitor must be equal to the amount of charge lost during the period when the diode (or) diodes are non-conducting and capacitor is discharging through load resistance R_L.

It can be seen that conduction period T_1 is very small compared to time period T, for the diode. Let, I_{dc} = average dc current

$I_{p(surge)}$ = peak value of the surge current.

Assume the current pulse to be rectangular assuming peak surge current flows for the entire conduction period of diode which is T_1.

Then Q (discharge) = Q (charge)

$$\therefore I_{dc} T = I_{P(surge)} T_1 \qquad \therefore I_{P(surge)} = I_{dc}\left(\frac{T}{T_1}\right)$$

As $T_1 << T$, it can be observed that $I_{p(surge)}$ can be many times larger than the average dc current supplied to the load.

Problem from previous External examinations:

10. A HWR circuit has filter capacitor of 1200μF and is connected to a load of 400Ω. The rectifier is connected to a 50Hz, 120V rms source. It takes 2msec for the capacitor to recharge during each cycle. Calculate the minimum value of the repetitive surge current for which the diode should be rated.

Solution:

Given C=1200μF, R_L=400Ω, f=50Hz, V_{rms}=120V

Conduction period of the diode, T_1=1ms

$$V_{sm} = \sqrt{2} \times V_{S(rms)} = = \sqrt{2} \times 120 \text{ V}$$

$$V_{dc} = V_{sm} - \frac{I_{dc}}{2fC}$$

$$\Rightarrow V_{dc} = V_{sm} - \frac{V_{dc}}{2fCR_L}$$

$$\Rightarrow V_{dc} = \frac{V_{sm}}{1 + \frac{1}{2fCR_L}}$$

$$= \frac{120\sqrt{2}}{1 + \frac{1}{2 \times 50 \times 1200 \times 10^{-6} \times 400}} = 3.46 \text{ V}$$

$$\therefore I_{dc} = \frac{V_{dc}}{R_L} = \frac{3.46}{400} = 8.658\text{mA}$$

Now $I_{dc}T = I_{p(surge)}T_1$

$$I_{P(surge)} = I_{dc}\left(\frac{T}{T_1}\right) = 8.658\text{mA} \times \frac{1}{50 \times 10^{-3}}$$

$$\therefore I_{P(surge)} = 0.17316 \text{ A}$$

Full-wave rectifier with capacitor filter:

The full-wave rectifier with capacitor filter is shown in the figure below:

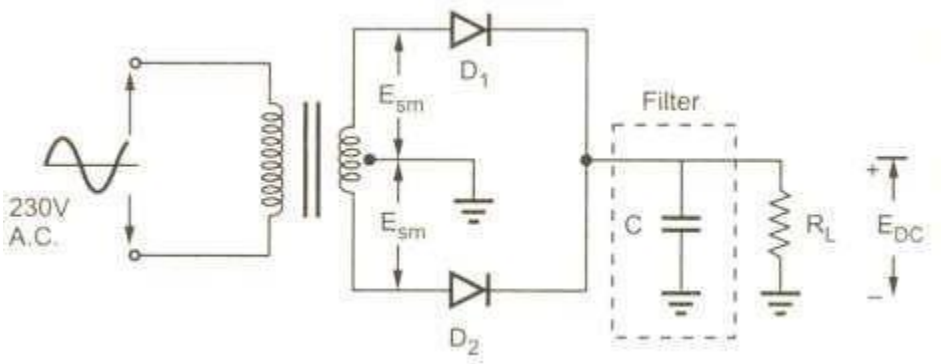


Fig. Full-wave rectifier with capacitor filter

Operation:

During the positive quarter cycle of the ac input signal, the diode D_1 is forward biased, the capacitor C gets charges through forward bias diode D_1 to the peak value of input voltage V_m.

In the next quarter cycle from $\frac{\pi}{2}$ to π the capacitor starts discharging through R_L, because once the capacitor gets charges to V_m, the diode D_1 gets reverse biased and stops conducting, so during the period from $\frac{\pi}{2}$ to π the capacitor C supplies the load current.

In the next quarter half cycle, that is, π to $\frac{3\pi}{2}$ of the rectified output voltage, if the input voltage exceeds the capacitor voltage, making D_2 forward biased, this charges the capacitor back to V_m.

In the next quarter half cycle, that is, from $\frac{3\pi}{2}$ to 2π , the diode gets reverse biased and the capacitor supplies the load current.

In FWR, as the time required by the capacitor to charge is very small and it discharges very little due to large time constant, hence ripple in the output gets reduced considerably. The output waveform is shown in figure below:

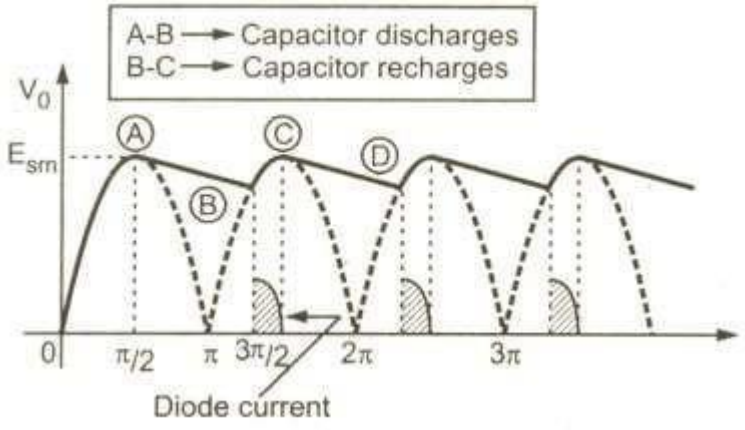
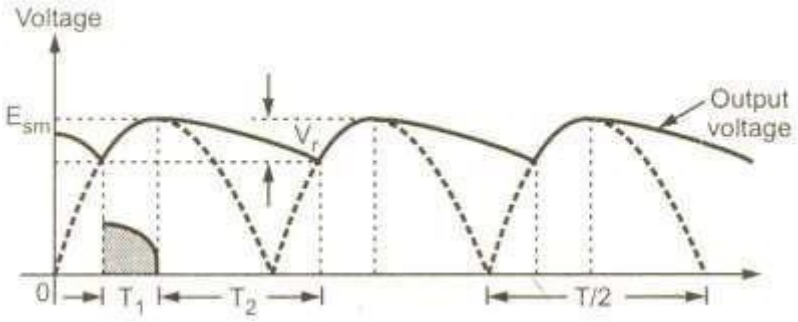


Fig. FWR output with capacitor filter.

Expression for Ripple factor:



Let, T = time period of the ac input voltage

$\frac{T}{2}$ = half of the time period

T_1 = time for which diode is conducting

T_2 = time for which diode is non-conducting

During time T_1, capacitor gets charged and this process is quick. During time T_2, capacitor gets discharged through R_L. As time constant R_LC is very large, discharging process is very slow and hence $T_2 >> T_1$.

Let V_r be the peak to peak value of ripple voltage, which is assumed to be triangular as shown in the figure below:

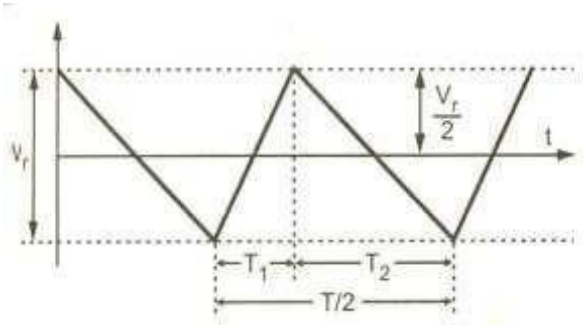


Fig. Triangular approximation of ripple

It is known mathematically that the rms value of such a triangular waveform is,

$$V_{rms} = \frac{V_r}{2\sqrt{3}}$$

During the time interval T_2, the capacitor C is discharging through the load resistance R_L. The charge lost is, $Q = CV_r$ But $i = \frac{dQ}{dt}$

$$\therefore Q = \int_0^{T_2} i\,dt = I_{DC}T_2$$

As integration gives average (or) dc value, hence $I_{dc} \cdot T_2 = C \cdot V_r$

$$\therefore V_r = \frac{I_{dc} T_2}{C} \qquad \text{But} \quad T_1 + T_2 = \frac{T}{2}$$

Normally, $T_2 >> T_1$,

$$\therefore T_1 + T_2 \approx T_1 = \frac{T}{2} \quad \text{where } T = \frac{1}{f}$$

$$\therefore V_r = \frac{I_{DC}\left(\frac{T}{2}\right)}{C} = \frac{I_{DC} \times T}{2C} = \frac{I_{DC}}{2fC}$$

But $I_{DC} = \frac{V_{DC}}{R_L}$, $\therefore V_r = \frac{V_{DC}}{2fCR_L}$ = peak to peak ripple voltage

Ripple factor, $= \frac{V_{rms}}{V_{dc}} = \frac{\frac{V_{dc}}{2fCR_L}}{2\sqrt{3}} \times \frac{1}{V_{dc}}$ $\left(\therefore V_{rms} = \frac{V_r}{2\sqrt{3}}\right)$

$$\therefore \text{Ripple factor} = \frac{1}{4\sqrt{3}fCR_L}$$

L-Section Filter (or) LC Filter:

The series inductor filter and shunt capacitor filter are not much efficient to provide low ripple at all loads. The capacitor filter has low ripple at heavy loads while inductor filter at small loads. A combination of these two filters may be selected to make the ripple independent of load resistance. The resulting filter is called L-Section filter (or) LC filter (or) Choke input filter. This name is due to the fact that the inductor and capacitor are connected as an inverted L. A full-wave rectifier with choke input filter is shown in figure below:

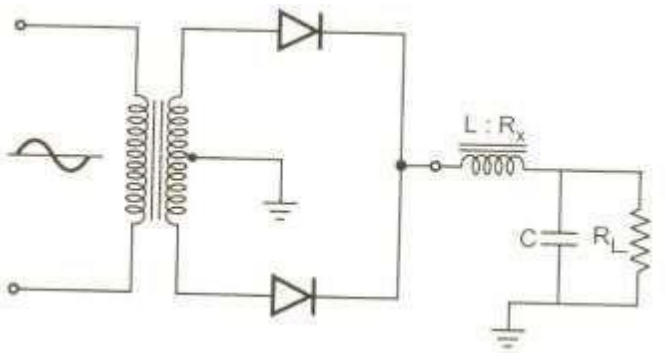


Fig. Full-wave rectifier with choke input filter.

The action of choke input filter is like a low pass filter. The capacitor shunting the load bypasses the harmonic currents because it offers very low reactance to a.c. ripple current while it appears as an open circuit to dc current.

On the other hand the inductor offers high impedance to the harmonic terms. In this way, most of the ripple voltage is eliminated from the load voltage.

Regulation:

The output voltage of the rectifier is given by, $\upsilon = \frac{2V_m}{\pi} - \frac{4V_m}{3\pi}\cos 2\omega t$

The dc voltage at no load condition is $V_{dc} = \frac{2V_m}{\pi}$

The dc voltage on load is $V_{dc} = \frac{2V_m}{\pi} - I_{dc} R$

Where $R = R_f + R_C + R_S$

R_f, R_C, R_S are resistances of diode, choke an secondary winding.

Ripple Factor:

The main aim of the filter is to suppress the harmonic components. So the reactance of the choke must be large as compared with the combined parallel impedance of capacitor and resistor.

The parallel impedance of capacitor and resistor can be made small by making the reactance of the capacitor much smaller than the resistance of the load. Now the ripple current which has passed through L will not develop much ripple voltage across R_L because the reactance of C at the ripple frequency is very small as compared with R_L.

Thus for LC filter, $X_L >> X_C$ at $2\omega = 4\Pi f$ and $R_L >> X_C$

Under these conditions, the a.c. current through L is determined primarily by $X_L = 2\omega L$ (the reactance of the inductor at second harmonic frequency). The rms value of the ripple current is

$$I_{r(rms)} = \frac{4V_m}{3\pi\sqrt{2}} \cdot \frac{1}{X_L} = \frac{2}{3\sqrt{2}X_L}\left(\frac{2V_m}{\pi}\right) = \frac{\sqrt{2}}{3X_L}\left(V_{dc}\right)$$

Always it was stated that X_C is small as compared with R_L, but it is not zero. The a.c. voltage across the load (the ripple voltage) is the voltage across the capacitor.

Hence $$V_{r(rms)} = I_{r(rms)} \times X_C$$
$$= \left\{ \frac{\sqrt{2} V_{dc}}{3X_L} \right\} X_C$$

We know that ripple factor γ is given by

$$\gamma = \frac{V_{r(rms)}}{V_{dc}} = \frac{\sqrt{2} X_C}{3X_L}$$

But $X_C = \frac{1}{2\omega C}$ and $X_L = 2\omega L$

$$\therefore \gamma = \frac{\sqrt{2}}{3(2\omega L)} \times \frac{1}{2\omega C} = \frac{1}{6\sqrt{2}\omega^2 LC}$$

$$\therefore \gamma = \frac{1}{6\sqrt{2}\omega^2 LC}$$

This shows that ω is independent of R_L.

The necessity of Bleeder Resistance R_B:

The basic requirement of this filter circuit is that the current through the choke must be continuous and not interrupted. An interrupted current through the choke may develop a large back e.m.f which may be in excess of PIV rating of the diodes and/or maximum voltage rating of the capacitor C. Thus this back e.m.f is harmful to the diodes and capacitor. To eliminate the back e.m.f. developed across the choke, the current through it must be maintained continuous. This is assured by connecting a bleeder resistance, R_B across the output terminals.

The full-wave rectifier with LC filter and bleeder resistance is shown in the figure below:

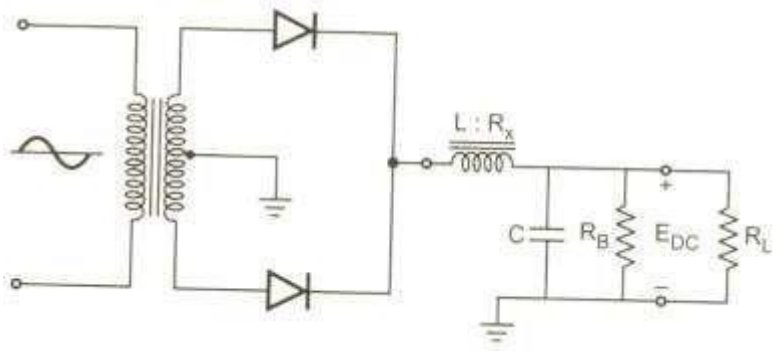
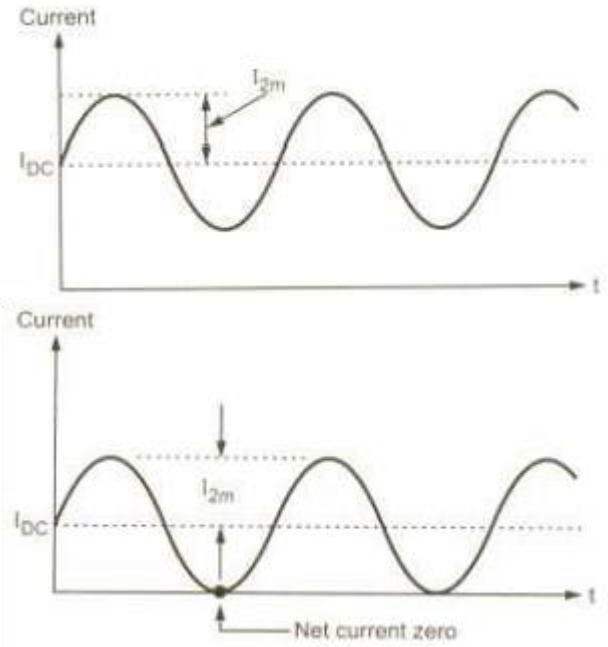


Fig. filter with Bleeder resistance

We know, $I_{DC} = \frac{2}{\pi} \frac{V_{sm}}{R_C + R}$ where R_C is choke terminal resistance , R is $R_B \| R_L$

$$I_{2m} = \frac{4}{3\pi} \frac{V_{sm}}{2\omega L}$$



Thus I_{DC} is seen to depend on load resistance $\lfloor R = R \;||\; R \rfloor$ while I_{2m} does not. I_{2m} is constant, independent of R_L. The second harmonic terminal I_{2m} is superimposed on I_{DC}, as shown in figure. If the load resistance is increased, I_{DC} will decrease, but I_{2m} will not.

If the load resistance is still further increased, a stage may come where I_{DC} may become less than I_{2m}. In such situation, for a certain period of time in each cycle, the net current in the circuit will be zero. In other words, the current will be interrupted and not continuous. This interruption of current, producing large back emf is harmful to both the diodes and filter capacitor C. To avoid such situation, certain minimum load current has to be drawn. For this purpose, the bleeder resistance R_B is so selected that it draws, a minimum current through choke.

The condition is $I_{DC} \geq I_{2m}$

$$I_{DC} = \frac{2}{\pi}\frac{V_{sm}}{R_C + R} \geq I_{2m} = \frac{4}{3\pi}\frac{V_{sm}}{2\omega L}$$

$\Rightarrow R_C + R \geq 3\omega L$ Usually $R_C << R$, then $R \geq 3\omega L$

Since R = $R_B || R_L$, considering the worst case that the load resistance R_L is not connected, then $R=R_B$ $\therefore R_B \geq 3\omega L$

$\therefore R_B \geq 6\pi fL \qquad (\because \omega = 2\pi f)$

If f=50Hz then $R_B \geq 943L$ Practically, R_B is selected to be equal to 900L.

Critical Inductance:

We have assumed that the current flows through the circuit all the times. For this, the value of inductance L must be kept above certain minimum value which is called *critical Inductance.* This value of inductance depends on load resistance R_L and supply frequency ω.

The required value of critical inductance for 50Hz supply frequency is $L_C \geq \frac{R_L}{943}$

Problem from previous External examination:

12. A full-wave rectifier supplies a load requiring 300V at 200mA. Calculate the transformer secondary voltage for
i) a capacitor input filter using a capacitor of 10μF.
ii) a choke input filter using a choke of 10H and a capacitance of 10μF.
Neglect the resistance of choke.

Multiple L-Section filters:

The number of L-sections i.e., LC circuits can be connected one after another to obtain multiple L-section filter. It gives excellent filtering and smooth dc output voltage. The figure below shows multiple L-section filter.

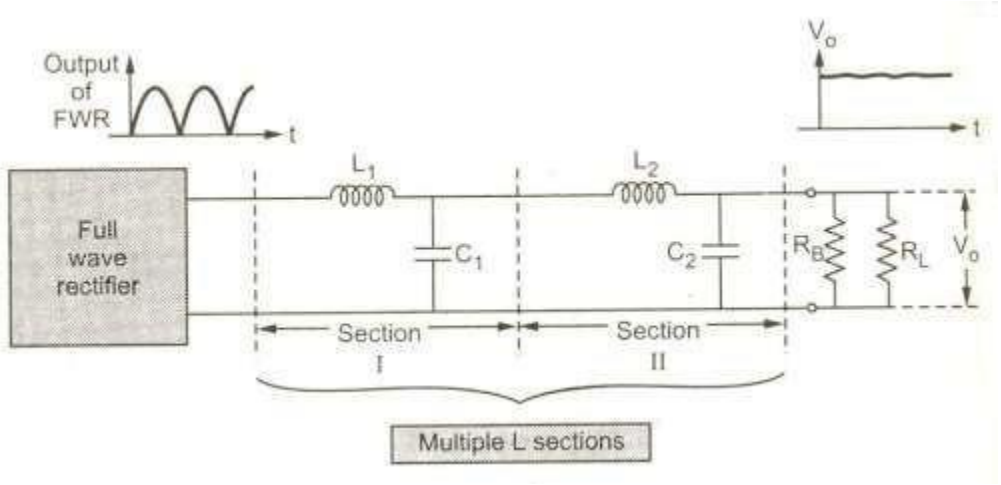


Fig. Multiple L-sections.

For two section LC filter, the ripple factor is given by $\Rightarrow \gamma = \frac{\sqrt{2}}{3} \cdot \frac{X_{C1}}{X_{L1}} \cdot \frac{X_{C2}}{X_{L2}}$

CLC Filter (or) Π – section Filter:

This is capacitor input filter followed by a L-section filter. The ripple rejection capability of a Π-section filter is very good. The full-wave rectifier with Π-section filter is shown in the figure.

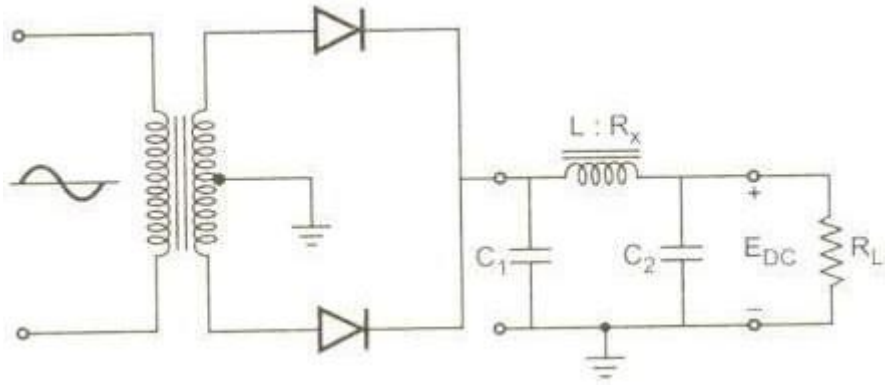


Fig. Π-section Filter.

It consists of an inductance L with a dc winding resistance as R_C and two capacitors C_1 and C_2. The filter circuit is fed from fill wave rectifier. Generally two capacitors are selected equal.

The rectifier output is given to the capacitor c_1. This capacitor offers very low reactance to the ac component but blocks dc component. Hence capacitor C_1 bypasses most of the ac component. The dc component then reaches to the choke L. The choke L offers very high reactance to dc. So it blocks ac component and does not allow it to reach to load while it allows dc component to pass through it. The capacitor C_2 now allows to pass remaining ac component and almost pure dc component reaches to the load. The circuit looks like a Π, hence called Π-Filter.

Ripple Factor:

The Fourier analysis of a triangular wave is given by

$$\upsilon = V_{dc} - \frac{V_r}{\pi}\left(\sin\omega t - \frac{\sin 4\omega t}{2} + \frac{\sin 6\omega t....}{3}\right) \quad \text{.....(1)}$$

In case of full wave rectifier with capacitor filter, we have proved that

$$V_\gamma = \frac{I_{dc}}{2fC} = \frac{I_{dc}}{2fC_1} \qquad \left(\therefore C = C_1 here\right) \quad \text{.....(2)}$$

The rms second harmonic voltage is

$$V_{r(rms)} = \frac{V_r}{\sqrt{2}} \quad \text{.....(3)}$$

Substituting the value of V_r from equation (2) in equation (3), we get

$$V_{r(rms)} = \frac{I_{dc}}{2\pi fC_1\sqrt{2}} = \sqrt{2}I_{dc}.XC_1 \quad \text{.....(4)}$$

Where $XC_1 = \frac{1}{2\omega C_1} = \frac{1}{4\pi fC_1}$ = reactance of C_1 at second harmonic frequency.

The voltage $V_{r(rms)}$ is impressed on L-section.

Now, the ripple voltage

age V"

$_{r(rms)}$ can be obtained by multiplying $V_{r(rms)}$ by $\frac{XC_2}{X_L}$ i.e.,

$$\left(V_r'\right)_{rms} = (V_r)_{rms} \times \frac{XC_1}{X_L}$$

(or) $$\left(V_r'\right)_{rms} = \sqrt{2} I_{dc} XC_1 . \frac{XC_2}{X_L} \quad \text{.....(5)}$$

$$\therefore \gamma = \frac{\left(V_r'\right)_{rms}}{V_{dc}} = \frac{\sqrt{2} I_{dc} XC_1 . \frac{XC_2}{X_L}}{V_{dc}}$$

$$\Rightarrow \gamma = \frac{\sqrt{2}.XC_1.XC_2}{R_L.X_L} \qquad \left(\because \frac{I_{dc}}{V_{dc}} = \frac{1}{R_L}\right)$$

$$\therefore \gamma = \frac{\sqrt{2}.XC_1.XC_2}{R_L.X_L}$$

Here all reactances are calculated at second harmonic frequency. Substituting the values, we get $$\gamma = \frac{\sqrt{2}}{8\omega^3 C_1 C_2 L R_L}$$

At f= 50Hz, $$\gamma = \frac{5700}{LC_1 C_2 R_L}$$

Where C_1 and C_2 are in μF, L in henrys and R_L in ohms.

Multiple Π-Section Filter:

To obtain almost pure dc to the load, more Π-sections may be used one after another. Such a filter using more than one Π-section is called multiple Π-section filter. The figure shows multiple Π-section filters.

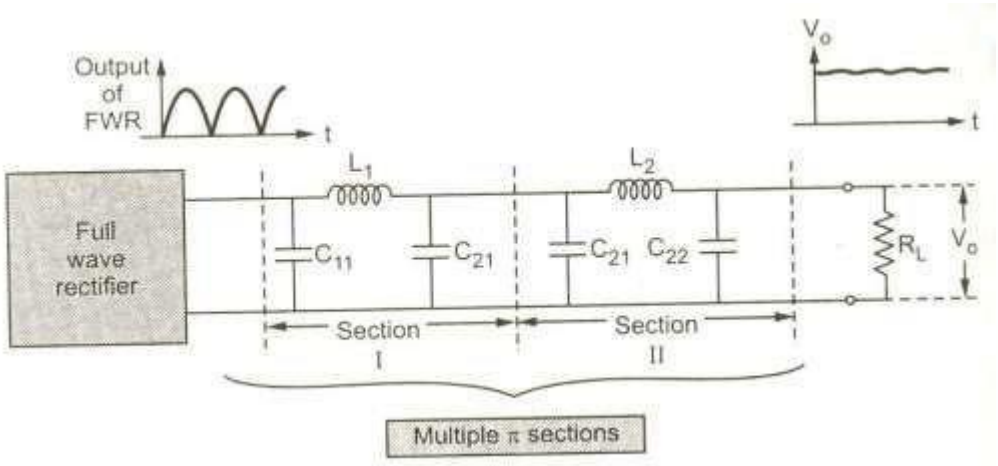


Fig. Multiple Π-section Filter.

The ripple factor of two section Π-filter is given by $\gamma = \sqrt{2}.\frac{X_{C11}}{R_L}.\frac{X_{C12}}{X_1}.\frac{X_{C22}}{X_2}$

Problems:

14. Design a CLC (or) Π-section filter for V_{dc}=10V, I_L=200mA and γ=2%

Solution:

$$R_L = \frac{V_{dc}}{I_L} = \frac{10}{200\times10^{-3}} = 50\Omega$$

$$\gamma = \frac{5700}{LC_1C_2R_L} \qquad \Rightarrow 0.02 = \frac{5700}{LC_1C_2R_L} = \frac{114}{LC_1C_2}$$

If we assume L=10H and $C_1=C_2=C$, we have

$$\Rightarrow 0.02 = \frac{114}{LC^2} = \frac{11.4}{C^2}$$

$C^2 = 750 \Rightarrow \sqrt{570}$ = **24μF**

Voltage Regulators:

A voltage regulator is an electronic device which produces constant output voltage irrespective of variations in the input voltage and load variations.

A voltage regulator is an electronic circuit that produces a stable dc voltage independent of the load current, temperature and ac line voltage variations.

Factors determining the stability:

The output voltage V_O depends on the input unregulated dc voltage V_{in}, load current I_L and temperature T. Hence the change in output voltage of power supply can be expressed as follows:

$$\Delta V_O = \frac{\partial V_O}{\partial V_{in}}\Delta V_{in} + \frac{\partial V_O}{\partial I_L}\Delta I_L + \frac{\partial V_O}{\partial T}\Delta T$$

$$\Delta V_O = S_V \Delta V_{in} + R_O \Delta I_L + S_T \Delta T$$

Where the three coefficients are defined as

Input regulation factor, $$S_V = \left.\frac{\Delta V_O}{\Delta V_{in}}\right|_{\Delta V_{in}=0;\Delta T=0}$$

Output resistance, $$R_O = \left.\frac{\Delta V_O}{\Delta I_L}\right|_{\Delta V_{in}=0;\Delta T=0}$$

Temperature coefficient, $$S_T = \left.\frac{\Delta V_O}{\Delta T}\right|_{\Delta V_{in}=0;\Delta I_L=0}$$

Smaller the value of the three coefficients, better the regulation of power supply.

Load Regulation:

Load regulation is expressed as

$$\text{Load regulation} = \frac{V_{no-load} - V_{full-load}}{V_{no-load}}$$

(or)

$$\text{Load regulation} = \frac{V_{no-load} - V_{full-load}}{V_{full-load}}$$

Where $V_{no\text{-}load}$ is the output voltage at zero load current and $V_{full\text{-}load}$ is the output voltage at related load current. This is usually denoted in percentage.

Zener diode voltage regulator:

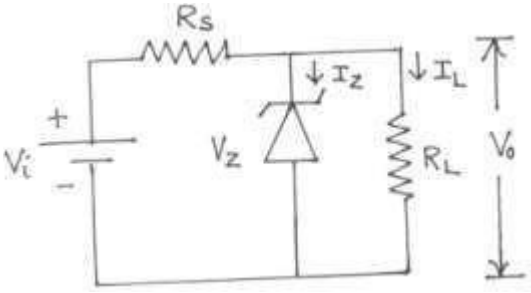


Fig. Zener Regulator.

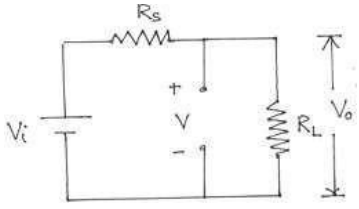
Zener voltage regulator is shown in figure above, in which a zener diode is connected in parallel to the load resistance R_L. The resistance R_S is a current limiting resistor.

V_i, R_S and R_L fixed:

The analysis can be carried out into two steps.

i) Determining the state of the zener diode by removing it from the network and calculating the voltage across the resulting open circuit.

$$V = V_o = \frac{R_L V_i}{R_S + R_L}$$



if $V \geq V_Z$ the zener diode is „ON“
if $V < V_Z$ the zener diode is „OFF“.

ii) Substitute the appropriate equivalent circuit and solve for the desired unknowns.

$$V_O = V_Z$$

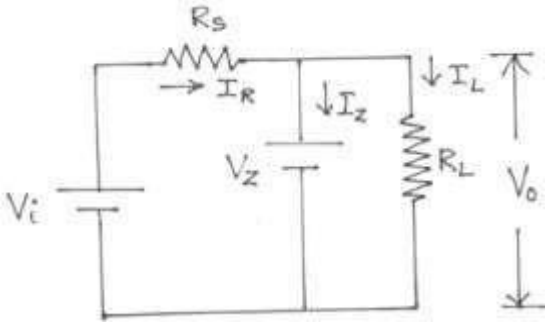
$$I_Z = I_R - I_L$$

$$I_L = \frac{V_Z}{R_L}$$

$$I_R = \frac{V_R}{R_S}$$

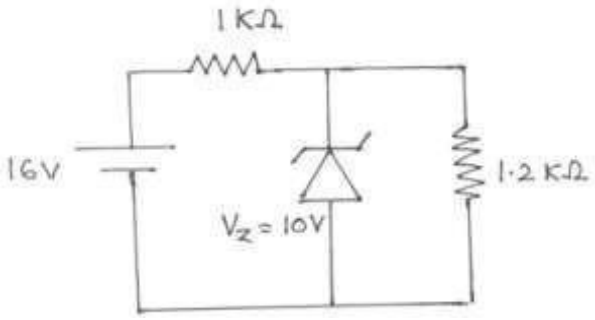
$$V_R = V_i - V_Z$$

$$P_Z = V_Z I_Z$$



Problem:

For the zener diode network of below figure determine V_O, V_R, V_Z and P_Z. Repate the same with R_L=3kΩ



Solution:

To find the diode status, replace the diode by open circuit and by finding the voltage across the open circuit.

$$V_o = \frac{16V \times 1.2k\Omega}{1+1.2k\Omega} \qquad V_o = \frac{16\times 1.2}{2.2} = 8.72 \text{ Volts}$$

$\therefore V_o < V_Z$, the zener diode is in „OFF" state $\qquad \therefore I_Z = 0$

$$I_L = \frac{V_L}{R_L} = \frac{8\ .}{1\ .k} = 7.27 \text{ mA}$$

$$I_R = \frac{V_R}{R} = \frac{V_i - V_o}{R} = \frac{16-7.27}{1k\Omega} = 8.72 \text{ mA}$$

With R_L = 3KΩ:

$$V_o = \frac{16\times 3}{4} = 12\text{Volts.}$$

$V_O > V_Z$ $\therefore$ The zener diode is „ON".

The equivalent circuit is replacing the zener by its equivalent voltage, to determine all the parameters are shown below.

$$V_L = \frac{16\times 3}{4} = 12 \text{ Volts}$$

Zener is ON

$$\therefore V_o = V_Z = 10V$$

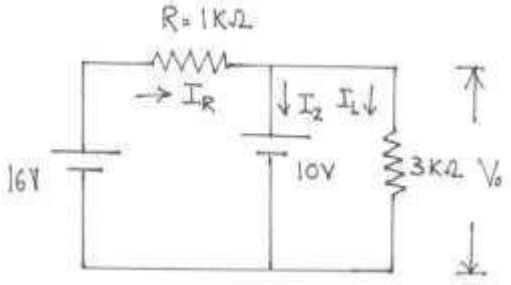
$$I_L = \frac{V_Z}{R_L} = \frac{10}{3k\Omega} = 3.33mA$$

$$I_R = \frac{V_R}{R} = \frac{V_i - V_Z}{R} = \frac{16-10}{1k\Omega} = \frac{6}{1k\Omega} = 6mA$$

$$I_R = I_Z + I_L$$

$$I_Z = I_R - I_L = 6\text{-}3.33 = 2.667 \text{ mA}$$

$$P_Z = V_Z . I_Z = 10\text{x}2.667 = 2.66 \text{ mW.}$$



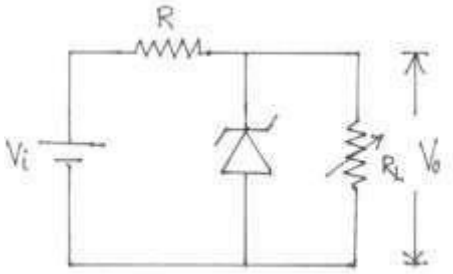
Fixed V_i, R and variable R_L:

$$V_o = V_Z = \frac{R_L V_i}{R_S + R}$$

Solving for R_L

$$R_{L\min} = \frac{R_i V_Z}{V_i - V_Z}$$

$$I_{L\max} = \frac{V_Z}{R_{L\min}}$$



Once the diode is in „ON" state

$$V_R = V_i - V_Z$$

$$I_R = \frac{V_R}{R}$$

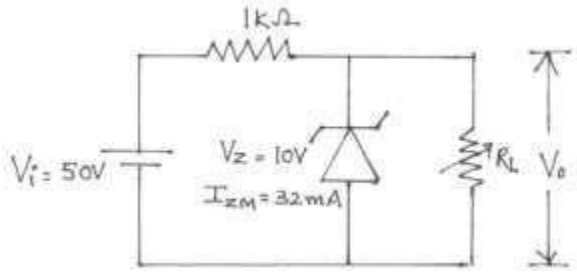
$$I_Z = I_R - I_L$$

$$I_{L\min} = I_R - I_{ZM}$$

$$R_{L\max} = \frac{V_Z}{I_{L\min}}$$

Problem:

For the network shown below, determine the range of R_L and I_L that will result in V_L being maintained at 10V.



Solution:

$$R_{L\min} = \frac{R.V_Z}{V_i - V_Z} = \frac{1k\Omega \times 10V}{50-10} = \frac{10k\Omega}{40} = 0.25k\Omega$$

$$I_{L\max} = \frac{V_Z}{R_{L\min}} = \frac{10}{0.25k} = 40mA$$

$$V_R = V_i - V_Z$$

$$V_R = 50 - 10 = 40$$

$$I_R = \frac{V_R}{R} = \frac{40}{1k\Omega} = 40mA$$

$$I_{L\min} = I_R - I_{ZM}$$

= 40-32 = 8mA

$$R_{L\max} = \frac{V_Z}{I_{L\min}} = \frac{10}{8mA} = 1.25k\Omega$$

Fixed R, R_L and variable V_i:

$$V_o = V_Z = \frac{R_L V_i}{R + R_L}$$

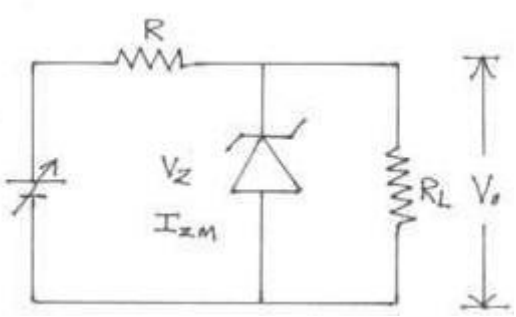
$$V_{i\min} = \frac{(R + R_L)V_Z}{R_L}$$

$$I_{R\max} = I_{ZM} + I_L$$

$$I_Z = \frac{V_Z}{R_L}$$

$$V_{i\max} = V_{R\max} + V_Z$$

$$V_{R\max} = (I_{R\max}.)R$$



Problem:

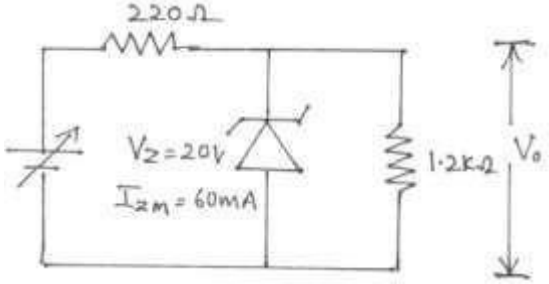
Determine the range of values of V_i, that will maintain the zener diode of figure below is in the „ON“ state.

Solution:

V_{imin} = 23.67V V_{imax} = 36.87V

$$V_{i\min} = \frac{(R + R_L)V_Z}{R_L}$$

$$= \frac{(220 + 1200)20}{1200} = 23.67V$$



$$V_{i\max} = V_{R\max} + V_Z$$

$$= \left(I_{R\max}\right)R + V_Z$$

$$= \left(I_{ZM} + I_L\right)R + V_Z$$

$$= \left(60mA + \frac{20}{1.2k}\right)(220) + 20$$

=36.87 Volts

Basic Voltage Regulator:

The basic voltage regulator in its simplest form consists of,

i) Voltage reference, V_R
ii) Error amplifier
iii) Feedback network
iv) Active series (or) shunt control element.

The voltage reference generally a voltage level which is applied to the comparator circuit, which is generally error amplifier. The second input to the error amplifier is obtained through feedback network. Generally using the potential divider, the feedback signal is derived by sampling the output voltage. The error amplifier converts the difference between the output sample and the reference voltage into an error signal. This error signal in turn controls the active element of the regulator circuit, in order to compensate the change in the output voltage. Such an active element is generally a transistor. Thus the output voltage of the regulator is maintained constant.

Types of voltage Regulators:

There are two types of voltage regulators available namely,

i) Shunt voltage regulator
ii) Series voltage regulator

Each type provides a constant dc output voltage which is regulated.

Shunt Voltage Regulator:

The heart of any voltage regulator circuit is a control element.

If such a control element is connected in shunt with the load, the regulator circuit is called shunt voltage regulator.

The figure shows the block diagram of shunt voltage regulator circuit.

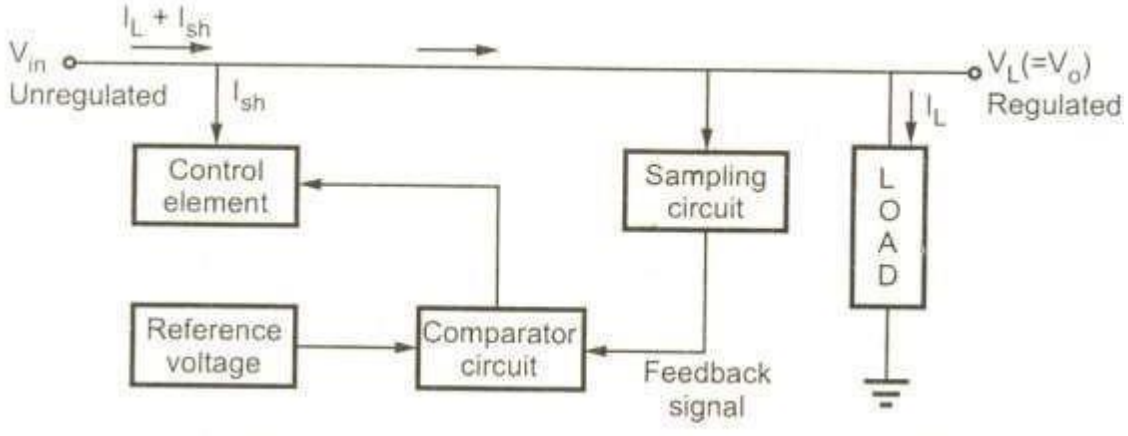


Fig. Block diagram of shunt voltage regulator.

The unregulated input voltage V_{in}, tries to provide the load current. But part of the current is taken by the control element, to maintain the constant voltage across the load.

If there is any change in the load voltage, the sampling circuit provides a feedback signal to the comparator circuit.

The comparator circuit compares the feedback signal with the reference voltage and generates a control signal which decides the amount of current required to be shunted to keep the load voltage constant.

For example, if load voltage increases then comparator circuit decides the control signal based on the feedback information, which draws increased shunt current I_{sh} value.

Due to this, the load current I_L deceases and hence the load voltage decreases to its normal.

Thus control element maintains the constant output voltage by shunting the current; hence the regulator circuit is called voltage shunt regulator circuit.

Series Voltage Regulator:

If in a voltage regulator circuit, the control element is connected in series with the load, the circuit is called series voltage regulator circuit.

Figure shows the block diagram of series voltage regulator circuit.

The unregulated dc voltage is the input to the circuit.

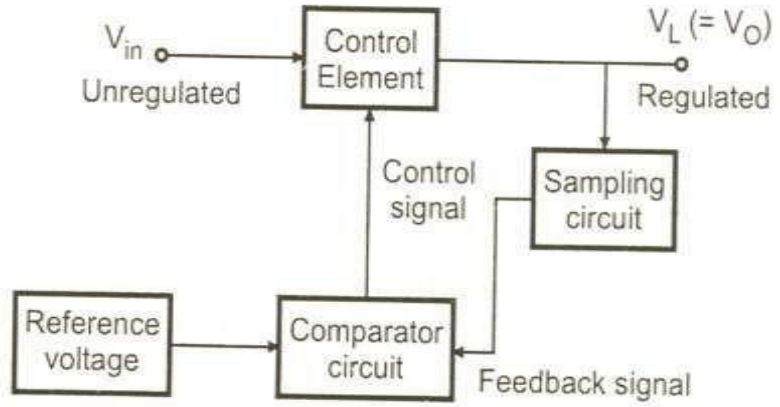


Fig. Block diagram of series voltage regulator.

The control element controls the amount of the input voltage that gets to the output. The sampling circuit provides the necessary feedback signal. The comparator circuit compares the feedback with the reference voltage to generate the appropriate control signal.

For example, if the load voltage tries to increase, the comparator generates a control signal based on the feedback information. This control signal causes the control element to decrease the amount of the output voltage. Thus the output voltage is maintained constant.

Thus, the control element which regulates the load voltage, based on the control signal is in series with the load and hence the circuit is called series voltage regulator circuit.

Comparison of Shunt and Series voltage regulators:

Sl. No.	Shunt Regulator	Series Regulator
1.	The control element is in parallel with the load.	The control element is in series with the load.
2.	Only small current passes through the control element which is required to be diverted to keep output constant	The entire load current I_L always passes through the control element.
3.	Any change in output voltage is compensated by changing the current I_{sh} through the control element as per the control signal.	Any change in output voltage is compensated by adjusting the voltage across the control element as per the control signal.
4.	The control element is low current, high voltage rating component.	The control element is high current, low voltage rating component.
5.	The regulation is poor.	The regulation is good.
6.	Efficiency depends on the load current.	Efficiency depends on the output voltage.
7.	Not suitable for varying load conditions. Preferred for fixed voltage applications.	Preferred for fixed as well as variable.
8.	Simple to design.	Complicated to design as compared to shunt regulators.
9.	Examples: Zener Shunt regulators, transistorized shunt regulator etc.,	Examples: Series feedback type regulator, series regulator with pre-regulator and feedback limiting etc.,

UNIT-III

Bipolar Junction Transistor

Introduction :

The transistor was invented in 1947 by John Bardeen, Walter Brattain and William Shockley at Bell Laboratory in America.

A transistor is a semiconductor device, commonly used as an Amplifier or an electrically Controlled Switch.

There are two types of transistors:

1) Unipolar Junction Transistor
2) Bipolar Junction Transistor

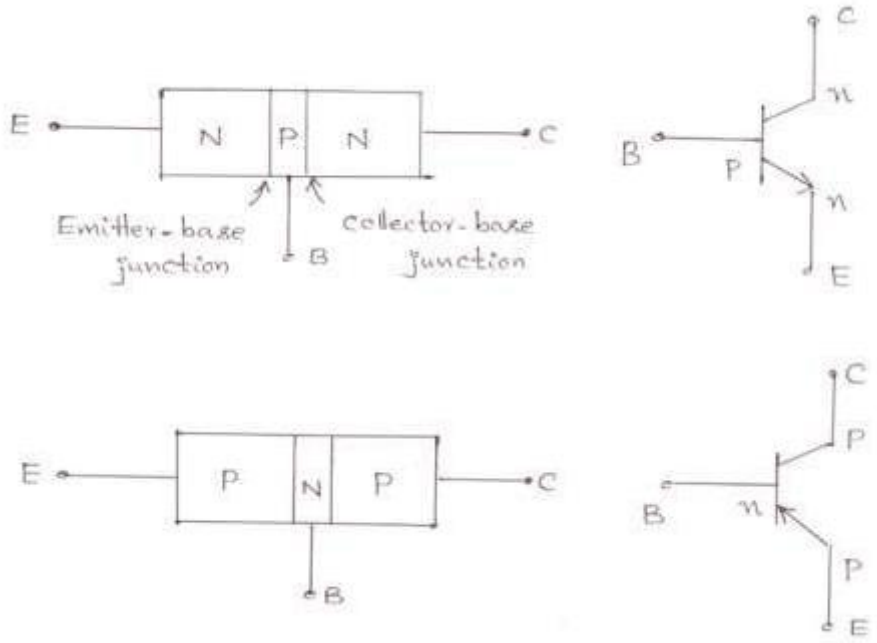
In Unipolar transistor, the current conduction is only due to one type of carriers i.e., majority charge carriers. The current conduction in bipolar transistor is because of both the types of charge carriers i.e., holes and electrons. Hence it is called as Bipolar Junction Transistor and it is referred to as BJT.

BJT is a semiconductor device in which one type of semiconductor material is sand witched between two opposite types of semiconductor i.e., an n-type semiconductor is sandwiched between two p-type semiconductors or a p-type semiconductor is sandwiched between two n-type semiconductor. Hence the BJTs are of two types.

They are:

1) n-p-n Transistor
2) p-n-p Transistor

The two types of BJTs are shown in the figure below.



The arrow head represents the conventional current direction from p to n.

Transistor has three terminals.

1) Emitter
2) Base
3) Collector

Transistor has two p-n junctions. They are:

1) Emitter-Base Junction 2)Collector-Base Junction

Emitter: Emitter is heavily doped because it is to emit the charge carriers.

Base: The charge carriers emitted by the emitter should reach collector passing through the base. Hence base should be very thin and to avoid recombination, and to provide more collector current base is lightly doped.

Collector: Collector has to collect the most of charge carriers emitted by the emitter. Hence the area of cross section of collector is more compared to emitter and it is moderately doped.

Transistor can be operated in three regions.

1) Active region.
2) Saturation region.
3) Cut-Off region.

Active Region: For the transistor to operate in active region base to emitter junction is forward biased and collector to base junction is reverse biased.

Saturation Region: Transistor to be operated in saturation region if both the junctions i.e., collector to base junction and base to emitter junction are forward biased.

Cut-Off Region: For the transistor to operate in cut-off region both the junctions i.e., base to emitter junction and collector to base junction are reverse biased.

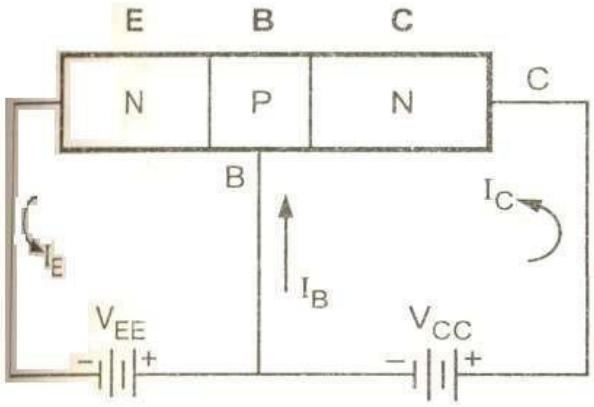
Transistor can be used as

1) Amplifier 2) Switch

For the transistor to act as an amplifier, it should be operated in active region. For the transistor to act as a switch, it should be operated in saturation region for ON state, and cut-off region for OFF state.

Transistor Operation:

Working of a n-p-n transistor:



The n-p-n transistor with base to emitter junction forward biased and collector base junction reverse biased is as shown in figure.

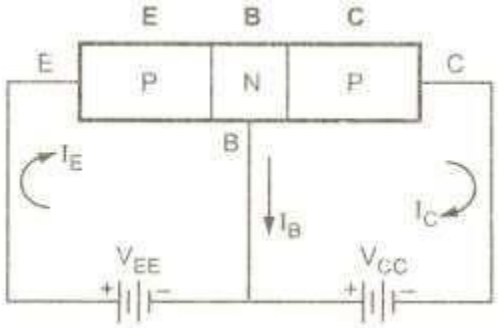
As the base to emitter junction is forward biased the majority carriers emitted by the n-type emitter i.e., electrons have a tendency to flow towards the base which constitutes the emitter current I_E.

As the base is p-type there is chance of recombination of electrons emitted by the emitter with the holes in the p-type base. But as the base is very thin and lightly doped only few electrons emitted by the n-type emitter less than 5% combines with the holes in the p-type base, the remaining more than 95% electrons emitted by the n-type emitter cross over into the collector region constitute the collector current.

The current distributions are as shown in fig

$$\mathbf{I_E = I_B + I_C}$$

Working of a p-n-p transistor:



The p-n-p transistor with base to emitter junction is forward biased and collector to base junction reverse biased is as show in figure.

As the base to emitter junction is forward biased the majority carriers emitted by the p-type emitter i.e., holes have a tendency to flow towards the base which constitutes the emitter current I_E.

As the base is n-type there is a chance of recombination of holes emitted by the emitter with the electrons in the n-type base. But as the base us very thin and lightly doped only few electrons less than 5% combine with the holes emitted by the p-type emitter, the remaining 95% charge carriers cross over into the collector region to constitute the collector current.

The current distributions are shown in figure.

$$\mathbf{I_E = I_B + I_C}$$

Current components in a transistor:

The figure below shows the various current components which flow across the forward-biased emitter junction and reverse-biased collector junction in P-N-P transistor.

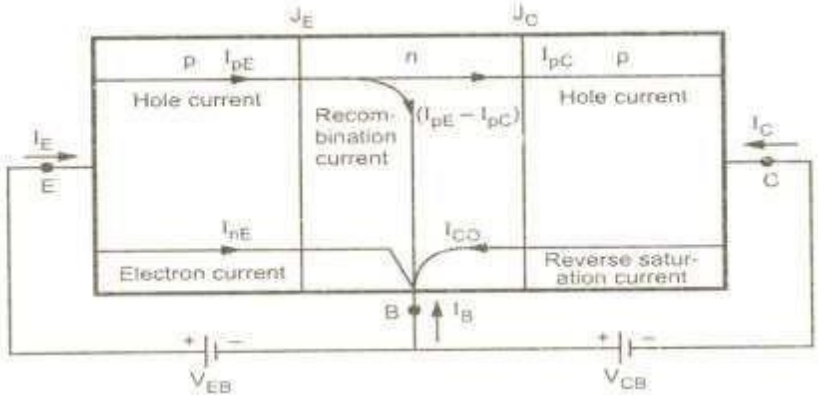


Figure. Current components in a transistor with forward-biased emitter and reverse-biased collector junctions.

The emitter current consists of the following two parts:

1) Hole current I_{pE} constituted by holes (holes crossing from emitter into base).

2) Electron current I_{nE} constituted by electrons (electrons crossing from base into the emitter).

Therefore, Total emitter current $I_E = I_{pE}$ (majority)+ I_{nE} (Minority)

The holes crossing the emitter base junction J_E and reaching the collector base junction J_C constitutes collector current I_{pC}.

Not all the holes crossing the emitter base junction J_E reach collector base junction J_C because some of them combine with the electrons in the n-type base.

Since base width is very small, most of the holes cross the collector base junction J_C and very few recombine, constituting the base current ($I_{pE} - I_{pC}$).

When the emitter is open-circuited, $I_E=0$, and hence $I_{pC}=0$. Under this condition, the base and collector together current I_C equals the reverse saturation current I_{CO}, which consists of the following two parts: I_{PCO} caused by holes moving across I_C from N-region to P-region.

I_{nCO} caused by electrons moving across I_C from P-region to N-region. $I_{CO} = I_{nCO} + I_{pCO}$

In general, $I_C = I_{nC} + I_{pC}$

Thus for a P-N-P transistor, $\mathbf{I_E = I_B + I_C}$

Transistor circuit configurations:

Following are the three types of transistor circuit configurations:

1) Common-Base (CB)
2) Common-Emitter (CE)
3) Common-Collector (CC)

Here the term „Common" is used to denote the transistor lead which is common to the input and output circuits. The common terminal is generally grounded.

It should be remembered that regardless the circuit configuration, the emitter is always forward-biased while the collector is always reverse-biased.

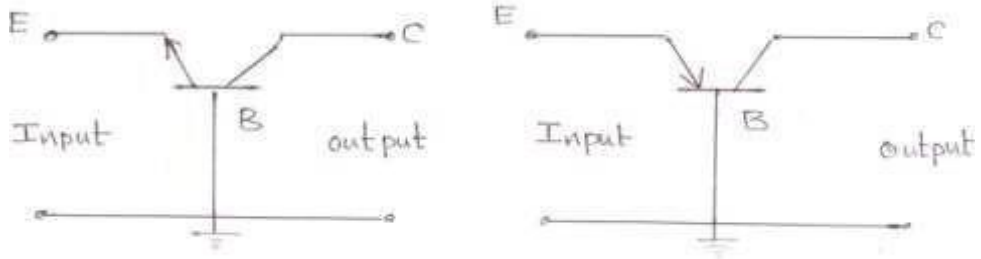


Fig. Common – Base configuration

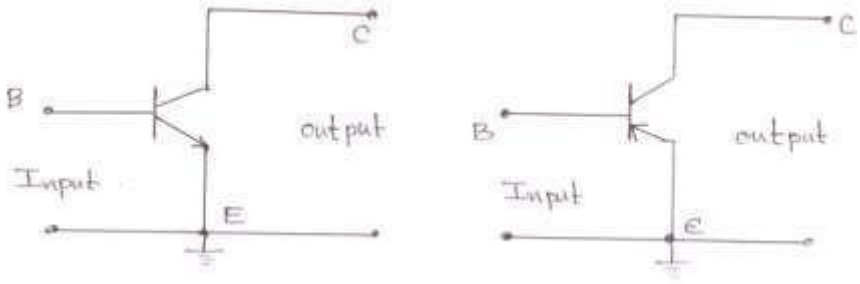


Fig. Common – emitter configuration

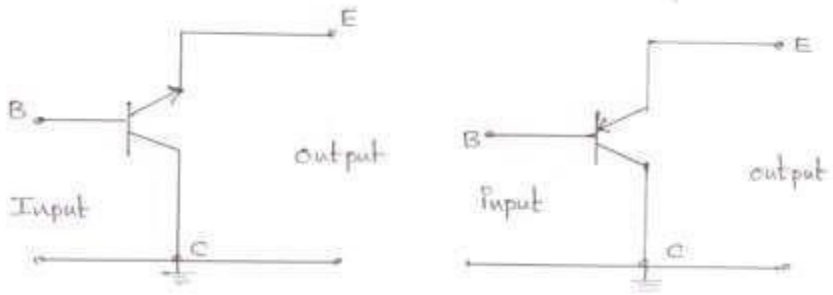


Fig. Common – Collector configuration

Common – Base (CB) configurations:

In this configuration, the input signal is applied between emitter and base while the output is taken from collector and base. As base is common to input and output circuits, hence the name common-base configuration. Figure show the common-base P-N-P transistor circuit.

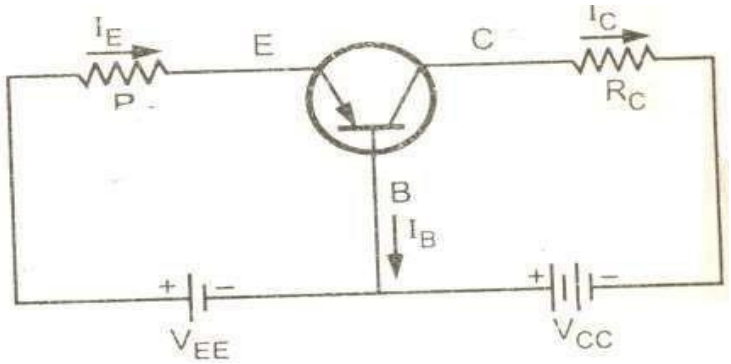


Fig. Common – base PNP transistor amplifier.

Current Amplification Factor (α):

When no signal is applied, then the ratio of the collector current to the emitter current is called dc alpha (α_{dc}) of a transistor.

$$\alpha_{dc} = \frac{-I_C}{I_E} \quad \text{,..... (1)}$$

(Negative sign signifies that I_E flows into transistor while I_C flows out of it).

„α “ of a transistor is a measure of the quality of a transistor. Higher is the value of „α “, better is the transistor in the sense that collector current approaches the emitter current.

By considering only magnitudes of the currents, $I_C = \alpha I_E$ and hence $I_B = I_E - I_C$

Therefore, $I_B = I_E - \alpha I_E = I_E(1-\alpha)$.....(2)

When signal is applied, the ratio of change in collector current to the change in emitter current at constant collector-base voltage is defined as current amplification factor,

$$\alpha_{dc} = -\frac{\Delta I_C}{\Delta I_E} \quad \text{..... (3)}$$

For all practical purposes, $\alpha_{dc} = \alpha_{ac} = \alpha$ and practical values in commercial transistors range from 0.9 to 0.99.

Total Collector Current:

The total collector current consists of the following two parts:

i) αI_E, current due to majority carriers
ii) I_{CBO}, current due to minority carriers

$\therefore$ Total collector current $I_C = \alpha I_E + I_{CBO}$.....(4)

The collector current can also be expressed as $I_C = \alpha (I_B + I_C) + I_{CBO}$ ($\Delta I_E = I_B + I_C$)

$$\Rightarrow I_C(1-\alpha) = \alpha I_B + I_{CBO}$$

$$\Rightarrow I_C = \left(\frac{\alpha}{1-\alpha}\right) I_B + \left(\frac{1}{1-\alpha}\right) I_{CBO} \quad \text{.... (5)}$$

Common-Emitter (CE) configuration:

In this configuration, the input signal is applied between base and emitter and the output is taken from collector and emitter. As emitter is common to input and output circuits, hence the name common emitter configuration.

Figure shows the common-emitter P-N-P transistor circuit.

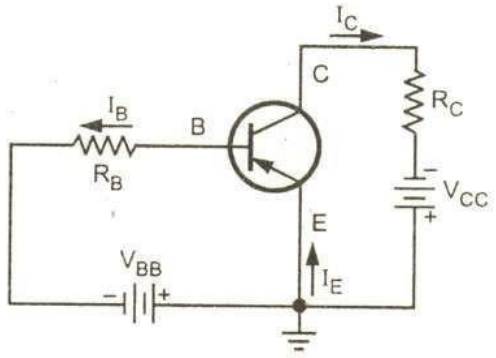


Fig. Common-Emitter PNP transistor amplifier.

Current Amplification Factor (β):

When no signal is applied, then the ratio of collector current to the base current is called dc beta (β_{dc}) of a transistor.

$$\beta_{dc} = \beta = \frac{I_C}{I_B} \quad \text{..... (1)}$$

When signal is applied, the ratio of change in collector current to the change in base current is defined as base current amplification factor. Thus,

$$\beta_{dc} = \beta = \frac{\Delta I_C}{\Delta I_B} \quad \text{.....(2)}$$

From equation (1), $I_C = \beta I_B$

Almost in all transistors, the base current is less than 5% of the emitter current. Due to this fact, „β" ranges from 20 to 500. Hence this configuration is frequently used when appreciable current gain as well as voltage gain is required.

Total Collector Current:

The Total collector current $I_C = \beta I_B + I_{CEO}$ .....(3)

Where I_{CEO} is the leakage current.

But, we have, $I_C = \left(\frac{\alpha}{1-\alpha}\right) I_B + \left(\frac{1}{1-\alpha}\right) ICBO$ .....(4)

Comparing equations (3) and (4), we get

$$\beta = \frac{\alpha}{1-\alpha} \text{ and } I_{CEO} = \frac{1}{1-\alpha} I_{CBO} \quad \text{.....(5)}$$

Relation between α and β :

We know that $\alpha = \frac{I_C}{I_E}$ and $\beta = \frac{I_C}{I_B}$

$$I_E = I_B + I_C \qquad \text{(or)} \qquad I_B = I_E - I_C$$

Now
$$\beta = \frac{I_C}{I_E - I_C} = \frac{\frac{I_C}{I_E}}{1 - \frac{I_C}{I_E}} = \frac{\alpha}{1-\alpha} \qquad \text{..... (6)}$$

$$\Rightarrow \beta(1-\alpha) = \alpha \quad \text{(or)} \quad \beta = \alpha(1+\beta)$$

$$\Rightarrow \alpha = \frac{\beta}{1+\beta} \qquad \text{..... (7)}$$

It can be seen that $1-\alpha = \frac{1}{1+\beta}$ ..... (8)

Common – Collector (CC) Configuration:

In this configuration, the input signal is applied between base and collector and the output is taken from the emitter. As collector is common to input and output circuits, hence the name common collector configuration. Figure shows the common collector PNP transistor circuit.

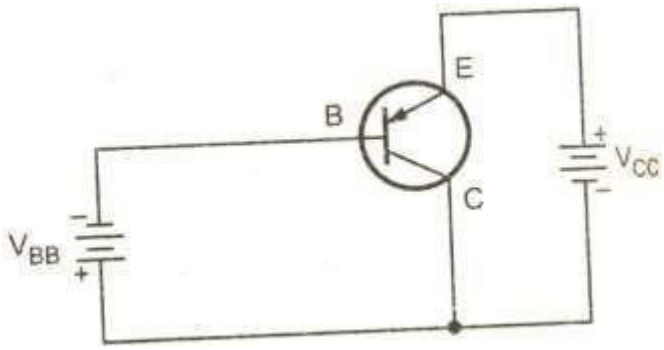


Fig. Common collector PNP transistor amplifier.

Current Amplification Factor (γ):

When no signal is applied, then the ratio of emitter current to the base current is called as dc gamma (γ_{dc}) of the transistor.

$$\gamma_{dc} = \gamma = \frac{I_E}{I_B} \qquad \text{..... (1)}$$

When signal is applied, then the ratio of change in emitter current to the change in base current is known as current amplification factor „ γ “.

$$\gamma_{ac} = \gamma = \frac{\Delta I_E}{\Delta I_B} \qquad \text{.....(2)}$$

This configuration provides the same current gain as common emitter circuit as $\Delta I_E \approx \Delta I_C$ but the voltage gain is always less than one.

Total Emitter Current:

We know that $I_E = I_B + I_C$ Also $I_C = \alpha I_E + I_{CBO}$

$I_E = I_B + (\alpha I_E + I_{CBO})$

$$\Rightarrow I_E(1-\alpha) = I_B + I_{CBO}$$

$$\Rightarrow I_E = \frac{I_B}{1-\alpha} + \frac{I_{CBO}}{1-\alpha}$$

(or) $$\Rightarrow I_E = (1+\beta)I_B + (1+\beta)I_{CBO} \quad \text{..... (3)} \qquad \left(\because \frac{1}{1-\alpha} = 1+\beta\right)$$

Relation between γ and α :

We know that $\gamma = \frac{I_E}{I_B}$ and $\alpha = \frac{I_C}{I_B}$

Also $I_B = I_E - I_C$

Now $$\gamma = \frac{I_E}{I_E - I_C} = \frac{1}{1 - \frac{I_C}{I_E}} = \frac{1}{1-\alpha}$$

$$\therefore \gamma = \frac{1}{1-\alpha} \quad \text{..... (4)}$$

Relation between γ and β :

We know that $\frac{1}{1-\alpha} = 1+\beta$

$\therefore$ From equation (4), $$\gamma = \frac{1}{1-\alpha} = 1+\beta \quad \text{..... (5)}$$

Characteristics of Common-Base Circuit:

The circuit diagram for determining the static characteristic curves of an NPN transistor in the common base configuration is shown in fig. below.

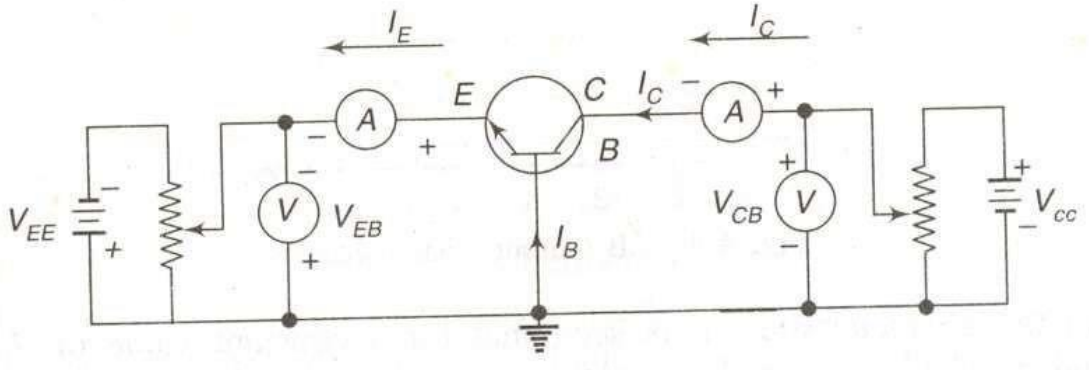


Fig. Circuit to determine CB static characteristics.

Input Characteristics:

To determine the input characteristics, the collector-base voltage V_{CB} is kept constant at zero volts and the emitter current I_E is increased from zero in suitable equal steps by increasing V_{EB}. This is repeated for higher fixed values of V_{CB}. A curve is drawn between emitter current I_E and emitter-base voltage V_{EB} at constant collector-base voltage V_{CB}.

The input characteristics thus obtained are shown in figure below.

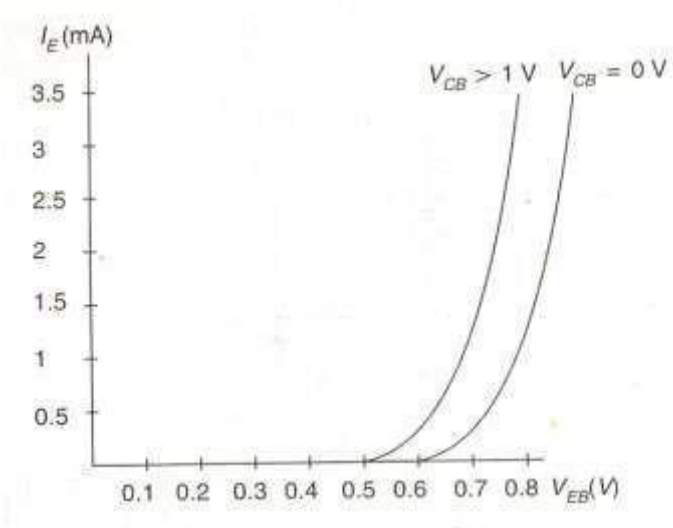
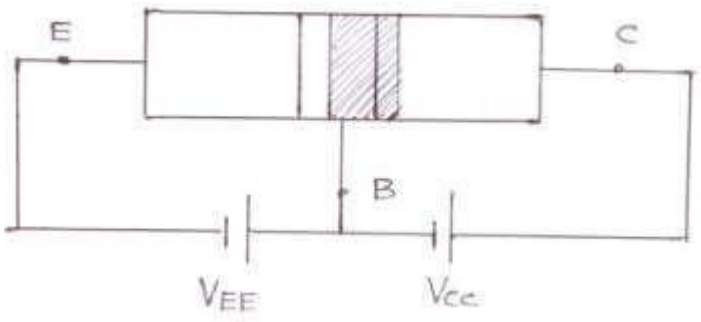


Fig. CB Input characteristics.

Early effect (or) Base – Width modulation:

As the collector voltage V_{CC} is made to increase the reverse bias, the space charge width between collector and base tends to increase, with the result that the effective width of the base decreases. This dependency of base-width on collector-to-emitter voltage is known as Early effect (or) Base-Width modulation.



Thus decrease in effective base width has following consequences:

i. Due to Early effect, the base width reduces, there is a less chance of recombination of holes with electrons in base region and hence base current I_B decreases.

ii. As I_B decreases, the collector current I_C increases.

iii. As base width reduces the emitter current I_E increases for small emitter to base voltage.

iv. As collector current increases, common base current gain (α) increases.

Punch Through (or) Reach Through:

When reverse bias voltage increases more, the depletion region moves towards emitter junction and effective base width reduces to zero. This causes breakdown in the transistor. This condition is called "Punch Through" condition.

Output Characteristics:

To determine the output characteristics, the emitter current I_E is kept constant at a suitable value by adjusting the emitter-base voltage V_{EB}. Then V_{CB} is increased in suitable equal steps and the collector current I_C is noted for each value of I_E. Now the curves of I_C versus V_{CB} are plotted for constant values of I_E and the output characteristics thus obtained is shown in figure below.

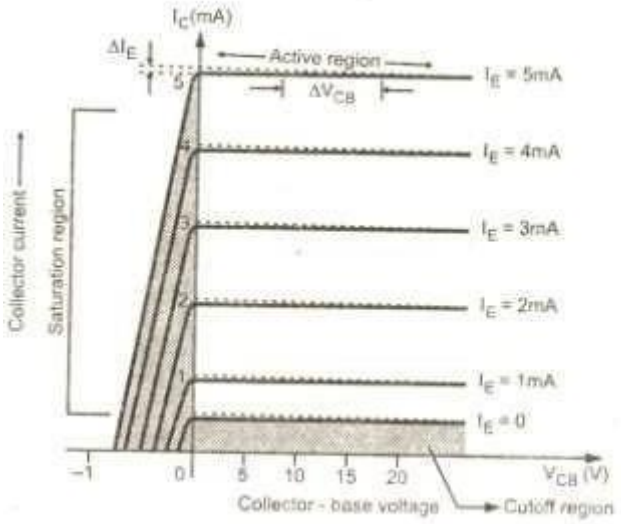


Fig. CB Output characteristics

From the characteristics, it is seen that for a constant value of I_E, I_C is independent of V_{CB} and the curves are parallel to the axis of V_{CB}. Further, I_C flows even when V_{CB} is equal to zero. As the emitter-base junction is forward biased, the majority carriers, i.e., electrons, from the emitter are injected into the base region. Due to the action of the internal potential barrier at the reverse biased collector-base junction, they flow to the collector region and give rise to I_C even when V_{CB} is equal to zero.

Transistor Parameters:

The slope of the CB characteristics will give the following four transistor parameters. Since these parameters have different dimensions, they are commonly known as common base hybrid parameters (or) h-parameters.

i) Input Impedance (h_{ib}):

It is defined as the ratio of change in (input) emitter to base voltage to the change in (input) emitter current with the (output) collector to base voltage kept constant. Therefore,

$$h_{ib} = \frac{\Delta V_{EB}}{\Delta I_E}$$, V_{CB} constant

It is the slope of CB input characteristics curve.

The typical value of h_{ib} ranges from 20Ω to 50Ω.

ii) Output Admittance (h_{ob}):

It is defined as the ratio of change in the (output) collector current to the corresponding change in the (output) collector-base voltage, keeping the (input) emitter current I_E constant. Therefore,

$$h_{ob} = \frac{\Delta I_C}{\Delta V_{CB}}$$, I_E constant

It is the slope of CB output characteristics I_C versus V_{CB}.

The typical value of this parameter is of the order of 0.1 to 10μmhos.

iii) Forward Current Gain (h_{fb}):

It is defined as a ratio of the change in the (output) collector current to the corresponding change in the (input) emitter current keeping the (output) collector voltage V_{CB} constant. Hence,

$$h_{fb} = \frac{\Delta I_C}{\Delta I_E}, \quad V_{CB} \text{ constant}$$

It is the slope of I_C versus I_E curve. Its typical value varies from 0.9 to 1.0.

iv) Reverse Voltage Gain (h_{rb}):

It is defined as a ratio of the change in the (input) emitter voltage and the corresponding change in (output) collector voltage with constant (input) emitter current, I_E.

Hence, $$h_{rb} = \frac{\Delta V_{EB}}{\Delta V_{CB}}, \quad I_E \text{ constant.}$$

It is the slope of V_{EB} versus V_{CB} curve. Its typical value is of the order of 10^{-5} to 10^{-4}.

Characteristics of Common-Emitter Circuit:

The circuit diagram for determining the static characteristic curves of the an N-P-N transistor in the common emitter configuration is shown in figure below.

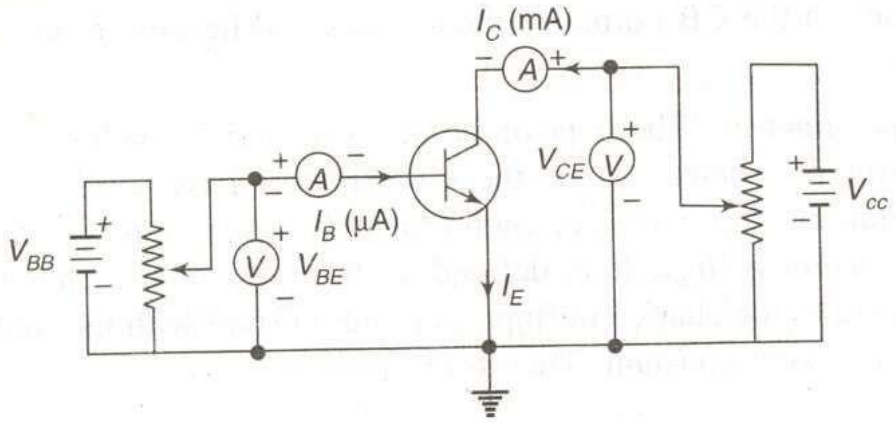


Fig. Circuit to determine CE Static characteristics.

Input Characteristics:

To determine the input characteristics, the collector to emitter voltage is kept constant at zero volts and base current is increased from zero in equal steps by increasing V_{BE} in the circuit. The value of V_{BE} is noted for each setting of I_B. This procedure is repeated for higher fixed values of V_{CE}, and the curves of I_B versus V_{BE} are drawn.

The input characteristics thus obtained are shown in figure below.

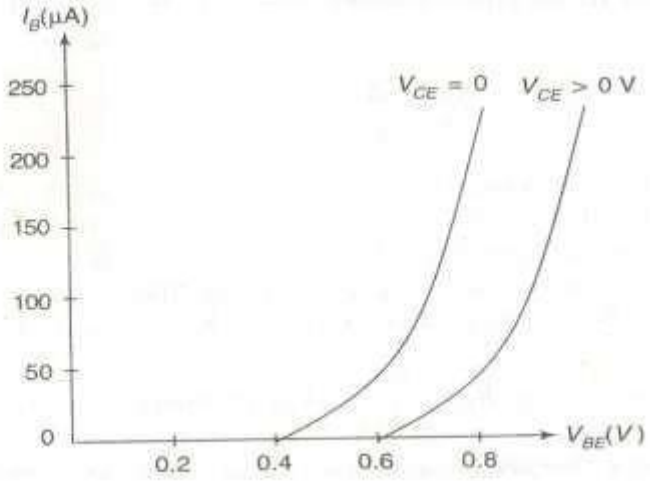


Fig. CE Input Characteristics.

When V_{CE}=0 , the emitter-base junction is forward biased and he junction behaves as a forward biased diode. When V_{CE} is increased, the width of the depletion region at the reverse biased collector-base junction will increase. Hence he effective width of the base will decrease. This effect causes a decrease in the base current I_B. Hence, to get the same value of I_B as that for V_{CE}=0, V_{BE} should be increased. Therefore, the curve shifts to the right as V_{CE} increases.

Output Characteristics:

To determine the output characteristics, the base current I_B is kept constant at a suitable value by adjusting base-emitter voltage, V_{BE}. The magnitude of collector-emitter voltage V_{CE} is increased in suitable equal steps from zero and the collector current I_C is noted for each setting of V_{CE}. Now the curves of I_C versus V_{CE} are plotted for different constant values of I_B. The output characteristics thus obtained are shown in figure below.

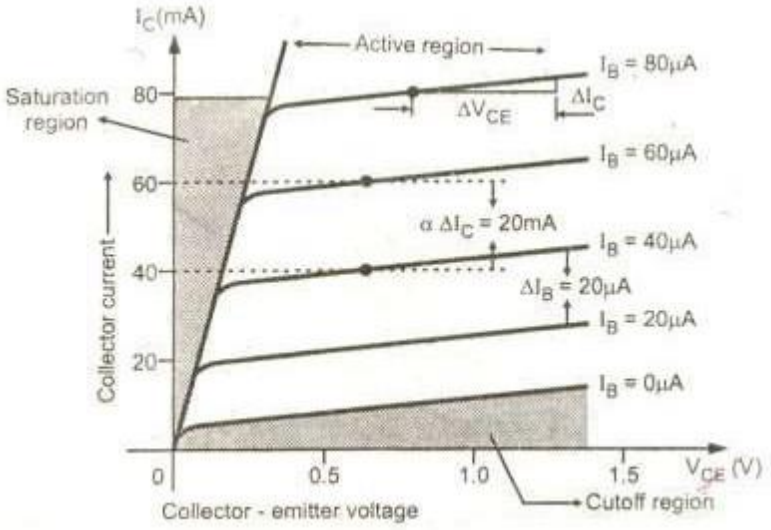


Fig. CE Output characteristics

The output characteristics of common emitter configuration consist of three regions: Active, Saturation and Cut-off regions.

Active Region: The region where the curves are approximately horizontal is the "Active" region of the CE configuration. In the active region, the collector junction is reverse biased. As V_{CE} is increased, reverse bias increase. This causes depletion region to spread more in base than in collector, reducing the changes of recombination in the base. This increase the value of α_{dc}. This Early effect causes collector current to rise more sharply with increasing V_{CE} in the active region of output characteristics of CE transistor.

Saturation Region: If V_{CE} is reduced to a small value such as 0.2V, then collector-base junction becomes forward biased, since the emitter-base junction is already forward biased by 0.7V. The input junction in CE configuration is base to emitter junction, which is always forward biased to operate transistor in active region. Thus input characteristics of CE configuration are similar to forward characteristics of p-n junction diode. When both the junctions are forwards biased, the transistor operates in the saturation region, which is indicated on the output characteristics. The saturation value of V_{CE}, designated $V_{CE(Sat)}$, usually ranges between 0.1V to 0.3V.

Cut-Off Region: When the input base current is made equal to zero, the collector current is the reverse leakage current I_{CEO}. Accordingly, in order to cut off the transistor, it is not enough to reduce I_B=0. Instead, it is necessary to reverse bias the emitter junction slightly. We shall define cut off as the condition where the collector current is equal to the reverse saturation current I_{CO} and the emitter current is zero.

Transistor Parameters:

The slope of the CE characteristics will give the following four transistor parameters. Since these parameters have different dimensions, they are commonly known as Common emitter hybrid parameters (or) h-parameters.

i) Input Impedance (h_{ib}):

It is defined as the ratio of change in (input) base voltage to the change in (input) base current with the (output) collector voltage (V_{CE}), kept constant. Therefore,

$$h_{ie} = \frac{\Delta V_{BE}}{\Delta I_B} \text{ , } \Delta V_{CE} \text{ constant}$$

It is the slope of CB input characteristics I_B versus V_{BE}.

The typical value of h_{ie} ranges from 500Ω to 2000Ω.

ii) Output Admittance (h_{oe}):

It is defined as the ratio of change in the (output) collector current to the corresponding change in the (output) collector voltage. With the (input) base current I_B kept constant. Therefore,

$$h_{oe} = \frac{\Delta I_C}{\Delta V_{CE}} \text{ , } I_B \text{ constant}$$

It is the slope of CE output characteristics I_C versus V_{CE}.

The typical value of this parameter is of the order of 0.1 to 10μmhos.

iii) Forward Current Gain (h_{fe}):

It is defined as a ratio of the change in the (output) collector current to the corresponding change in the (input) base current keeping the (output) collector voltage V_{CE} constant. Hence,

$$h_{fe} = \frac{\Delta I_C}{\Delta I_B}, V_{CE} \text{ constant}$$

It is the slope of I_C versus I_B curve.

Its typical value varies from 20 to 200.

iv) Reverse Voltage Gain (h_{re}):

It is defined as a ratio of the change in the (input) base voltage and the corresponding change in (output) collector voltage with constant (input) base current, I_B. Hence,

$$h_{re} = \frac{\Delta V_{BE}}{\Delta V_{CE}}, I_E \text{ constant.}$$

It is the slope of V_{BE} versus V_{CE} curve.

Its typical value is of the order of 10^{-5} to 10^{-4}.

Characteristics of common collector circuit:

The circuit diagram for determining the static characteristics of an N-P-N transistor in the common collector configuration is shown in fig. below.

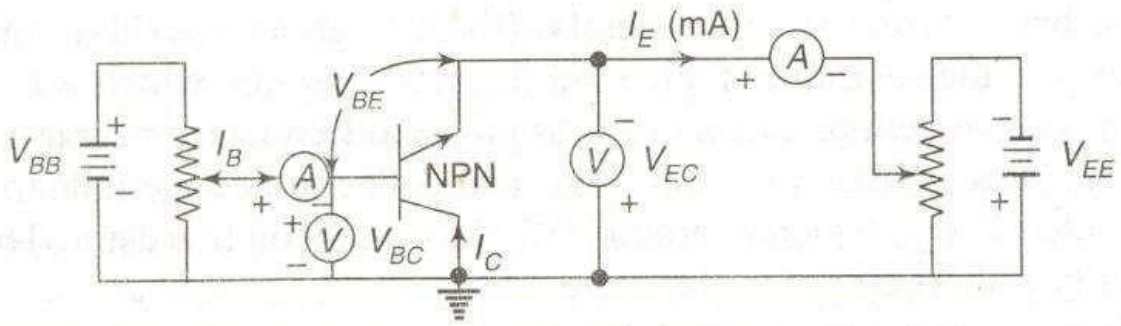


Fig. Circuit to determine CC static characteristics.

Input Characteristics:

To determine the input characteristic, V_{EC} is kept at a suitable fixed value. The base-collector voltage V_{BC} is increased in equal steps and the corresponding increase in I_B is noted. This is repeated for different fixed values of V_{EC}. Plots of V_{BC} versus I_B for different values of V_{EC} shown in figure are the input characteristics.

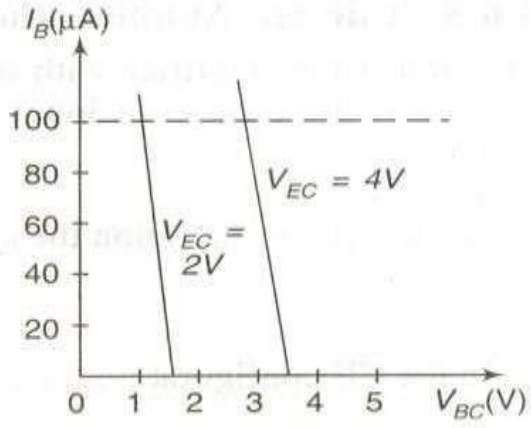


Fig. CC Input Characteristics.

Output Characteristics:

The output characteristics shown in figure below are the same as those of the common emitter configuration.

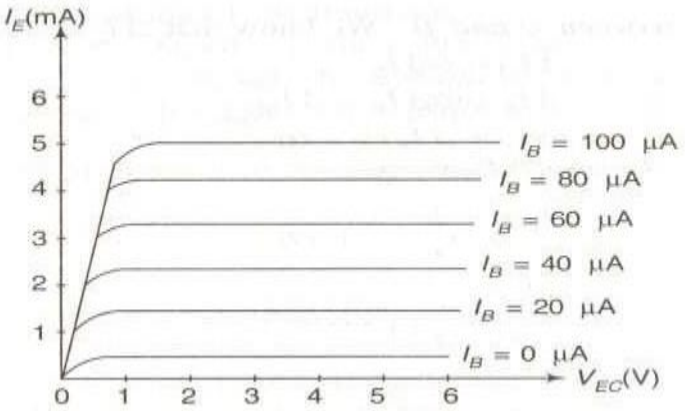


Fig. CC output characteristics.

Comparison:

Table: A comparison of CB, CE and CC configurations

Property	CB	CE	CC
Input Resistance	Low (About 100Ω)	Moderate (About 750Ω)	High (About 750kΩ)
Output Resistance	High (About 450kΩ)	Moderate (About 45kΩ)	Low (About 25Ω)
Current Gain	1	High	High
Voltage Gain	About 150	About 500	Less than 1
Phase Shift between input and output voltages	0^o (or) 360^o	180^o	0^o (or) 360^o
Applications	For high frequency circuits	For Audio frequency circuits	For impedance matching

Problem:

1 A Germanium transistor used in a complementary symmetry amplifier has I_{CBO}=10μA at 27°C and h_{fe}=50.

(a) find I_C when I_B=0.25mA and

(b) Assuming h_{fe} does not increase with temperature; find the value of new collector current, if the transistor"s temperature rises to 50°C.

Solution:

Given data: I_{CBO} = 10μA and h_{fe} (=β) = 50

a) $I_C = \beta I_B+(1+\beta)I_{CBO}$

$= 50x(0.25x10^{-3})+(1+50)x(10x10^{-6})A$

$=$**13.01mA**

b) $I"_{CBO}$ (β=50) $= I_{CBO} \times 2^{(T_2-T_1)/10}$

$= 10 \times 2^{(50-27)/10}$

$= 10 \times 2^{2.3}$ μA

$= 49.2\mu A$

I_C at 50°C is

$I_C= \beta I_B+(1+\beta)I"_{CBO}$

$= 50x(0.25x10^{-3})+(1+50)x(49.2x10^{-6})$

=15.01 mA.

UNIJUNCTION TRANSISTOR:

Uni Junction Transistor (UJT) is a three terminal semi conductor switching device. As it has only one PN junction and three leads, it is commonly called as Uni Junction Transistor.

The three terminals are: Emitter (E), Base1 (B1) and Base2 (B2).

Construction and Symbol:

The basic structure and symbol of UJT is shown in figure below.

It consists of a lightly doped n-type silicon bar with a heavily doped p-type material alloyed to its one side closer to B2 for producing single PN junction.

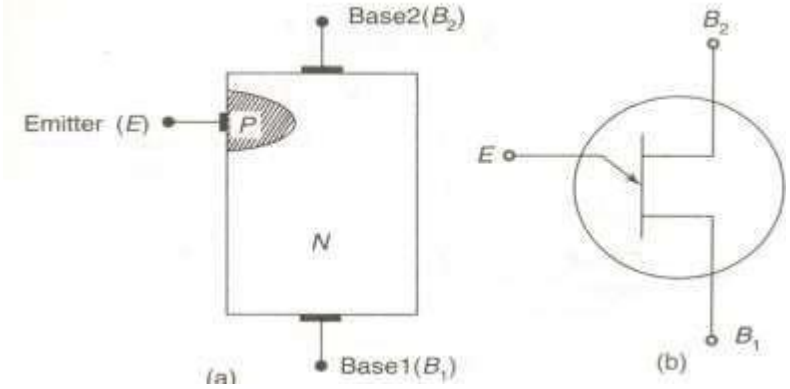


Fig. UJT (a) Basic structure (b) Circuit symbol

Here the emitter leg is drawn at an angle to the vertical and the arrow indicates the direction of the conventional current.

Operation of UJT:

The inter base resistance between B2 and B1 of the silicon bar is, $R_{BB}=R_{B1}+R_{B2}$.

With emitter terminal open, if voltage V_{BB} is applied between the two bases, a voltage gradient is established along the n-type bar.

The voltage drop across R_{B1} is given by $V_1 = \eta V_{BB}$, where the intrinsic stand-off ratio $\eta = \dfrac{R_{B1}}{R_{B1}+R_{B2}}$. The typical value of η ranges from 0.56 to 0.75.

This voltage V_1 reverse biases the PN-junction and emitter current is cut-off. But a small leakage current flows from B2 to emitter due to minority carriers. The equivalent circuit of UJT is shown in figure below.

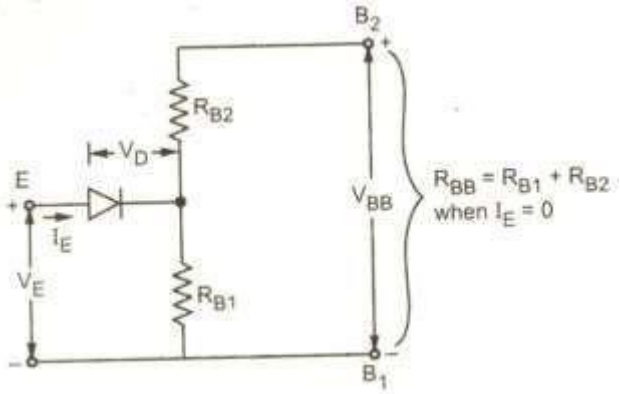


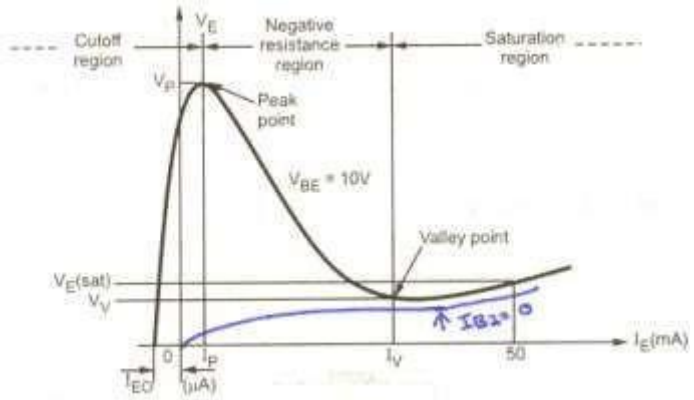
Fig. UJT equivalent circuit.

If a negative voltage is applied to the emitter, PN-junction remains reverse biased and the emitter current is cut-of. The device is now in the „OFF" state.

If a positive voltage V_E is applied to the emitter, the PN-junction will remain reverse biased so long as V_E is less than V_1. If V_E exceeds V_1 by the cut-in voltage vY, the diode becomes forward biased. Under this condition, holes are injected into n-type bar. These holes are repelled by the terminal B2 and are attracted by the terminal B1. Accumulations of holes in E to B1 region reduce the resistance in this section and hence emitter current I_E is increased and is limited by V_E. The device is now in the „ON" state.

Characteristics of UJT:

Figure below shows the input characteristics of UJT.



Here, up to the peak point P, the diode is reverse biased and hence, the region to the left of the peak point is called cut-off region.

At P, the peak voltage $V_P = \eta V_{BB} + V_\gamma$, the diode starts conducting and holes are injected into n-layer. Hence, resistance decreases thereby decreasing V_E for the increase in I_E. SO there is a negative resistance region from peak point P to valley point V.

After the valley point, the device is driven into saturation and behaves like a conventional forward biased PN-junction diode. The region to the right of the valley point is called saturation region. In the valley point, the resistance is changes from negative to positive. The resistance remains positive in the saturation region.

Due to the negative resistance property, a UJT can be employed in a variety of applications, viz., a saw-tooth wave generator, pulse generator, switching, timing and phase control circuits.

UJT Relaxation Oscillator:

The Relaxation oscillator using UJT which is meant for generating saw-tooth waveform is shown in figure below:

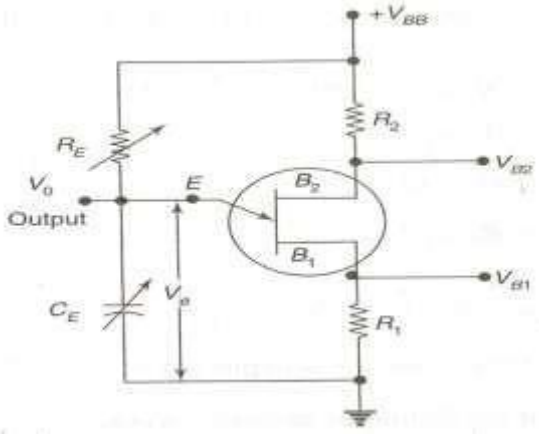
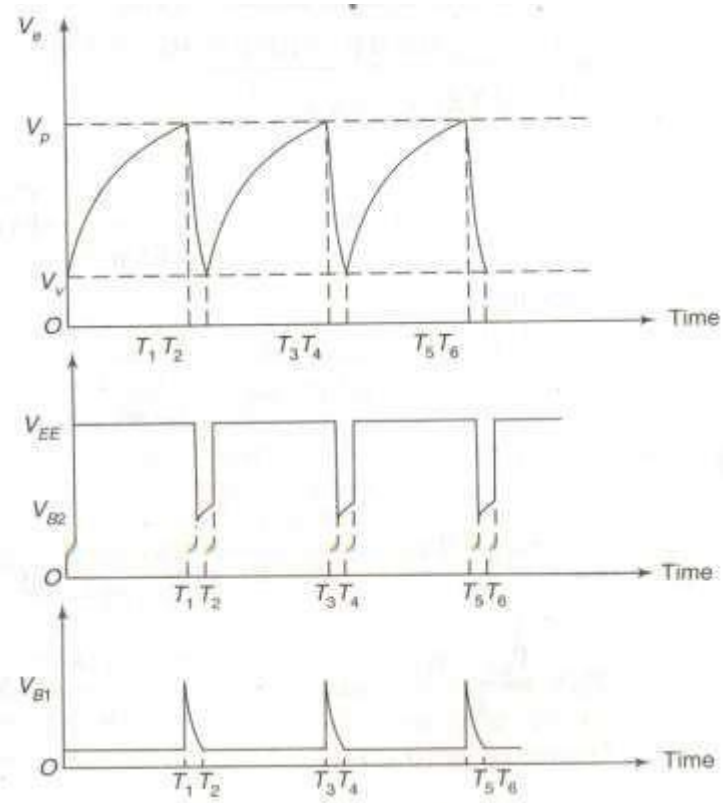


Fig: UJT Relaxation Oscillator.

It consists of a UJT and a capacitor C_E which is charged through R_E as the supply voltage V_{BB} is switched ON.



The voltage across the capacitor increases exponentially and when the capacitor voltage reach the peak point voltage V_P, the UJT starts conducting and the capacitor voltage is discharged rapidly through EB1 and R1.

After the peak point voltage of UJT is reached, it provides negative resistance to the discharge path which is useful in the working of the relaxation oscillator. As the capacitor voltage reaches zero, the device then cuts off and capacitor C_E starts to charge again. This cycle is repeated continuously generating a saw-tooth waveform across C_E.

The inclusion of external resistors R2 and R1 in series with B2 and B1 provides spike waveforms. When the UJT fires, the sudden surge of current through B1 causes drop across R1, which provides positive going spikes.

Also, at the time of firing, fall of V_{EB1} causes I_2 to increase rapidly which generates negative going spikes across R_2. By changing the values of capacitance C_E (or) resistance R_E, frequency of the output waveform can be changed as desired, since these values control the time constant R_EC_E of the capacitor changing circuit.

Frequency of oscillations:

The time period and hence the frequency of the saw-tooth wave can be calculated as follows. Assuming that the capacitor is initially uncharged, the voltage V_C across the capacitor prior to breakdown is given by

$$V_C = V_{BB}\left(1 - e^{-t/R_E C_E}\right)$$

Where R_EC_E = charging time constant of resistor-capacitor circuit, and t= time from the commencement of the waveform. The discharge of the capacitor occurs when V_C is equal to the peak-point voltage V_P, i.e,

$$\Rightarrow \eta = 1 - e^{-t/R_E C_E}$$

$$e^{-t/R_E C_E} = 1 - \eta$$

$$\therefore t = R_E C_E \log_e \left(\frac{1}{1-\eta} \right)$$

$$= 2.303 R_E C_E \log_{10} \left(\frac{1}{1-\eta} \right)$$

If the discharge time of the capacitor is neglected, then t=T, the period of the wave. Therefore, frequency of oscillations of saw-tooth wave,

$$f = \frac{1}{T} = \frac{1}{2.3 R_E C_E \log_{10} \left(\frac{1}{1-\eta} \right)}$$

AMPLIFIERS :

INTRODUCTION:

A circuit that increases the amplitude of the given input signal is an „Amplifier". A small a.c. signal fed to the amplifier is obtained as a larger a.c. signal of the same frequency at the output. In discrete circuits, bipolar junction transistors and Field Effect transistors are commonly used as amplifying elements.

Classification of Amplifiers

Amplifiers can be classified as follows:

1. Based on the active device.
   a) BJT Amplifier
   b) FET Amplifier

2. Based on the transistor configuration.
   a) Common Emitter amplifier
   b) Common Collector amplifier
   c) Common Base amplifier

3. Based on input.
   a) Small signal amplifiers
   b) Large signal amplifiers

4. Based on the output.
   a) Voltage amplifier
   b) Power amplifier

5. Based on the number of stages.
   a) Single stage amplifier
   b) Multistage amplifier

6. Based on the Q-point (Operating conduction)
   a) Class A Amplifier
   b) Class B Amplifier
   c) Class AB Amplifier
   d) Class C Amplifier

7. Based on the frequency response.
   a) Audio frequency amplifier
   b) Intermediate frequency amplifier
   c) Radio frequency amplifier

8. Based on the bandwidth.
   a) Narrow band amplifier
   b) Wide band amplifier

Transistor as an Amplifier:

To make the transistor work as an amplifier, it is to be biased to operate in the active region, i.e., base-emitter junction is to be forward biased, while base-collector junction to be reverse biased.

When only one transistor with associated circuitry is used for amplifying a weak signal, the circuit is known as "Single Stage Transistor Amplifier".

Common Emitter Amplifier Circuit

Let us consider the common emitter amplifier circuit using self bias (or) voltage divider bias as shown in fig1. below.

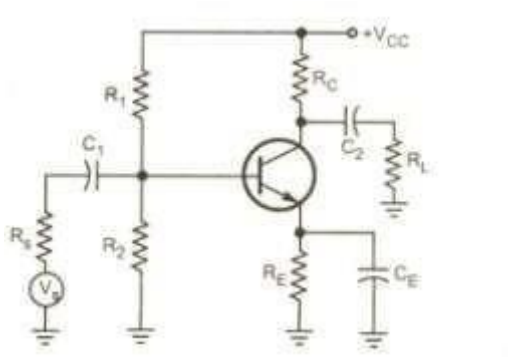


Fig1. Common emitter amplifier

It consists of different circuit components. The functions of these components are as follows.

1. Biasing circuit:

The resistances R_1, R_2 and R_E form the voltage divider biasing circuit for the CE amplifier. It sets the proper operating point for the CE amplifier.

2. Input Capacitor C_1:

This capacitor couples the signal to the base of the transistor. It blocks any dc component present in the signal and passes only ac signal for amplification, because of this, biasing conditions are maintained constant.

3. Emitter Bypass Capacitor C_E:

An emitter bypass capacitor C_E is connected in parallel with the emitter resistance R_E, to provide a low reactance path to the amplified ac signal. If it is not inserted, the amplified a.c signal passing through R_E will cause a voltage drop across it. This will reduce the output voltage, reducing the gain of the amplifier.

4. Output Coupling Capacitor C_2:

The coupling capacitor C_2 couples the output of the amplifier to the load (or) to the next stage of the amplifier. It blocks d.c. and passes only a.c. part of the amplified signal.

Need for C_1, C_2 and C_E:

Consider that the signal source is connected directly to the base of the transistor then we can notice that source resistance R_s is in parallel with R_2, this will reduce the bias voltage at the transistor base and consequently alter the collector current, which is not desired.

Similarly, by connecting R_L directly, the d.c. levels of V_c and V_{CE} will change. To avoid this and maintain the stability of bias condition coupling capacitors are connected. Coupling capacitors acts as open circuits to d.c., maintain stable biasing conditions even after connection of Rs and R_L. Another advantage of connecting C_1 is that any d.c. component in the signal is opposed and only a.c. signal is routed to the transistor amplifier.

The emitter resistance R_E is one of the components which provide bias stabilization. But it also reduces the voltage swing at the output. The emitter bypass capacitor C_E provides a low reactance path to the amplified a.c. signal increasing the output voltage swing.

How Transistor amplifies?

When a weak a.c. signal is given to the base of transistor, a small base current starts flowing. Due to transistor action, a much larger a.c. current flows through the collector resistance R_c. As the value of R_c is quite high (usually 4 – 10 kΩ), therefore, a large voltage appears across R_c. Thus, a weak signal applied in the base circuit appears in amplified form in the collector circuit. It is in this way that a transistor acts as an Amplifier.

Phase Reversal:

The phase relationship between the input and output voltages can be determined by considering the effect of a positive half cycle and negative half cycle separately. Consider the positive half cycle of input signal in which terminal „A" is positive w.r.t. „B" due to this, two voltages, a.c. and d.c. will be adding each other, increasing forward bias in base emitter junction. This increases base current. The collector current is β times the base current, hence the collector current will also increases. This increases the voltage drop across R_c.

Since $V_c = V_{cc} - I_c R_c$

The increase in I_c, results in a drop in collector voltage V_c, as V_{cc} is constant. Thus, as V_i increases in a positive direction, V_0 goes in a negative direction and we get negative half cycle of output voltage for positive half cycle at the input.

In the negative half cycle of input, in which terminal „A" becomes negative w.r.t. terminal „B", the a.c. and d.c. voltages will oppose each other, reducing forward bias on base-emitter p-n junction, this reduces base current. Accordingly collector current and drop across R_c both reduces, increasing the output voltage. Thus, we get positive half cycle at the output for negative half cycle at the input.

Therefore, we can say that there is a phase shift of 180^0 between input and output voltages for a common emitter amplifier.

Common Collector Amplifier Circuit

Common collector amplifier circuit is shown in fig. (2) below.

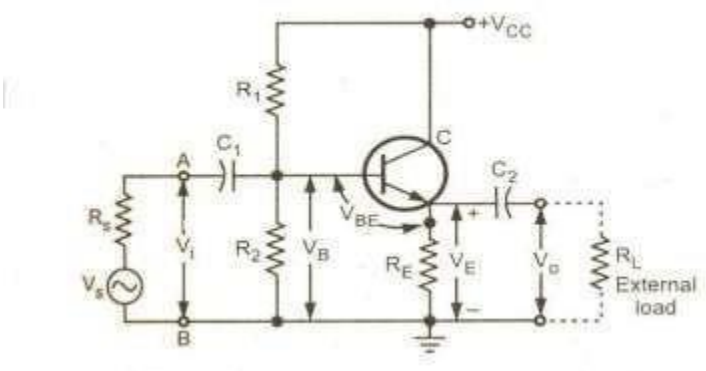


Figure 2. Common Collector Amplifier

The d.c. biasing is provided by R_1, R_2 and R_E. The load resistance is capacitor coupled to the emitter terminal of the transistor.

When a signal is applied via to the base of the transistor, V_B is increased and decreased as the signal goes positive and negative respectively.

From fig. we can write $V_E = V_B - V_{BE}$

By considering V_{BE} is constant, we say that variation in the V_B appears at emitter and emitter voltage V_E will vary same as base voltage V_B.

Since the emitter is output terminal, it can be noted that the output voltage from a common collector circuit is the same as its input voltage. In other words, we can say that in common collector circuit, emitter terminal follows the signal voltage applied to the base. Hence the common collector circuit is also known as an "Emitter Follower".

Common Base Amplifier Circuit

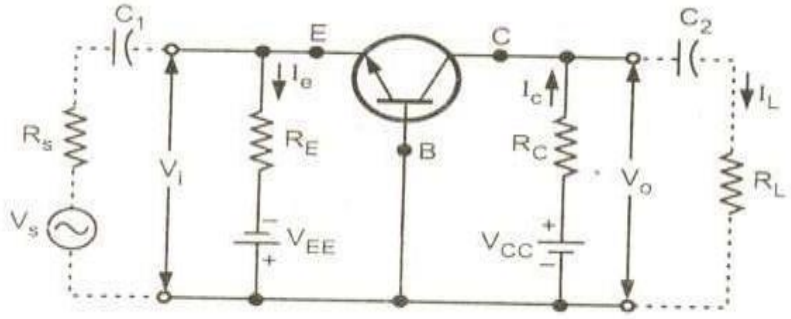


Figure 3. Common Base Amplifier

Common Base Amplifier circuit is shown in fig3. The signal source is coupled to the emitter of the transistor via C_1. The load resistance R_L is coupled to the collector of the transistor via C_2.

The positive going pulse of input source increases the emitter voltages as base voltage is constant; the forward bias of emitter base junction reduces. This reduces I_B, reducing Ic and hence the drop across Rc.

Since Vo = Vcc – Ic Rc the reduction in Ic results in an increase in Vo.

Therefore we can say that positive going input produces positive going output and similarly negative going input produces negative going output and there is no phase shift between input and output in a common base amplifier.

Small Signal transistor models

A small signal linear model represents the operation of the transistor in the active region so that the output is not distorted (i.e., the operating point 'Q' lies in the active region).

Two Port devices and Network parameters:

Fig. 4. A two-port network

A transistor can be treated as a two - port network. The terminal behavior of any two-port network can be specified by the terminal voltages V_1 and V_2 at ports 1 and 2 respectively, and currents I_1 and I_2 entering ports 1 and 2 respectively.

Of these four variables V_1, V_2, I_1 and I_2 two can be selected as independent variables and the remaining two can be expressed in terms of these independent variables. This leads to various two-port parameters out of which the following three are more important.

i) Z - Parameters (or) Impedance Parameters

ii) Y - Parameters (or) Admittance Parameters

iii) H - Parameters (or) Hybrid Parameters

Z - Parameters (or) Impedance Parameters:

Here i_1 and i_2 are taken as independent variables. The voltages V_1 and V_2 are given by the equations.

$$V_1 = Z_{11}i_1 + Z_{12}i_2$$
$$V_2 = Z_{21}i_1 + Z_{22}i_2$$

These four impedance parameters Z_{11}, Z_{22}, Z_{12} and Z_{21} are defined as follows.

$Z_{11} = V_1/i_1$ with $i_2=0$
= Input impedance with Output port open circuited.

$Z_{22} = V_2/i_2$ with $i_1=0$
= Output impedance with Input port open circuited.

$Z_{12} = V_1/i_2$ with $i_1=0$
= Reverse Transfer impedance with port1 open circuited.

$Z_{21} = V_2/i_1$ with $i_2=0$
= Forward Transfer impedance with port2 open circuited.

Y - Parameters (or) Admittance Parameters:

Here V_1 and V_2 are taken as independent variables; the currents i_1 and i_2 are given by the equations.

$$i_1 = Y_{11}\,V_1 + Y_{12}\,V_2$$
$$i_2 = Y_{21}\,V_1 + Y_{22}\,V_2$$

Y_{11}, Y_{12}, Y_{21} and Y_{22} are called short circuited admittance parameters and that are defined as follows.

$Y_{11} = i_1/V_1$ with $V_2=0$
= Input Admittance with port 2 short circuited.

$Y_{22}= i_2/V_2$ with $V_1=0$
= Output Admittance with port 1 short circuited.

$Y_{12}= i_1/V_2$ with $V_1=0$
= Reverse Transfer Admittance with port 1 short circuited.

$Y_{21}= i_2/V_1$ with $V_2=0$
= Forward Transfer Admittance with port 2 short circuited.

h - Parameters (or) Hybrid Parameters:

If the input current i_1 and the output voltage V_2 are taken as independent variables, the input voltage V_1 and output current i_2 can be written as

$$V_1 = h_{11}\, i_1 + h_{12}\, V_2$$
$$i_2 = h_{21}\, i_1 + h_{22}\, V_2$$

The four hybrid parameters h_{11}, h_{12}, h_{21} and h_{22} are defined as follows.

$h_{11}= V_1/i_1$ with $V_2=0$
= Input impedance with output port short circuited.

$h_{22}= i_2/V_2$ with $i_1=0$
= Output Admittance with input port open circuited.

$h_{12}= V_1/V_2$ with $i_1=0$
= Reverse Voltage Transfer ratio with input port open circuited.

$h_{21}= i_2/i_1$ with $V_2=0$
= Forward current gain with output port short circuited.

The dimensions of h - parameters are:

h_{11} - ohms
h_{22} - mhos
h_{12}, h_{21} - dimension less.

As the dimensions are not alike, i.e., they are hybrid in nature, these parameters are called as hybrid parameters.

Notation:

When h - parameters are applied to transistors, first subscript, i - input; o - output; f - forward transfer; r - reverse transfer and Second subscript to designate the type of configuration, e - common emitter; b - common base; c - common collector.

For CE configuration;
- hie - short circuit i/p impedance
- hoe - open circuit o/p impedance
- hre - open circuit reverse voltage transfer ratio
- hfe - short circuit forward current gain

The Hybrid model for two - port network

$$V_1 = h_i\, i_1 + h_r\, V_2$$
$$i_2 = h_f\, i_1 + h_0\, V_2$$

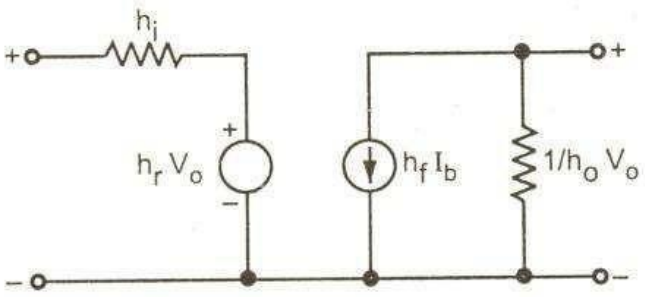


Figure.5. Hybrid model for two-port network

The model can be verified by writing Kirchoff's voltage law in the input loop and Kirchoff's current law for the output node.

Transistor hybrid model:

Use of h-parameters to describe a transistor has the following advantages.

i) h - parameters are real numbers up to radio frequencies.

ii) They are easy to measure.

iii) They can be determined from the transistor static characteristics curve.

iv) They are convenient to use in circuit analysis and design.

v) Easily convertible from one configuration to other.

vi) Readily supplied by manufacturers

Hybrid models for the transistor in three different configurations

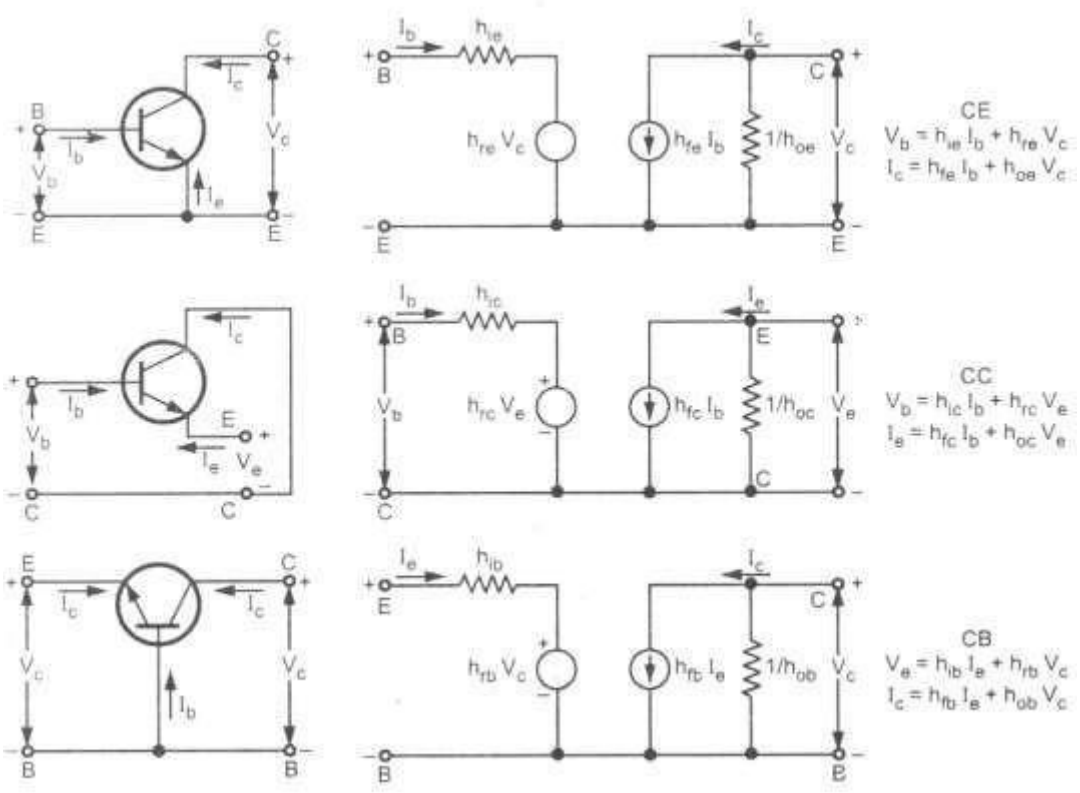


Figure 6. Transistor configurations and their hybrid models

Typical h- parameters values for a transistor

Parameters	CE	CC	CB
hi	1,100 Ω	1,100 Ω	21.6 Ω
hr	2.5×10^{-4}	1	2.9×10^{-4}
hf	50	-51	-0.98
ho	25 μA/v	25 μA/v	0.49 μA/v
1/h0	40K	40K	2.04M Ω

Conversion formulas for h-parameters

CC	CB
$h_{ic} = h_{ie}$	$hib = \frac{hie}{1+hfe}$
$h_{rc} = 1$	$hrb = \frac{hiehoe}{1+hfe} - hre$
$h_{fc} = -(1+h_{fe})$	$hfb = \frac{-hfe}{1+hfe}$
$h_{oc} = h_{oe}$	$hob = \frac{hoe}{1+hfe}$

Analysis of a Transistor Amplifier Circuit Using h– Parameters

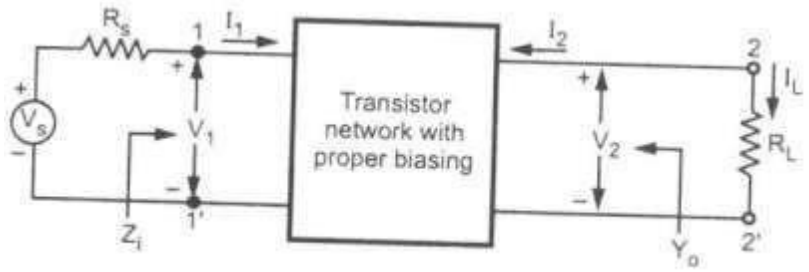


Fig.7. Basic Amplifier circuit

A transistor amplifier can be constructed by connecting an external load and signal source as indicated in fig. above and biasing the transistor properly.

The two – port active network represents a transistor in any of its configuration.

The hybrid equivalent circuit is valid for any type of load whether it is pure resistance (or) impedance (or) another transistor. It is assumed that h-parameters remain constant over the operating range. Further, the input is sinusoidal and I_1, V_1, I_2 and V_2 are phasor quantities.

Current Gain (or) Current Amplification, A_i

For a transistor amplifier, the current gain A_I is defined as the ration of output current to the input current.

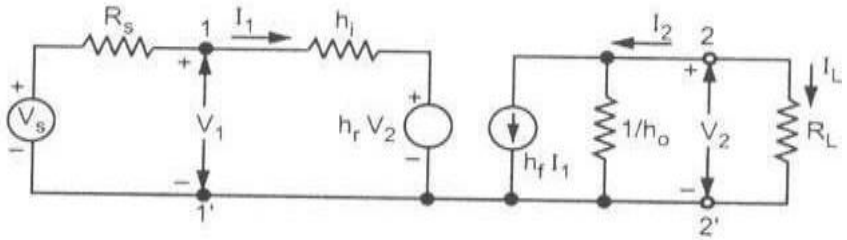


Figure 8. Transistor amplifier in its h-parameter model

From Output circuit

$$I_2 = h_f I_1 + h_0 V_2$$

But $V_2 = I_L Z_L = -I_2 Z_L$

$$\therefore I_2 = h_f I_1 - I_2 Z_L h_0$$

$$I_2 + I_2 Z_L ho = h_f I_1$$

$$I_2 (1 + Z_L ho) = h_f I_1$$

$$A_I = \frac{-I_2}{I_1} = \frac{-h_f}{1 + Z_L ho}$$

$$\therefore \quad A_I = \frac{-h_f}{1+ hoZ_L}$$

Input Impedance (Z_i):

In the circuit, Rs is the signal source resistance. The impedance seen when looking into the amplifier terminals (1, 1") is the amplifier input impedance Z_i , i.e.,

$Z_i = V_1/I_1$

From Input circuit $V_1 = h_i I_1 + h_r V_2$

Hence, $Z_i = \frac{h_i I_1 + h_r V_2}{I_1}$

$$Z_i = h_i + h_r \frac{V_2}{I_1}$$

Substituting $V_2 = -I_2 Z_L = A_I I_1 Z_L$

$$Z_i = h_i + h_r A_i Z_L$$

Substituting for A_I

$$Z_i = h_i - \frac{h_f h_r Z_L}{1+ hoZ_L}$$

$$Z_i = hi - \frac{h_f h_r}{\left(\frac{1}{Z_L} + ho\right)} Z_L$$

Taking the load admittance as $Y_L = \frac{1}{Z_L}$

$$\therefore \quad Z_i = hi - \frac{h_f h_r}{Y_L + ho}$$

Voltage Gain (or) Voltage Amplification factor (A_v):

The ratio of the output voltage V_2 to the input voltage V_i gives the voltage gain of the transistor. i.e., $A_V = \frac{V_2}{V_1}$

Substituting $V_2 = -I_2 Z_L = A_I I_1 Z_L$

$$A_V = \frac{A_I I_1 Z_L}{V_1} = \frac{A_I Z_L}{Z_i}$$

$$\therefore A_V = \frac{A_I Z_L}{Z_i}$$

Output Admittance (Y_0):

By definition, Yo is obtained by setting V_1 to zero, Z_L to infinity and by driving the output terminals from a generator V_2. . If the current drawn from V_2 is I_2, then

$Y_0 = \frac{I_2}{V_2}$ With $V_1 = 0$ and $R_L = \infty$

From the circuit, $I_2 = h_f I_1 + h_0 V_2$

Dividing by V_2 $$\frac{I_2}{V_2} = h_f \frac{I_1}{V_2} + h_0$$

From the circuit $$V_1 = h_i I_1 + h_r V_2$$

Dividing by V_2 , and taking $V_1=0$

$$0 = h_i \frac{I_1}{V_2} + h_r$$

$$\Rightarrow \frac{I_1}{V_2} = \frac{-h_r}{h_i}$$

Using this equation in the above equation, we get,

$$\frac{I_2}{V_2} = h_f \left(\frac{-h_r}{h_i} \right) + h_0$$

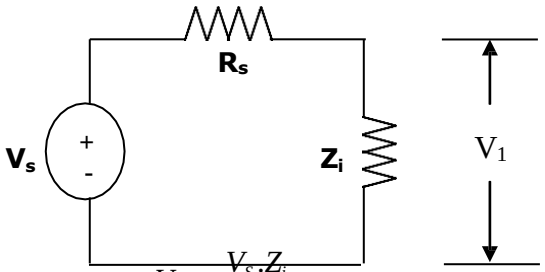
$$\therefore Y_0 = h_0 - \frac{h_f h_r}{h_i}$$

Voltage Amplification (A_{vs}) taking into account the resistance (Rs) of the source:

The overall voltage gain A_{VS} is given by

$$A_{VS} = \frac{V_2}{V_S} = \frac{V_2}{V_1} \cdot \frac{V_1}{V_S} = A_V \cdot \frac{V_1}{V_S}$$

From the equivalent input circuit using Thevenin"s equivalent for the source shown in figure.



$$V_1 = \frac{V_S . Z_i}{Z_i + R_s}$$

$$\frac{V_1}{V_S} = \frac{Z_i}{Z_i + R_s} \quad \text{Then} \quad A_{VS} = \frac{A_V Z_i}{Z_i + R_s}$$

Substituting $$A_V = \frac{A_I Z_L}{Z_i}$$

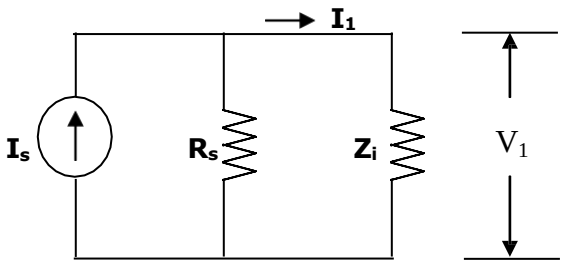
$$\therefore A_{VS} = \frac{A_I Z_L}{Z_i + R_S}$$

Note that if $R_S=0$, then $A_{VS} = \frac{A_I Z_L}{Z_i + R_S} = A_V$. Hence, A_v is the voltage gain with an ideal voltage source (with Rs=0). In practice, A_{VS} is more meaningful than A_v because source resistance has an appreciable effect on the overall amplification.

Current amplification (A_{IS}) taking into account the source resistance:

The equivalent input circuit using Norton"s equivalent circuit for the source, for the calculation of A_{IS} is shown in fig. below.

Overall current gain, $$A_{IS} = \frac{-I_2}{I_S} = \frac{-I_2}{I_1} \cdot \frac{I_1}{I_S} = A_I \cdot \frac{I_1}{I_S}$$



From the figure $$I_1 = I_s \frac{R_s}{R_S + Z_i}$$

and hence, $$\frac{I_1}{I_s} = \frac{R_S}{R_S + Z_i}$$

If Rs=∞, then $A_{IS} = A_I$. Hence, A_I is the current gain with an ideal current source (one with infinite source resistance).

But, $$A_{VS} = \frac{A_I Z_L}{Z_i + R_S} \cdot \frac{R_S}{R_S}$$

$$\Rightarrow A_{VS} = \frac{A_{IS} Z_L}{R_S}$$

Operating Power Gain:

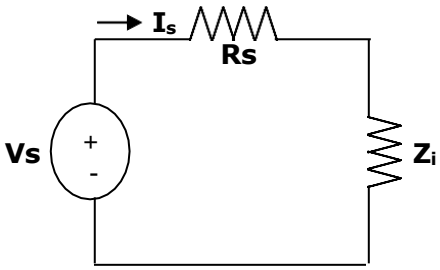
Average power delivered to the load is $P_2 = |V_2||I_L| Cos\theta$, where θ is the phase angle between V_2 and I_L. Assume that Z_L is resistive i.e., $Z_L=R_L$. Since h-parameters are real at low frequencies, the power delivered to the load is $P_2 = V_2 I_L = -V_2 I_2$, since the input power $P_1=V_1I_1$, the operating power gain Ap of the transistor is defined as

$$A_p = \frac{P_2}{P_1} = \frac{-V_2 I_2}{V_1 I_1} = A_v A_i$$

$$A_P = A_I A_I \frac{R_L}{R_i}$$

$$\therefore A_P = A_I^2 \left(\frac{R_L}{R_i} \right)$$

Input impedance taking into account the source resistance (Rs):



$$Z_{IS} = \frac{V_S}{I_S} = R_S + Z_I$$

$$\therefore Z_{IS} = R_S + h_i + h_r A_I Z_L$$

Output impedance taking into account the source resistance (Rs):

By definition, Y_0 is obtained by setting Vs to zero, Z_L to infinitely and by driving the output terminals from a generator V_2.

If the current drawn from V_2 is I_2, then $Y_0 = \frac{I_2}{V_2}$ with Vs=0 and $R_L = \infty$

From the circuit, $I_2 = h_f I_1 + h_0 V_2$

Dividing by V_2, $\frac{I_2}{V_2} = h_f \frac{I_1}{V_2} + h_0$

With Vs=0, by applying KVL in input circuit, $R_S I_1 + h_i I_1 + h_r V_2 = 0$

$I_1[R_s + h_i] + h_r V_2 = 0$

$$\therefore \frac{I_1}{V_2} = \frac{-h_r}{R_S + h_i}$$

Using this in the above equation, we get

$$\frac{I_2}{V_2} = h_f \left(\frac{-h_r}{R_S + h_i} \right) + h_0 \qquad \therefore Y_0 = h_0 - \frac{h_f h_r}{R_S + h_i}$$

SUMMARY

1) $A_I = \frac{-h_f}{1 + ho Z_L}$

2) $Z_i = hi - \frac{h_f h_r}{Y_L + ho}$

3) $Z_{is} = R_s + Z_i$

4) $Y_0 = h_0 - \frac{h_f h_r}{h_i}$

5) $Y_{0S} = h_0 - \frac{h_f h_r}{R_S + h_i}$

6) $A_V = \frac{A_I Z_L}{Z_i}$

7) $A_{VS} = \frac{A_V Z_i}{Z_i + R_s}$

8) $A_{IS} = A_{VS} \cdot \frac{R_S}{Z_L}$

9) $A_P = A_I^2 \left(\frac{R_L}{R_i} \right)$

Analysis of CE amplifier using h-parameter model:

Circuit diagram:

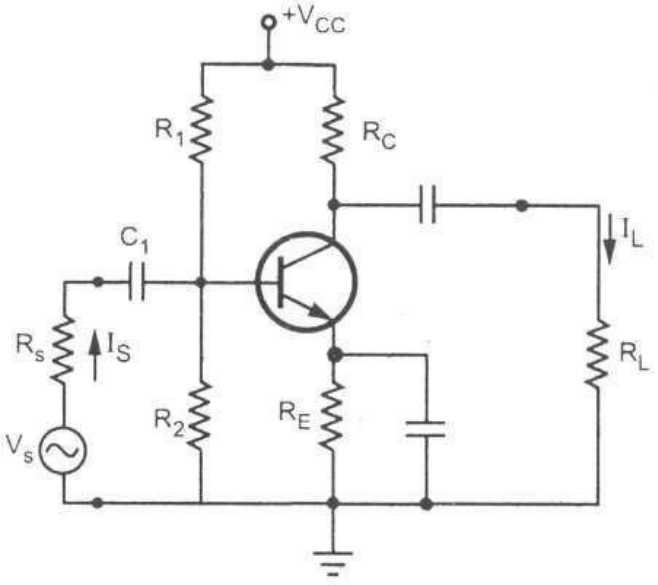
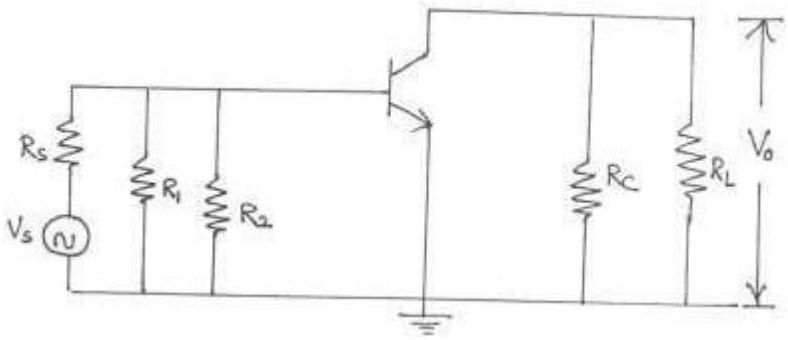


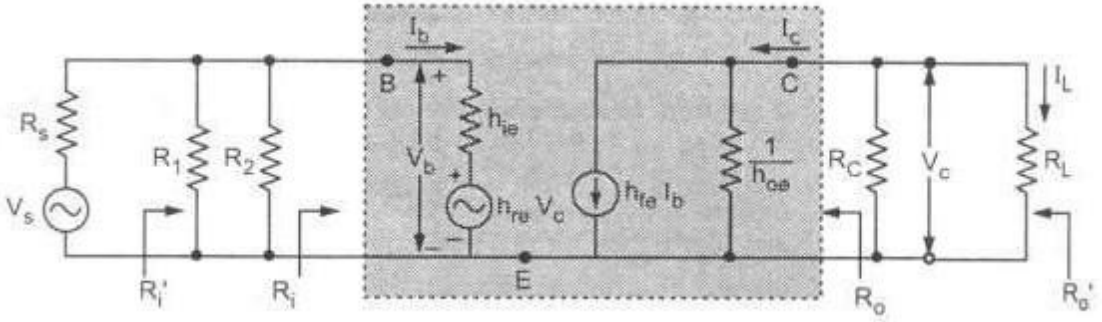
Figure 9. Common Emitter Amplifier

AC equivalent circuit:

i) Vcc=0 ii) Xc=0



h-parameter model equivalent circuit:



Step 1:

Load impedance :

$$Z_L = R_c \,||\, R_L \qquad \text{.....(1)}$$

Step 2:

Current gain (A_I): $A_I = \dfrac{I_0}{I_i} = \dfrac{-i_c}{i_b}$

But, $i_c = h_{fe} i_b + h_{oe} V_c$

$$V_c = -i_c Z_L$$

$$\therefore i_c = h_{fe} i_b + h_{oe}(-i_c Z_L)$$

$$i_c(1 + h_{oe} Z_L) = h_{fe} i_b$$

$$\frac{i_c}{i_b} = \frac{h_{fe}}{1 + h_{oe} Z_L}$$

$$A_I = \frac{-i_c}{i_b} = \frac{-h_{fe}}{1 + h_{oe} Z_L} \qquad \therefore A_I = \frac{-h_{fe}}{1 + h_{oe} Z_L} \qquad \text{.....(2)}$$

Step 3:

Input Impedance (Z_i): $Z_i = \frac{V_i}{I_i} = \frac{V_b}{i_b}$

But, $V_b = h_{ie} i_b + h_{re} V_c$

$$\therefore Z_i = \frac{h_{ie} i_b + h_{re} V_c}{i_b} = h_{ie} + \frac{h_{re}}{i_b} . V_c$$

$$= h_{ie} + \frac{h_{re}[-i_c Z_L]}{i_b} \qquad \because V_c = -i_c Z_L$$

$$\therefore Z_i = h_{ie} + h_{re} A_I Z_L \quad \text{..... (3)} \qquad \because \frac{-i_c}{i_b} = A_I$$

Step 4:

Voltage Gain (A_V): $A_V = \frac{V_0}{V_i} = \frac{V_c}{V_b}$

$$A_V = \frac{-i_c Z_L}{i_b Z_i} = \frac{A_I Z_L}{Z_i} \qquad \because \frac{-i_c}{i_b} = A_I$$

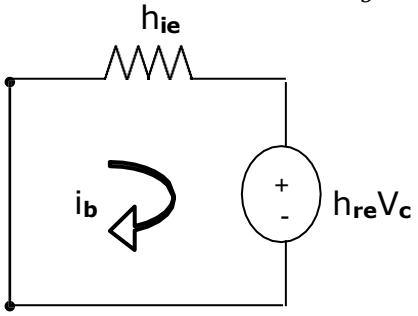
$$\therefore A_V = \frac{A_I Z_L}{Z_i} \quad \text{..... (4)}$$

Step 5:

Output Impedance (Z_0): $Y_0 = \frac{i_c}{V_c}$ at $V_b = 0$

$$Y_0 = \frac{h_{fe} i_b + h_{oe} Vc}{V_c} = h_{oe} + h_{fe}\left(\frac{i_b}{V_c}\right)$$

Short circuiting the input section, $\because V_b = 0$



$$h_{ie} i_b + h_{re} V_c = 0$$

$$\Rightarrow h_{ie} i_b = -h_{re} V_c$$

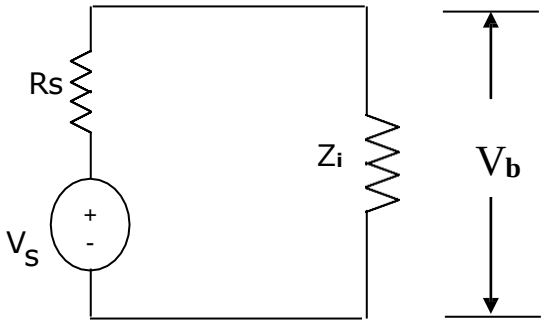
$$\frac{i_b}{V_c} = \frac{-h_{re}}{h_{ie}}$$

$$\therefore Y_0 = h_{oe} - \frac{h_{fe} h_{re}}{h_{ie}} \quad \text{..... (5)}$$

$$Z_0 = \frac{1}{Y_0}$$

Step 6:

Voltage gain by considering Rs into the analysis (A_{VS}):



$$A_{VS} = \frac{V_0}{V_s} = \frac{V_c}{V_b} \cdot \frac{V_b}{V_s}$$

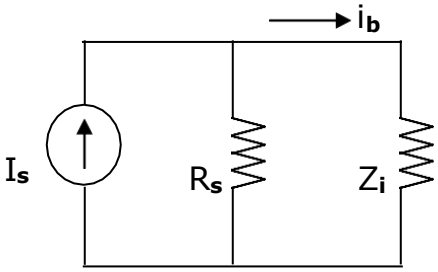
$$V_b = \frac{Z_i}{Z_i + R_s} . V_s$$

$$\frac{V_b}{V_s} = \frac{Z_i}{Z_i + R_s}$$

$$A_{VS} = A_V \cdot \frac{Z_i}{Z_i + R_s} \quad \text{..... (6)}$$

Step 7:

Current gain by considering Rs into the analysis (A_{IS}):



$$A_{IS} = \frac{I_0}{I_s} = \frac{I_0}{i_b} \cdot \frac{i_b}{I_s}$$

$$A_{IS} = \frac{-i_c}{i_b} \cdot \frac{i_b}{i_s} \qquad \because i_0 = -i_c$$

$$A_{IS} = A_I \left(\frac{i_b}{i_s} \right) \qquad \because i_b = \frac{R_s i_s}{R_s + Z_i}$$

$$\frac{i_b}{i_s} = \frac{R_s i_s}{R_s + Z_i}$$

$$\therefore A_{IS} = A_I \frac{R_s}{R_s + Z_i} \quad \text{..... (7)}$$

Step 8:

Input impedance by considering Rs into analysis (Z_{is}):

$$Z_{is} = Z_i + R_S$$

$$\Rightarrow Z_{IS} = h_{ie} + R_s + h_{re} A_I Z_L \quad \text{..... (8)}$$

Step 9:

Output impedance by considering Rs into analysis (Z_{os}):

$$Y_0 = h_{oe} - \frac{h_{fe}h_{re}}{h_{ie}}$$

$$\therefore Y_{os} = h_{oe} - \frac{h_{fe}h_{re}}{h_{ie} + R_s} \quad \text{.....(9)}$$

$$Z_{os} = \frac{1}{Y_{os}}$$

Analysis of CB amplifier using h-parameter model

Circuit diagram:

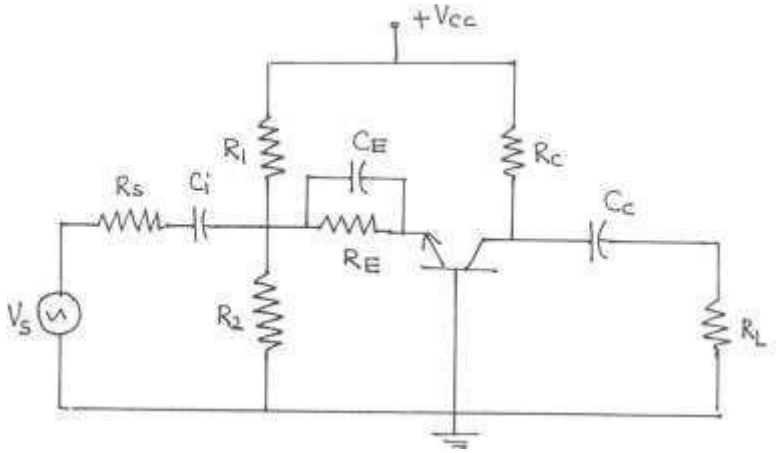
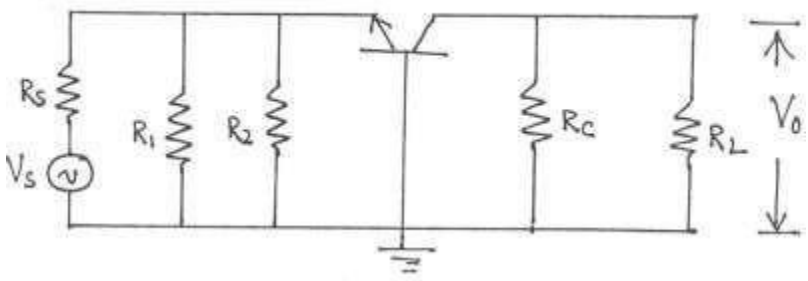


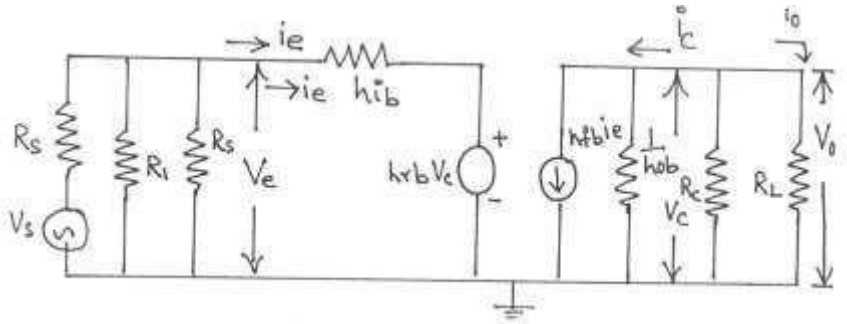
Figure 10. Common Base Amplifier

AC equivalent circuit:

i) Vcc=0 ii) Xc=0



h-parameter model:



Step 1:

Load impedance :

$$Z_L = R_c \,||\, R_L \qquad \text{.....(1)}$$

Step 2:

Current gain (A_I): $A_I = \dfrac{-i_c}{i_e}$

But, $i_c = h_{fb} i_e + h_{ob}$ $\square V_c = -i_c Z_L$

$$\therefore i_c = h_{fb} i_e - h_{ob} i_c Z_L$$

$$i_c(1 + h_{ob} Z_L) = h_{fb} i_e$$

$$\frac{i_c}{i_e} = \frac{h_{fb}}{1 + h_{ob} Z_L}$$

$$\therefore A_I = \frac{-h_{fb}}{1 + h_{ob} Z_L} \qquad \text{..... (2)}$$

Step 3:

Input Impedance (Z_i): $Z_i = \dfrac{V_e}{i_e}$

We have, $V_e = h_{ib} i_e + h_{rb} V_c$

$$\frac{V_e}{i_e} = h_{ib} + h_{rb} \frac{V_c}{i_e}$$

But, $\square V_c = -i_c Z_L$

$$\therefore \frac{V_e}{i_e} = h_{ib} + \frac{h_{rb}(-i_c) Z_L}{i_e}$$

$$\therefore Z_i = h_{ib} + h_{rb} A_I Z_L \text{.....} \quad (3) \qquad \square \frac{-i_c}{i_b} = A_I$$

Step 4:

Voltage Gain (A_V): $A_V = \frac{V_c}{V_e}$

But, $V_c = -i_c Z_L$ and $V_e = i_e Z_I$

$$A_V = \frac{-i_c Z_L}{i_e Z_I} \qquad \frac{-i_c}{i_e} = A_I$$

$$\therefore A_V = \frac{A_I Z_L}{Z_I} \qquad \text{..... (4)}$$

Step 5:

Output Impedance (Z_0): $Y_0 = \frac{i_c}{V_c}$ at $V_e=0$

We have, $i_c = h_{fb} i_e + h_{ob} V_c$

$$\Rightarrow \frac{i_c}{V_c} = h_{ob} + h_{fb} \frac{i_e}{V_c}$$

We have, $V_e = h_{ib} i_e + h_{rb} V_c \qquad \Rightarrow 0 = h_{ib} i_e + h_{rb} V_c$

$$\Rightarrow \frac{i_e}{V_c} = \frac{-h_{rb}}{h_{ib}}$$

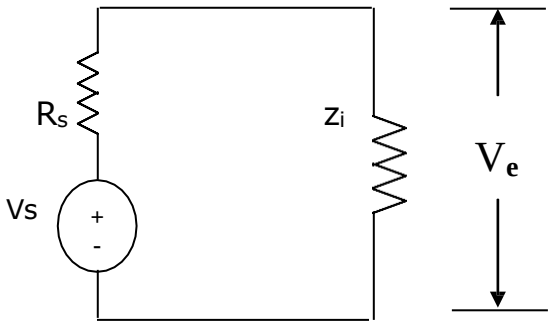
$$\therefore \frac{i_e}{V_c} = h_{ob} - \frac{h_{fb} h_{rb}}{h_{ib}}$$

$$\therefore Y_0 = h_{ob} - \frac{h_{fb} h_{rb}}{h_{ib}}$$

$$\therefore Z_0 = \frac{h_{ib}}{h_{ob} h_{ib} - h_{fb} h_{rb}} \qquad \text{..... (5)}$$

Step 6:

Voltage gain with source resistance (A_{VS}):



$$A_{VS} = \frac{V_0}{V_s} = \frac{V_c}{V_e} \cdot \frac{V_e}{V_s}$$

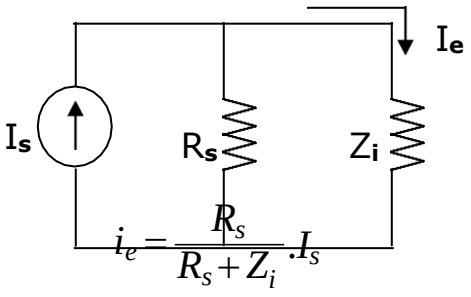
$$V_e = \frac{Z_i}{Z_i + R_s} . V_s$$

$$\frac{V_e}{V_s} = \frac{Z_i}{Z_i + R_s}$$

$$A_{VS} = A_V \cdot \frac{Z_i}{Z_i + R_s} \quad \text{..... (6)}$$

Step 7:

Current gain with source resistance (A_{IS});



$$A_{IS} = \frac{I_0}{I_s} = \frac{-i_c}{i_e} \cdot \frac{i_e}{I_s}$$

$$\frac{i_e}{i_s} = \frac{R_s}{R_s + Z_i}$$

$$A_{IS} = A_I \cdot \frac{R_s}{Z_i + R_s} \quad \text{..... (7)}$$

Step 8:

Input impedance with source resistance (Z_{is}):

$$Z_{is} = Z_i + R_s$$

$$Z_{is} = h_{ib} + R_s + h_{rb} A_I Z_L \quad \text{..... (8)}$$

Step 9:

Output impedance with source resistance (Z_{os}):

$$Y_0 = h_{ob} - \frac{h_{fb} h_{rb}}{h_{ib}}$$

$$\therefore Y_{os} = h_{ob} - \frac{h_{fb} h_{rb}}{h_{ib} + R_s} \quad \text{..... (9)}$$

$$Z_{os} = \frac{1}{Y_{os}}$$

Analysis of CC amplifier using h-parameter model

Circuit diagram:

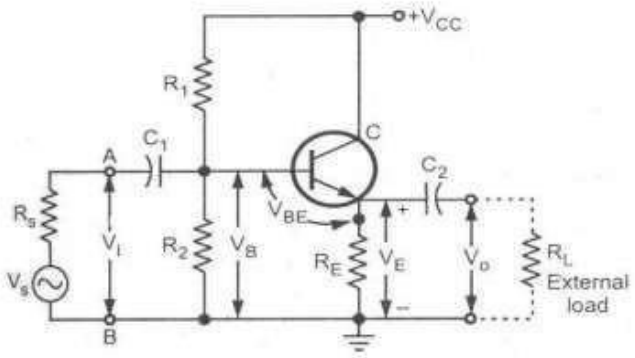
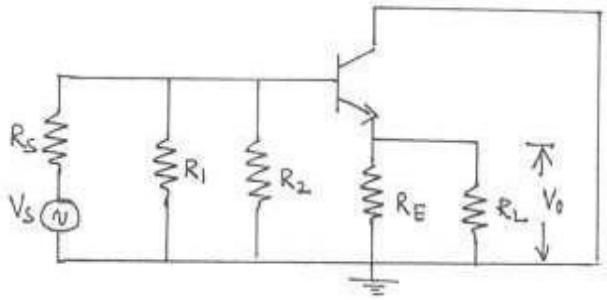


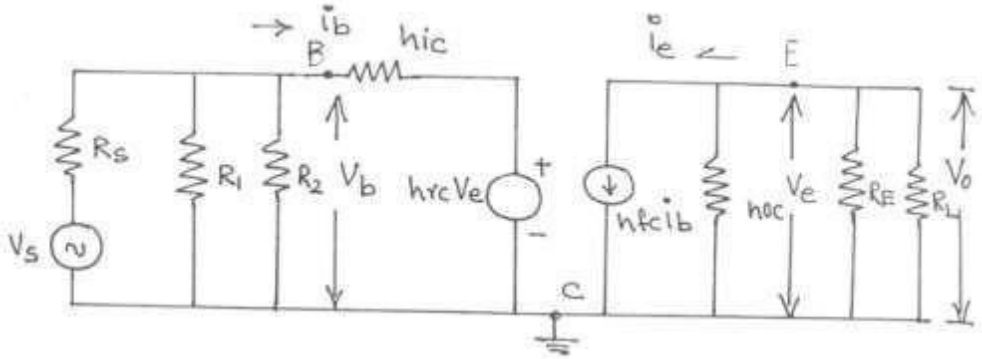
Figure .11 Common Collector Amplifiers

AC equivalent circuit:

1) Vcc=0 ii) Xc=0



h-parameter model:



Step 1:

Load impedance (Z_L): $Z_L = R_E \,||\, R_L$ .....(1)

Step 2 :

Current Gain (A_I): $A_I = \dfrac{-i_e}{i_b}$

We have, $i_e = h_{fc} i_b + h_{oc} V_e$

But, $V_e = -i_e Z_L$

$$i_e = h_{fc} i_b + h_{oc}(-i_e) Z_L$$

$$i_e(1 + h_{oc} Z_L) = h_{fc} i_b$$

$$\frac{i_e}{i_b} = \frac{h_{fc}}{1 + h_{oc} Z_L}$$

$$\therefore A_I = -\frac{h_{fc}}{1 + h_{oc} Z_L} \quad \text{..... (2)}$$

Step 3:

Input Impedance (Z_i): $Z_i = \frac{V_b}{i_b}$

We have, $V_b = h_{ic} i_b + h_{rc} V_e$

$\frac{V_b}{i_b} = h_{ic} + h_{rc} \frac{V_e}{i_b}$

But, $V_e = -i_e Z_L$

$\therefore \frac{V_b}{i_b} = h_{ic} + h_{rc} \frac{-i_e Z_L}{i_b}$

$\therefore Z_i = h_{ic} + h_{rc} A_I Z_L$ ..... (3) $\quad \frac{-i_e}{i_b} = A_I$

Step 4:

Voltage Gain (A_V): $A_V = \frac{V_e}{V_b}$

But, $V_e = -i_e Z_L$ and $V_b = i_b Z_I$

$A_V = \frac{-i_e Z_L}{i_b Z_I}$ $\quad \frac{-i_e}{i_b} = A_I$ $\quad \therefore A_V = \frac{A_I Z_L}{Z_I}$ ..... (4)

Step 5:

Output Impedance (Z_0): $Y_0 = \frac{i_e}{V_e}$ at $V_b = 0$

We have, $i_e = h_{fc} i_b + h_{oc} V_e$

$\Rightarrow \frac{i_e}{V_e} = h_{oc} + h_{fc} \frac{i_b}{V_e}$

We have, $V_b = h_{ic} i_b + h_{rc} V_e$

$\Rightarrow 0 = h_{ic} i_b + h_{rc} V_e$

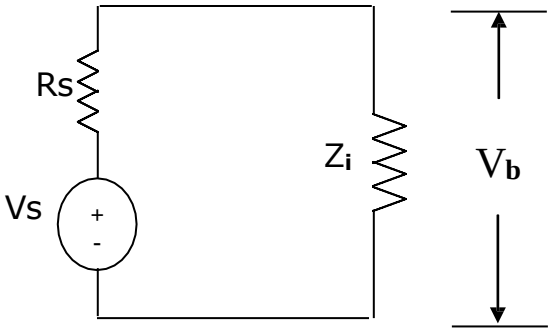
$\Rightarrow \frac{i_b}{V_e} = \frac{-h_{rc}}{h_{ic}}$

$\therefore \frac{i_e}{V_e} = h_{oc} - \frac{h_{fc} h_{rc}}{h_{ic}}$ $\quad \therefore Y_0 = h_{oc} - \frac{h_{fc} h_{rc}}{h_{ic}}$

$Z_0 = \frac{1}{Y_0}$ $\quad \therefore Z_0 = \frac{h_{ic}}{h_{oc} h_{ic} - h_{fc} h_{rc}}$ ..... (5)

Step 6:

Voltage gain with source resistance (A_{VS}):



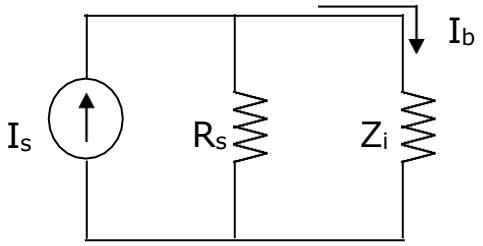
$$A_{VS} = \frac{V_0}{V_s} = \frac{V_c}{V_b} \cdot \frac{V_b}{V_s} = A_V \cdot \frac{V_b}{V_S}$$

$$V_b = \frac{Z_i}{Z_i + R_s} . V_s$$

$$\frac{V_b}{V_s} = \frac{Z_i}{Z_i + R_s} \qquad A_{VS} = A_V \cdot \frac{Z_i}{Z_i + R_s} \qquad \text{.....(6)}$$

Step 7:

Current gain with source resistance (A_{IS});



$$A_{IS} = \frac{I_0}{I_s} = \frac{-i_e}{i_b} \cdot \frac{i_b}{I_s} = A_I \cdot \frac{i_b}{i_S}$$

$$i_b = \frac{R_s}{R_s + Z_i} . i_s \qquad \frac{i_b}{i_s} = \frac{R_s}{R_s + Z_i}$$

$$\therefore A_{IS} = A_I \cdot \frac{R_s}{R_s + Z_i} \qquad \text{..... (7)}$$

Step 8:

Input impedance with source resistance (Z_{is}):

$$Z_{is} = Z_i + R_s$$

$$Z_{is} = h_{ic} + R_s + h_{rc} A_I Z_L \qquad \text{..... (8)}$$

Step 9:

Output impedance with source resistance (Z_{OS}):

$$Y_0 = h_{oc} - \frac{h_{fc} h_{rc}}{h_{ic}}$$

$$Z_o = \frac{1}{Y_o}$$

$$\therefore Y_{os} = h_{oc} - \frac{h_{fc}h_{rc}}{h_{ic} + R_s} \quad \text{..... (9)}$$

$$Z_{os} = \frac{1}{Y_{os}}$$

Simplified CE hybrid model:

We have calculated current gain, voltage gain, input impedance and output impedance in different configurations of a transistor using h-parameters.

However, in most of the practical circuits, we may use simplified hybrid model. Such an approximate model is justified because h-parameters themselves are not steady but vary considerably for the same type of transistor since CE configuration is the most widely used, it is taken for consideration.
Figure below shows the exact CE h-parameter model.

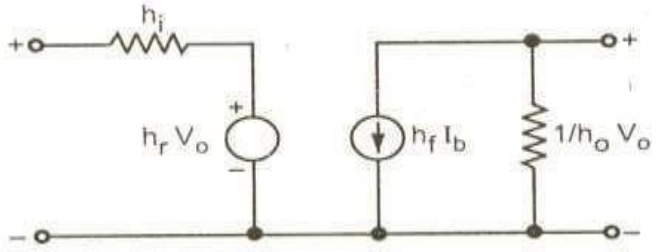


Figure 12. Exact CE hybrid model

Now we proceed to find simplified approximate and accurate version of this model. It is obvious from the figure that resistance (1/hoe) appears in parallel with the load resistance R_L. (1/hoe) is often large enough to be ignored in comparison to a parallel load. On having omitted hoe, the collector current is given by $i_C = h_{fe}i_b$. Further $V_C = i_C R_L = h_{fe}i_b R_L$. Accordingly the magnitude of the voltage of generator in the emitter circuit also gets modified. This is given by $h_{re}|V_c| = h_{re}h_{fe}i_b R_L$. Since $h_{re}h_{fe} \approx 0.01$, this voltage may be neglected in comparison with the voltage drop across $h_{ie} = h_{ie}i_b$ provided that R_L is not too large.Thus it is possible to neglect the parameters hoe and hre in approximate CE h-model and use remaining two other h-parameters. Figure shows the simplified approximate CE hybrid model.

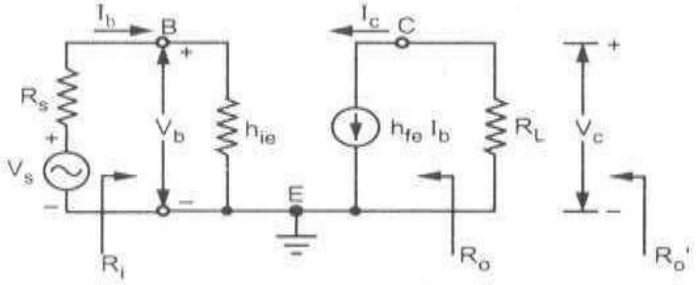


Figure 13. Approximate CE hybrid model.

Generalized Approximate Model

The approximate CE h-parameters model is redrawn as shown in fig. below. This is known as generalized approximate model.

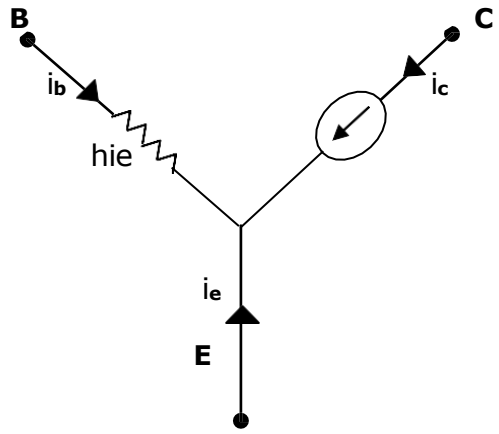


Figure 14. Approximate hybrid model valid for all configurations.

This model can be used for any configuration by simply grounding the appropriate terminal. The signal is always applied between the input terminal and ground while the load impedance is connected between output terminal and the ground.

The generalized approximate model for common base circuit is as shown below.

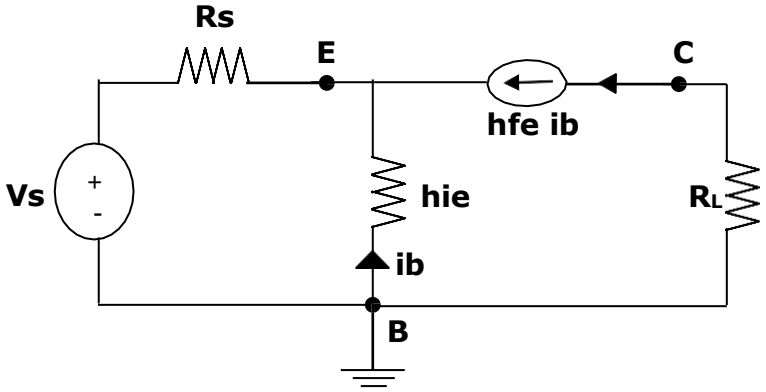
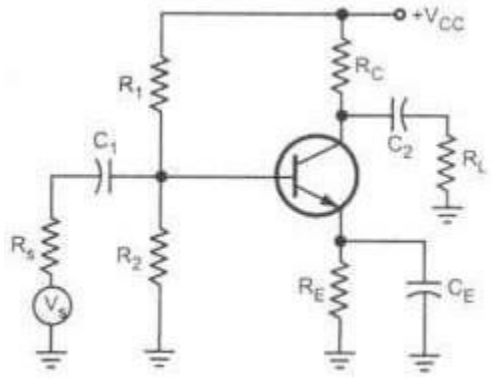


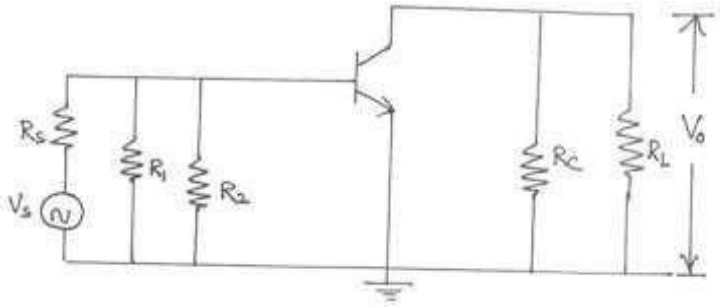
Fig 15. CB generalized approximate model

Analysis of CE amplifier using approximate model:

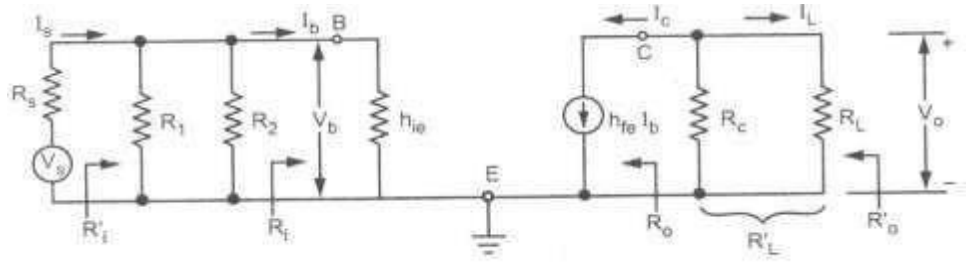
Circuit diagram:



AC equivalent circuit:



Approximate hybrid model:



Step 1:

Load impedance (Z_L):

$$Z_L = R_C \,||\, R_L \quad \text{..... (1)}$$

Step 2 :

Current Gain (A_I): $A_I = \dfrac{-i_c}{i_b}$

We have, $i_c = h_{fe} i_b$

$$\frac{i_c}{i_b} = h_{fe}$$

$$\therefore A_I = -h_{fe} \quad \text{..... (2)}$$

Step 3:

Input Impedance (Z_i): $Z_i = \dfrac{V_b}{i_b}$

We have, $V_b = h_{ie} i_b$

$$\frac{V_b}{i_b} = h_{ie}$$

$$\therefore Z_i = h_{ie} \quad \text{..... (3)}$$

Step 4:

Voltage Gain (A_V): $A_V = \dfrac{V_c}{V_b}$

But, $V_c = -i_c Z_L = -h_{fe} i_b Z_L$ and $V_b = i_b Z_I$

$$A_V = \frac{-h_{fe} i_b Z_L}{i_b Z_I}$$

$$A_V = \frac{-h_{fe} Z_L}{Z_i}$$

But, $Z_i = h_{ie}$

$$\therefore A_V = \frac{-h_{fe} Z_L}{h_{ie}} \quad \text{..... (4)}$$

Step 5:

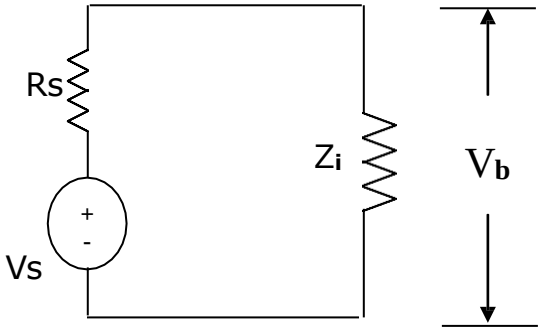
Output Impedance (Z_0): $Y_0 = \frac{i_c}{V_c}$ at $V_b=0$

With $V_b=0$, $i_b=0$ and $i_e=0$

$\therefore$ $i_c=0$ Therefore, $Y_0=0$ $\mathbf{Z_0=\infty}$ ..... (5)

Step 6:

Voltage gain with source resistance (A_{VS}):

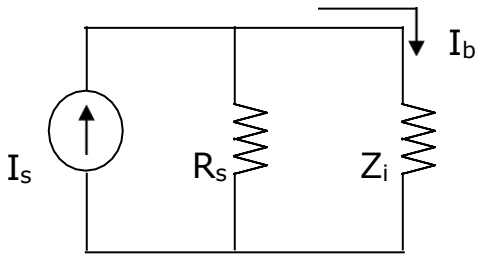


$$A_{VS} = A_V \cdot \frac{Z_i}{Z_i + R_s}$$

$$\Rightarrow A_{VS} = A_V \cdot \frac{h_{ie}}{h_{ie} + R_s} \quad \text{..... (6)}$$

Step 7:

Current gain with source resistance (A_{IS});



$$A_{IS} = A_I \cdot \frac{R_s}{R_s + Z_i}$$

$$\Rightarrow A_{IS} = A_I \cdot \frac{R_s}{R_s + h_{ie}} \quad \text{..... (7)}$$

Step 8:

Input impedance with source resistance (Z_{is}):

$$Z_{is} = Z_i + R_s \qquad \Rightarrow Z_{is} = h_{ie} + R_s \qquad \text{..... (8)}$$

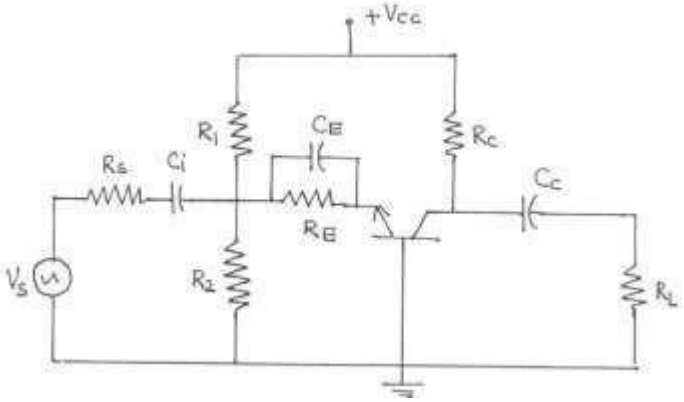
Step 9:

Output impedance with source resistance (Z_{os}):

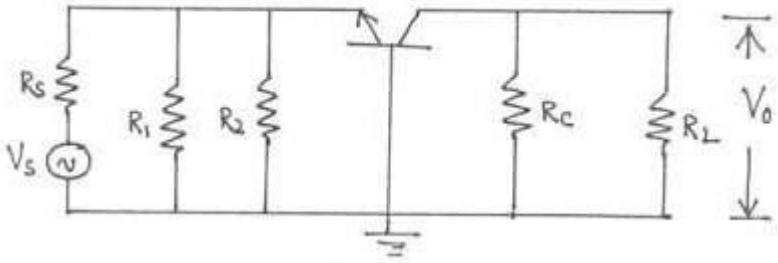
$$\therefore Z_{os} = \infty \text{.....(9)}$$

Analysis of CB amplifier using approximate model

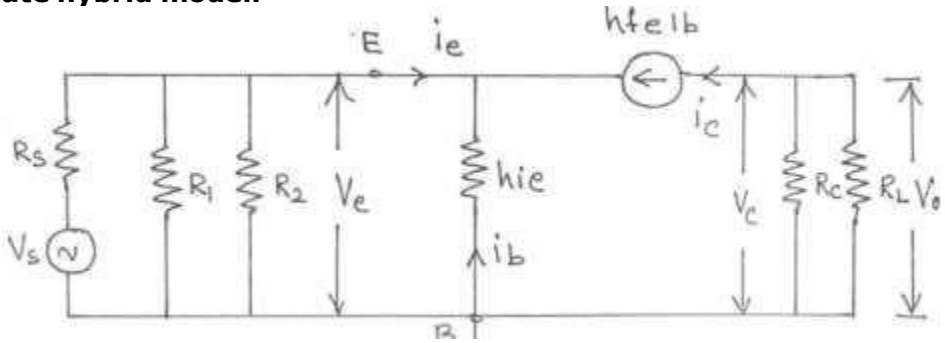
Circuit diagram:



AC equivalent circuit:



Approximate hybrid model:



Step 1:

Load impedance (Z_L):

$$Z_L = R_C \| R_L \qquad \text{..... (1)}$$

Step 2 :

Current Gain (A_I): $A_I = \frac{-i_c}{i_e}$

We have, $i_c = h_{fe} i_b$

From figure, $i_e + i_b + h_{fe} i_b = 0$ $\quad i_e = -i_b(1+h_{fe})$

$$\therefore A_I = \frac{-h_{fe} i_b}{-i_b (1+h_{fe})}$$

$$\therefore A_I = \frac{h_{fe}}{(1+h_{fe})} \quad \text{..... (2)}$$

Step 3:

Input Impedance (Z_i): $Z_i = \frac{V_e}{i_e}$

We have, $V_e = -h_{ie} i_b$ and $i_e = -i_b(1+h_{fe})$

$$\therefore Z_i = \frac{-h_{ie} i_b}{-i_b(1+h_{fe})}$$

$$\therefore Z_i = \frac{h_{ie}}{(1+h_{fe})} \quad \text{..... (3)}$$

Step 4:

Voltage Gain (A_V): $A_V = \frac{V_c}{V_e}$

But, $V_c = -h_{fe} i_b Z_L$ and $V_e = -h_{ie} i_b$

$$A_V = \frac{-h_{fe} i_b Z_L}{-h_{ie} i_b}$$

$$\therefore A_V = \frac{h_{fe} Z_L}{h_{ie}} \quad \text{..... (4)}$$

Step 5:

Output Impedance (Z_0): $Y_0 = \frac{i_C}{V_c}$ at $V_e = 0$

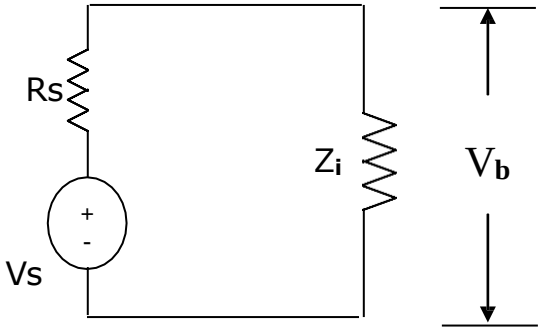
With $V_e = 0$, $i_e = 0$ and $i_b = 0$

$\therefore i_c = 0$ Therefore, $Y_0 = 0$

$Z_0=\infty$ ..... (5)

Step 6:

Voltage gain with source resistance (A_{VS}):

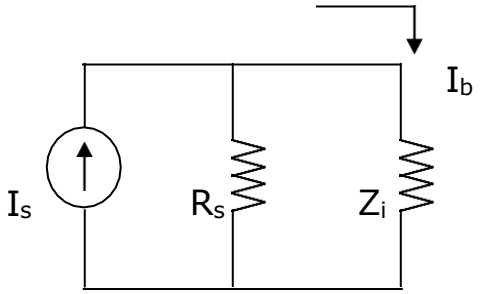


$$A_{VS} = A_V \cdot \frac{Z_i}{Z_i + R_s}$$

$$\Rightarrow A_{VS} = \frac{h_{fe} Z_L}{h_{ie} + \left(1 + h_{fe}\right) R_S} \quad \text{..... (6)}$$

Step 7:

Current gain with source resistance (A_{IS});



$$A_{IS} = A_I \cdot \frac{R_S}{R_s + Z_i}$$

$$\Rightarrow A_{IS} = \frac{h_{fe} R_S}{h_{ie} + \left(1 + h_{fe}\right) R_S} \quad \text{..... (7)}$$

Step 8:

Input impedance with source resistance (Z_{is}):

$$Z_{is} = Z_i + R_s$$

$$\Rightarrow Z_{is} = \frac{h_{ie} + R_s\left(1 + h_{fe}\right)}{\left(1 + h_{fe}\right)} \quad \text{..... (8)}$$

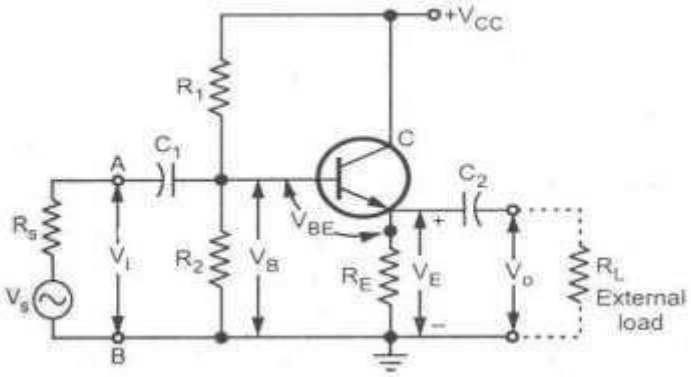
Step 9:

Output impedance with source resistance (Z_{os}):

$$\therefore Z_{os} = \infty \quad \text{.....(9)}$$

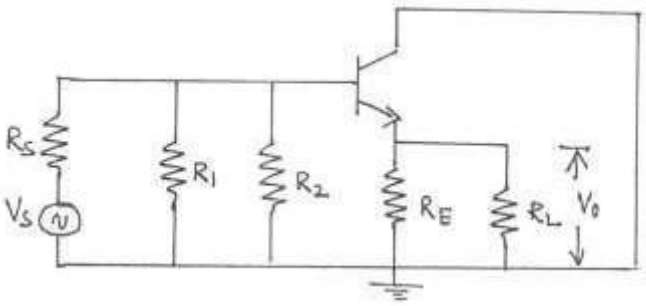
Analysis of CC amplifier using approximate model

Circuit diagram:

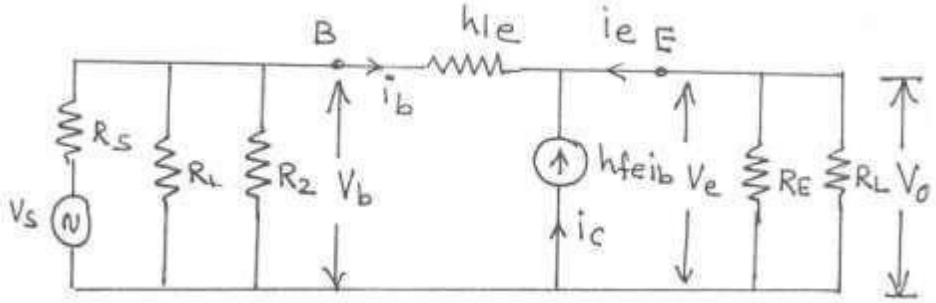


AC equivalent circuit:

i) Vcc=0 ii) Xc=0



Approximate hybrid model:



Step 1:

Load impedance (Z_L): $Z_L = R_E \,||\, R_L$ ..... (1)

Step 2 :

Current Gain (A_I): $A_I = \dfrac{-i_e}{i_b}$

From circuit,

$$i_e + i_b + h_{fe} i_b = 0$$

$$\Rightarrow i_e + i_b\left(1 + h_{fe}\right) = 0$$

$$\Rightarrow \frac{-i_e}{i_b} = 1 + h_{fe}$$

$$\therefore A_I = 1 + h_{fe} \quad \text{..... (2)}$$

Step 3:

Input Impedance (Z_i): $Z_i = \dfrac{V_b}{i_b}$

From circuit, $V_b = h_{ie} i_b + V_e$ and $V_e = -i_e Z_L$

$$\therefore V_b = h_{ie} i_b - i_e Z_L$$

$$\Rightarrow V_b = h_{ie} i_b + \left(1 + h_{fe}\right) i_b Z_L$$

$$\Rightarrow \frac{V_b}{i_b} = h_{ie} + \left(1 + h_{fe}\right) Z_L$$

$$\Rightarrow Z_i = h_{ie} + \left(1 + h_{fe}\right) Z_L \quad \text{..... (3)}$$

Step 4:

Voltage Gain (A_V):

$$A_V = \frac{V_e}{V_b}$$

From circuit, $V_e = -i_e Z_L$ and $V_b = i_b\left(h_{ie} + \left(1 + h_{fe}\right)Z_L\right)$

$$A_V = \frac{-i_e Z_L}{i_b Z_i} \qquad \therefore A_V = \frac{A_I Z_L}{Z_i}$$

$$\therefore A_V = \frac{\left(1 + h_{fe}\right)Z_L}{h_{ie} + \left(1 + h_{fe}\right)Z_L} \quad \textbf{(or)} \quad \therefore A_V = 1 - \frac{h_{ie}}{Z_i} \quad \text{..... (4)}$$

Step 5:

Output Impedance (Z_0):

$$Y_0 = \frac{i_e}{V_e} \text{ at } V_b = 0$$

We have, $V_b = h_{ie} i_b + V_e$

$$\Rightarrow 0 = h_{ie} i_b + V_e$$

$$V_e = -h_{ie} i_b$$

But $$i_e = -i_b\left(1+h_{fe}\right)$$

$$\therefore Y_0 = \frac{1+h_{fe}}{h_{ie}}$$

$$\therefore Z_0 = \frac{h_{ie}}{1+h_{fe}} \quad \text{..... (5)}$$

Comparison of Transistor Amplifier configurations

The characteristics of three configurations are summarized for the quantities **A_i,A_V,R_i,Ro** and **Ap** calculated fir typical h-parameters by taking the values of **R_L** and **Rs** are as 3KΩ.

Quantity	CB	CC	CE
A_i	0.98	47.15	-46.5
A_V	131	0.989	-131
Ap	128.38	46.98	6091.5
R_i	22.6Ω	144KΩ	1065Ω
Ro	1.72MΩ	80.5Ω	45.5KΩ

Characteristics of CB Amplifier:

i) Current gain of less than unity.

ii) High voltage gain.

iii) Power gain approximately equal to voltage gain.

iv) No phase shift for current (or) voltage.

v) Small input impedance.

iv) Large output impedance.

Applications:

The CB amplifier is not commonly used for amplification purpose. It is used for.

1) Matching a very low impedance source.
2) As a non-inverting amplifier with voltage gain exceeding unity.
3) For driving a high impedance load.
4) As a constant current source.

Characteristics of CC Amplifier:

1) High current gain.
2) Voltage gain of approximately unity.

3) Power gain approximately equal to current gain.
4) No current (or) voltage phase shift.
5) Large input impedance.
6) Small output impedance.

Applications:

The CC amplifier is widely used as a buffer stage between a high impedance source and a low impedance load. The CC amplifier is called the emitter follower.

Characteristics of CE amplifier:

1) Large current gain.
2) Large voltage gain.
3) Large power gain.
4) Voltage phase shift of 180^0.
5) Moderate input impedance.
6) Moderate output impedance.

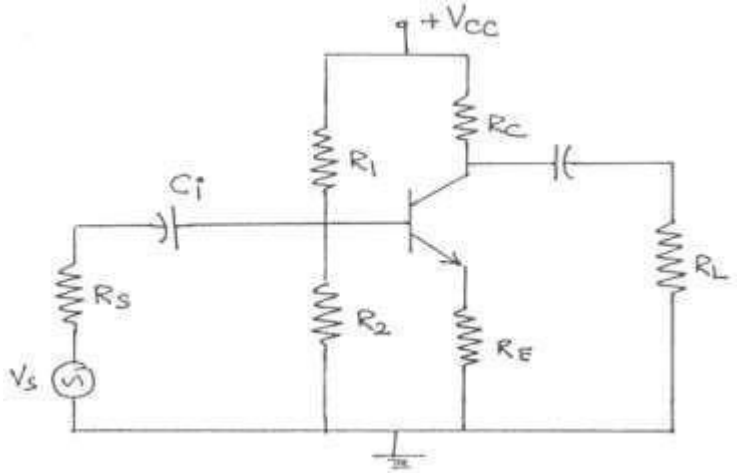
Applications:

Of the three configurations CE amplifier alone is capable of providing both voltage gain and current gain. The input resistance $\mathbf{R_i}$ and the output resistance **Ro** are moderately high.

Hence the CE amplifier is widely used for amplification purpose.

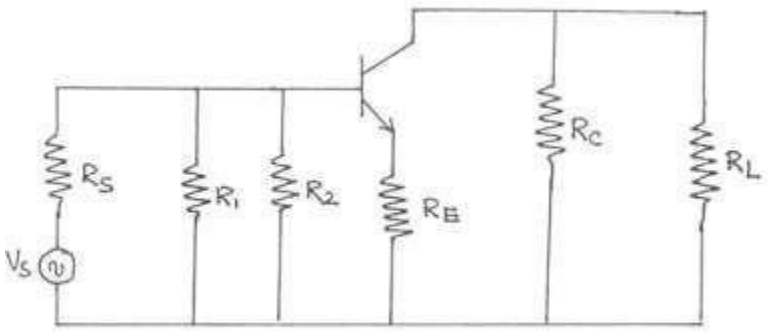
Common Emitter Amplifier with Emitter Resistor is un bypassed by a Capacitor (C_E):

Circuit diagram:

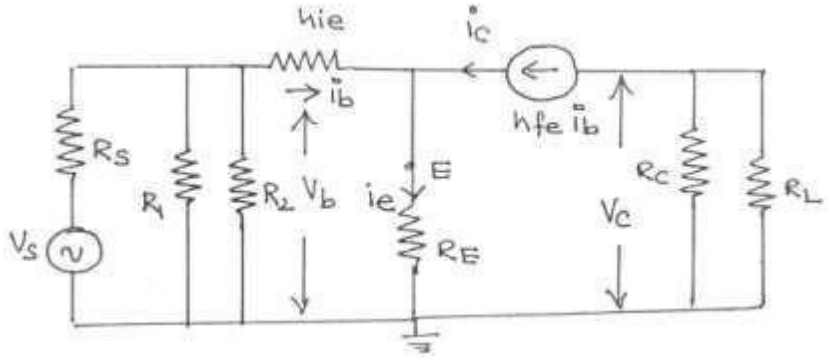


AC Equivalent circuit:

1) Vcc=0 ii) Xc=o



h-parameter model:



Step 1:

Load impedance (Z_L): $Z_L = R_C \| R_L$ ..... (1)

Step 2:

Current Gain (A_I): $A_I = \dfrac{-i_c}{i_b}$

We have, $i_c = h_{fe} i_b$ $\qquad \dfrac{i_c}{i_b} = h_{fe}$

$\therefore A_I = -h_{fe}$ ..... (2)

Step 3:

Input Impedance (Z_i): $Z_i = \dfrac{V_b}{i_b}$

From the circuit, $V_b = h_{ie} i_b + i_e R_E$

$i_e = \left(1 + h_{fe}\right) i_b$

$V_b = h_{ie} i_b + \left(1 + h_{fe}\right) i_b R_E$

$\dfrac{V_b}{i_b} = \left(h_{ie} + \left(1 + h_{fe}\right) R_E\right)$ $\qquad \therefore Z_i = h_{ie} + (1 + h_{fe}) R_E$ ..... (3)

Step 4:

Voltage Gain (A_V): $$A_V = \frac{V_c}{V_b}$$

But, $$V_c = -i_c Z_L = -h_{fe} i_b Z_L$$

Dividing with $\mathbf{V_b}$ on both sides of the above equation

$$\frac{V_C}{V_b} = \frac{-h_{fe} i_b Z_L}{V_b} = \frac{-h_{fe} Z_L}{\frac{V_b}{i_b}}$$

$$A_V = \frac{-h_{fe} Z_L}{Z_I} \qquad \therefore A_V = \frac{-h_{fe} Z_L}{h_{ie} + \left(1 + h_{fe}\right) R_E} \qquad \text{..... (4)}$$

Step 5:

Output Impedance (Z_0): $$Y_0 = \frac{i_c}{V_c} \quad \text{at } V_b = 0$$

$$i_c = -h_{fe} i_b$$

$$V_b = h_{ie} i_b + (1 + h_{fe}) R_E i_b$$

If $V_b = 0 \Rightarrow i_b = 0$

$\therefore i_c = 0$

Therefore, $Y_0 = 0$ $\mathbf{Z_0 = \infty}$ ..... (5)

UNIT - IV

TRANSISTOR BIASING AND STABIIZATION

Introduction:

The basic function transistor is to do amplification. The process of raising the strength of a weak signal without any change in its shape is known as faithful amplification.

For faithful amplification, the following three conditions must be satisfied:

- The emitter-base junction should be forward biased,
- The collector-base junction should be reverse biased.
- Three should be proper zero signal collector current.

The proper flow of zero signal collector current (proper operating point of a transistor) and the maintenance of proper collector-emitter voltage during the passage of signal is known as 'transistor biasing'.

When a transistor is not properly biased, it work inefficiently and produces distortion in the output signal. Hence a transistor is to be biased correctly. A transistor is biased either with the help of battery (or) associating a circuit with the transistor. The latter method is generally employed. The circuit used with the transistor is known as biasing circuit.

In order to produce distortion-free output in amplifier circuits, the supply voltages and resistances in the circuit must be suitably chose. These voltages and resistances establish a set of d.c. voltage VCEQ and current ICQ to operate the transistor in the active region. These voltages and currents are called quiescent values which determine the operating point (or) Q-Point for the transistor.

The process of giving proper supply voltages and resistances for obtaining the desired Q-Point is called biasing.

Operating Point (or) Quiescent Point:

In designing a circuit, a point on the load line is selected as the dc bias point (or) quiescent point. The Q-Point specifies the collector current IC and collector to emitter voltage VCE that exists when no input signal is applied.

The dc bias point (or) quiescent point is the point on the load line which represents the current in a transistor and the voltage across it when no signal is applied. The zero signal values of IC ad VCE are known as the operating point.

How to choose the operating point on DC load line:

The transistor acts as an amplifier when it is operated in active region. After the d.c. conditions are established in the circuit, when an a.c. signal is applied to the input, the base current varies according to the amplitude of the signal and causes IC to vary consequently producing an output voltage variation. This can be seen from output characterizes

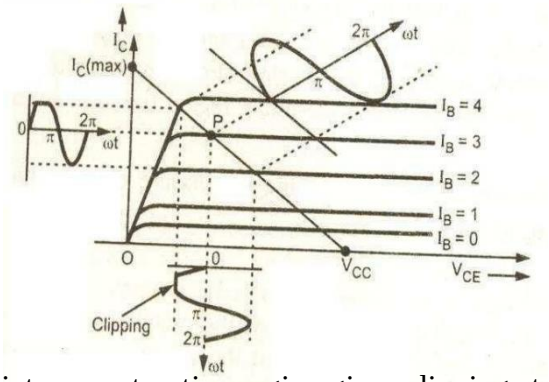


Fig. Operating point near saturation region gives clipping at the positive peak

Consider point A which is very near to the saturation point, even though the base current is varying sinusoid ally the output current and output voltage is seen to be clipped at the positive peaks. This results in distortion of the signal.

Consider point B which is very near to the cut-off region. The output signal is now clipped at the negative peak. Hence this two is not a suitable operating point.

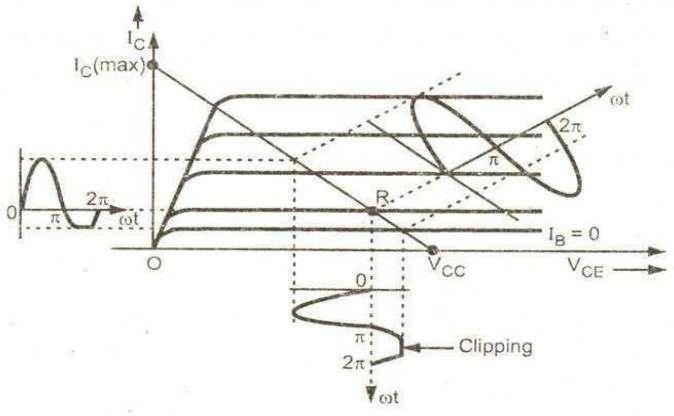


Fig. Operating point near cut-off region given clipping at the negative peak

Consider point C which is the mid-point of the DC load line then the output signal will not be distorted.

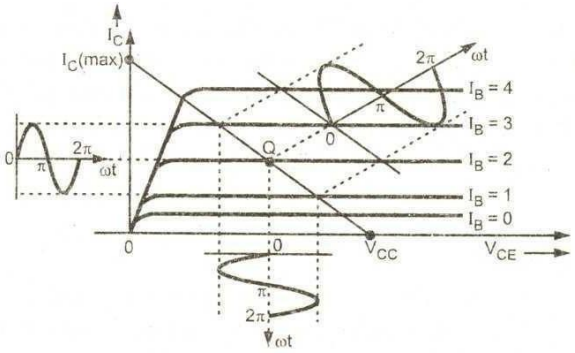
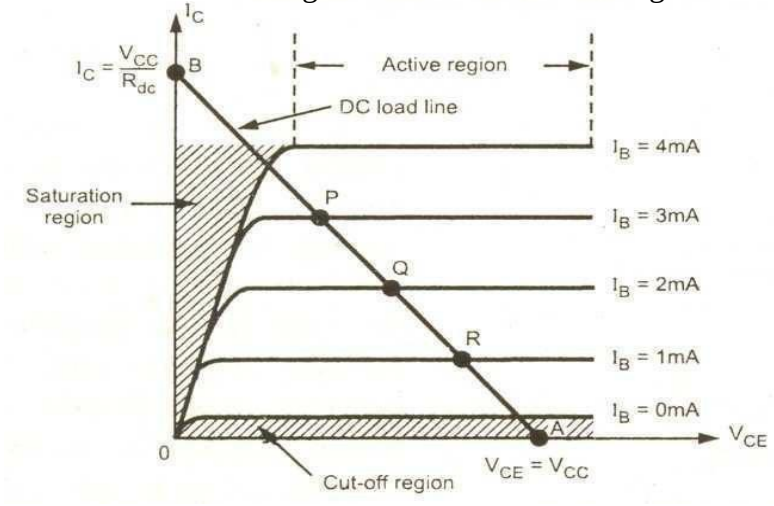


Fig. Operating point at the centre of active region is most suitable.

A good amplifier amplifies signals without introducing distortion. Thus always the operating point is chosen as the mid-point of the DC load line.

DC Load Line:

Consider common emitter configuration circuit shown in figure below:



In transistor circuit analysis generally it is required to determine the value of IC for any desired value of VCE. From the load line method, we can determine the value of IC for any desired value of VCE. The output characteristics of CE configuration is shown in figure below

By applying KVL to the collector circuit

$$V_{CE} + I_C R_C - V_{CC} = 0$$

$$V_{CE} + I_C R_C = V_{CC}$$

If the bias voltage VBB is such that the transistor is not conducting then IC=0 and VCE= VCC. Therefore, when IC=0, VCE= VCC this point is plotted on the output characteristics as point A.

Biasing:

The process of giving proper supply voltages and resistances for obtaining the desired Q-point is called 'biasing'.

Stabilization:

The maintenance of operating point stable is known as '*STABILIZATION'.*

There are two factors which are responsible for shifting the operating point. They are:

- The transistor parameters are temperature dependent.
- When a transistor is replaced by another of same type, there is a wide spread in the values of transistor parameters.

So, stabilization of the operating point is necessary due to the following reasons:

- Temperature dependence of IC.
- Individual variations
- Thermal runaway.

Temperature dependence of IC:

The instability of IC is principally caused by the following three sources:

(i) The ICO doubles for every 10^oC rise in temperature.

(ii) Increase of β with increase of temperature.

(iii) The VBE decreases about 2.5mV per ^oC increase in temperature.

Individual variations:

When a transistor is replaced by another transistor of the same type, the values of β and VBE are not exactly the same. Hence the operating point is changed. So it is necessary to stabilize the operating point irrespective of individual variations in transistors parameters.

Thermal Runaway:

Depending upon the construction of a transistor, the collector junction can withstand maximum temperature. The range of temperature lies between 60^oC to 100^oC for 'Ge' transistor and 150^oC to 225^oC for 'Si' transistor. If the temperature increases beyond this range then the transistor burns out. The increase in the collector junction temperature is due to thermal runaway.

When a collector current flows in a transistor, it is heated i.e., its temperature increases. If no stabilization is done, the collector leakage current also increases. This further increases the transistor temperature. Consequently, there is a further increase in collector leakage current. The action becomes cumulative and the transistor may ultimately burn out. The self-destruction of an unstabilized transistor is known as thermal runaway.

The following two techniques are used for stabilization.

Stabilization techniques:

The technique consists in the use of a resistive biasing circuit which permits such a variation of base current IB as to maintain IC almost constant in spite of ICO, β and VBE.

Compensation techniques:

In this technique, temperature sensitive devices such as diodes, thermistors and sensistors etc., are used. Such devices produce compensating voltages and current in such a way that the operating points maintained stable.

Stability factors:

The rise of temperature results in increase in the value of transistor gain β and the leakage current Ico. So, I_C also increases which results in a shift in operating point. Therefore, The biasing network should be provided with thermal stability. Maintenance of the operating point is specified by S, which indicates the degree of change in operating point due to change in temperature.

The extent to which I_C is stabilized with varying I_C is measured by a stability factor S

$$S = \frac{\partial I_C}{\partial I_{CO}} \approx \frac{dI_C}{dI_{CO}} \approx \frac{\Delta I_C}{\Delta I_{CO}}, \beta \text{ and } I_B \text{ constant}$$

For CE configuration $I_C = \beta I_B + (1+\beta) I_{CO}$

Differentiate the above equation w.r.t I_C , We get

$$1 = \beta \frac{dI_B}{dI_C} + (1+\beta) \frac{dI_{co}}{dI_c}$$

$$\therefore \left(1 - \beta \frac{dI_B}{dI_C}\right) = \frac{(\beta+1)}{S}$$

$$\therefore S = \frac{1+\beta}{1-\beta \frac{dI_B}{dI_C}}$$

S should be small to have better thermal stability.

Stability factor S' and S'':

S' is defined as the rate of change of I_C with V_{BE}, keeping I_C and V_{BE} constant.

$$S' = \frac{\partial I_c}{\partial V_{BE}}$$

S'' is defined as the rate of change of I_C with β, keeping I_{CO} and V_{BE} constant.

$$S'' = \frac{\partial I_c}{\partial \beta}$$

Methods of Biasing:

Some of the methods used for providing bias for a transistor are as follows:

1) Fixed bias (or) base resistor method.
2) Collector to base bias (or) biasing with feedback resistor.
3) Voltage divider bias.

1) Fixed bias (or) base resistor method:

A CE amplifier used fixed bias circuit is shown in figure below:

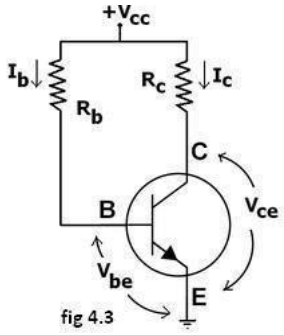


Fig. Fixed bias circuit

In this method, a high resistance R_B is connected between positive terminal of supply V_{CC} and base of the transistor. Here the required zero signal base current flows through R_B and is provided by V_{CC}.

In figure, the base-emitter junction is forward biased because the base is positive w.r.t. emitter. By a proper selection of R_B, the required zero signal base current (and hence $I_C=\beta I_B$) can be made to flow.

Circuit Analysis: Base Circuit:

Consider the base-emitter circuit loop of the above figure.

Writing KVL to the loop, we obtain

$-V_{CC}+I_BR_B+V_{BE}=0$

$V_{CC}= I_BR_B+V_{BE}$

$I_B= (V_{CC}- V_{BE}) / R_B$

BUT $IC = \beta I_B+I_{C\,EO}$

As I_{CEO} is very small, $IC = \beta I_B$

Therefore $I_C = \beta(V_{CC}-V_{BE}) / R_B$

$\Rightarrow \beta, V_{CC}, V_{BE}$ are constant for a transistor, therfore I_C depends on R_B.

Choose suitable value of R_B to get constant IC in active region.

Collector Circuit:

Consider the collector-emitter circuit loop of the circuit. Writing KVL to the collector circuit, we get

$V_{CC}= I_BR_B+V_{BE}$

STABILITY FACTOR S:

The stability factor s is given by

$$\mathbf{S=}(I+\beta) / (I-\beta)\partial I_B/\partial I_C$$

we have $I_B= (V_{CC}- V_{BE}) / R_B$ is constant therefore $\partial I_B=0$

therefore $S=(I+\beta)$

If $\beta=100$ then S=101. This shows that IC changes 101 times as much as any changes in ICO. Thus IC is dependent upon ICO and temperature.

The value of S is high and has very poor stability.

Stability factor S':

We have $IC=\beta I_B+I_{CO}$

But $I_B = (V_{CC} - V_{BE}) / R$

$I_C = \beta(V_{CC} - V_{BE}) / R_B + (I + \beta)I_{CO}$

Differentiating the above equation w.r.t. to I_C

We get $1 = -\beta \partial V_{BE} / \partial I_C$

$S' = -\beta / R_B$

Stability factor S'':

We have $IC = \beta I_B + I_{CO}$

Differentiating the above equation w.r.t. β

We get $\partial I_C / \beta = I_B + I_{CO}$ (I_{CO} is very small)

$S'' = I_B$

$S'' = IC / \beta$

Advantages of fixed bias circuit:

1. This is a simple circuit which uses very few components.
2. The operating point can be fixed anywhere in the active region of the characteristics by simply changing the values of RB. Thus, it provides maximum flexibility in the design.

Disadvantages of fixed bias circuit:

1. With the rise in temperature the operating point if not stable.
2. When the transistor is replaced by another with different value of β, the operating point with shift i.e., the stabilization of operating point is very poor in fixed bias circuit.

Because of these disadvantages, fixed bias circuit required some modifications. In the modified circuit, RB is connected between collector and base. Hence the circuit is called 'collector to base bias circuit.

2) Collector to Base bias (or) Biasing with feedback resistor:

A CE amplifier using collector to base bias circuit is shown in the figure. In this method,

the biasing resistor is connected between the collector and the base of the transistor.

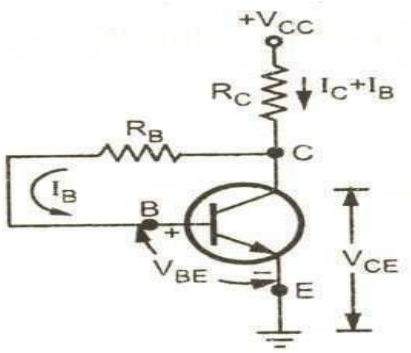


Fig. Collector–to–Base bias circuit.

Stability factor S':

$$\boldsymbol{IC} = \frac{\beta(\boldsymbol{V}_{CC} - \boldsymbol{V}_{BE} - \boldsymbol{I}_{C}\boldsymbol{R}_{C})}{\boldsymbol{R}_B + \boldsymbol{R}_C}$$

Differentiating the above equation w.r.t. IC we get

$$IC = \frac{-\beta V_{BE}}{R_B + R_C} - \beta\frac{R_C}{R_C + R_B}$$

$$1 + \beta\frac{R_C}{R_C + R_B} = \frac{-\beta V_{BE}}{R_B + R_C}$$

$$\frac{R_C + R_B + \beta R_C}{R_B + R_C} = \frac{-\beta V_{BE}}{R_B + R_C}$$

$$S' = \frac{-\beta}{R_B + (1+\beta)R_C}$$

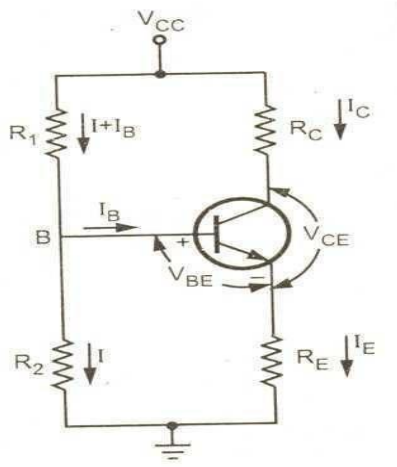
Stability factor S'':

we have

$$\boldsymbol{IC} = \frac{\beta(\boldsymbol{V}_{CC} - \boldsymbol{V}_{BE} - \boldsymbol{I}_{C}\boldsymbol{R}_{C})}{\boldsymbol{R}_B + \boldsymbol{R}_C}$$

3) Voltage Divider Bias (Or) Self-Bias (Or) Emitter Bias:

The voltage divider bias circuit is shown in figure.



In this method, the biasing is provided by three resistors R1, R2 and RE. The resistor R1 and R2 acts as a potential divider giving a fixed voltage to the base.

If collector current increases due to change in temperature (or) change in β, the emitter current IE also increases and the voltage drop across RE increases, reducing the voltage difference between base and emitter (VBE).

Due to reduction in VBE, base current IB and hence collector current IC is also reduces. Therefore, we can say that negative feedback exists in the emitter bias circuit. This reduction in collector current IC components for the original change in IC.

Circuit Analysis:

Let current flows through R1. As the base current IB is very small, the current flowing through R2 can also be taken as I

The calculation of collector current IC is as follows:

the current i flow through R1or R2 is $\boldsymbol{I = \frac{V_{CC}}{R1+R2}}$

the voltage v2 developed across rR2 is given by

$$V_2 = \frac{V_{CC}R_2}{R_1 + R_2}$$

Base Circuit:

Applying KVL to the base circuit, we have

$$v^{TH} = R^{TH}IB + V_{BE} + (I_B + I_C)$$

differentiating w.r. to I_C

$$\frac{\partial v^{TH}}{\partial I_C} = \frac{R^{TH}\partial I_B}{\partial I_C} + \frac{\partial V_{BE}}{\partial I_C} + \frac{\partial I_B}{\partial I_C}R_E + \frac{\partial I_C}{\partial I_C}R_E$$

$$0 = \frac{R^{TH}\partial I_B}{\partial I_C} + 0 + \frac{\partial I_B}{\partial I_C}R_E + R_E$$

$$= \frac{\partial I_B}{\partial I_C}(R_E + R^{TH}) + R_E$$

$$\frac{\partial I_B}{\partial I_C}(R_E + R^{TH}) = -R_E$$

$$\frac{\partial I_B}{\partial I_C} = -\frac{R_E}{(R_E + R^{TH})}$$

Substitute $\frac{\partial I_B}{\partial I_C}$ in the standard stability factor eq

$$s = \frac{1+\beta}{1-\beta(\frac{\partial I_B}{\partial I_C})}$$

$$S = \frac{1+\beta}{1-\beta\,(\frac{-R_E}{R_E + R^{TH}})}$$

$$S = \frac{1+\beta}{1+\beta\,(\frac{R_E}{R_E + R^{TH}})}$$

$$S = \frac{1+\beta(R_E + R^{TH})}{R_E + R^{TH} + \beta R_E}$$

$$= \frac{1+\beta(R_E + R^{TH})}{R^{TH} + R_E(1+\beta)}$$

Dividing each term by R_E

$$S = \frac{(1+\beta)R_E / R_E + (1+\beta)R^{TH} / R_E}{\frac{R^{TH}}{R_E} + (1+\beta)}$$

$$= \frac{(1+\beta)\,(1 + R^{TH}/R_E)}{(1+\beta) + R^{TH}/R_E}$$

If $R^{TH}/_{R_E} \ll 1$ we $neglect$ $R^{TH}/_{R_E}$

$$\frac{(1+\beta)}{(1+\beta)} = 1$$

Theoretically the stability factor value is '0' here the stability factor for voltage divider bias is almost equal to zero therefore this circuit provides more stability compared to all biasing techniques.

Bias Compensation Techniques:

The biasing circuits provide stability of operating point in case variations in the transistor parameters such as ICO, VBE and β.

The stabilization techniques refer to the use of resistive biasing circuits which permit IB to vary so as to keep IC relatively constant.

On the other hand, compensation techniques refer to the use of temperature sensitive devices such as diodes, transistors, thermistors, sensistors etc., to compensate for the variation in currents. Sometimes for excellent bias and thermal stabilization, both stabilization as well as compensation techniques are used.

The following are some compensation techniques:

1) Diode compensation for instability due to VBE variation.
2) Diode compensation for instability due to ICO variation.
3) Thermistor compensation.
4) Sensistor compensation.

1) Diode compensation for instability due to VBE variation:

For germanium transistor, changes in ICO with temperature contribute more serious problem than for silicon transistor.

On the other hand, in a silicon transistor, the changes of VBE with temperature possesses significantly to the changes in IC.

A diode may be used as compensation element for variation in VBE (or) ICO.

The figure below shows the circuit of self bias stabilization technique with a diode compensation for VBE. The Thevenin's equivalent circuit is shown in figure.

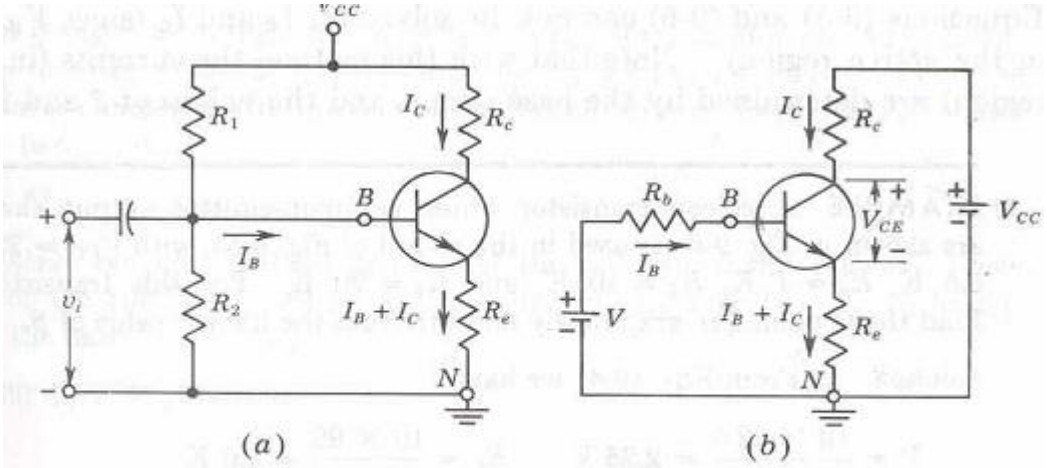


Fig. (a) A self-biasing circuit. (b) Simplification of the base circuit in (a) by the use of Thévenin's theorem.

The diode D used here is of the same material and type as the transistor. Hence the voltage VD across the diode has same temperature coefficient (-2.5mV/°C) as VBE of the transistor. The diode D is forward biased by the source V_{DD} and resistor R_D.

Applying KVL to the base circuit, we get

$$-V_{TH} + I_B R_{TH} + V_{BE} + I_E R_E - V_D = 0$$

we are solving the above equation becomes

$$I_C = \frac{\beta[V - (V_{BE} - V_D)] + (R_E + R_B)(1 + \beta)I_{C0}}{R_B + (1 + \beta)R_E}$$

When V_{BE} changes by ∂V_{BE} with change in temperature V_D changes by ∂V_D

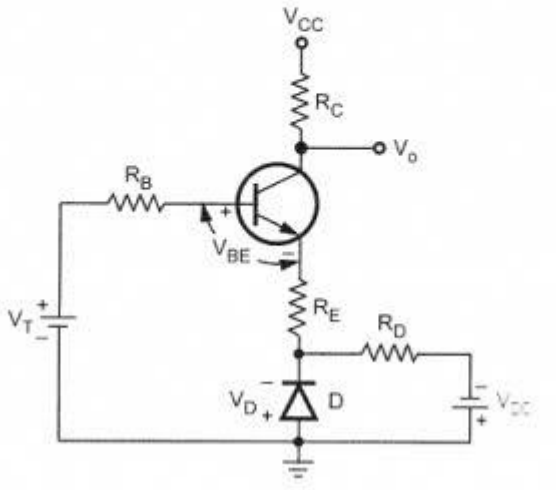
Diode compensation for instability due to ICO variation:

Consider the transistor amplifier circuit with diode D used for compensation of variation in ICO. The diode D and the transistor are of the same type and same material.

In this circuit diode is kept in reverse biased condition.

The reverse saturation current IO of the diode will increase with temperature at the same as the transistor collector saturation current I_{CO}.

$$\begin{aligned} V_T &= I_B R_B + V_{BE} + (I_B + I_C) R_E - V_D \\ &= I_B (R_B + R_E) + I_C R_E + V_{BE} - V_D \end{aligned}$$



From figure

$$I = \frac{V_{CC} - V_{BE}}{R_1}$$

$$I = \frac{V_{CC}}{R_1}$$

We know current equation

$$I_C = \beta I_B + (1 + \beta) I_{C0}$$

$$I_C = \beta(1 - I_0) + (1 + \beta) I_{C0}$$

$$= \beta I - \beta I_0 + I_{C0} + \beta I_{C0}$$

$$= \beta I - \beta I_0 + \beta I_{C0}$$

$$I_0 = I_{C0}$$

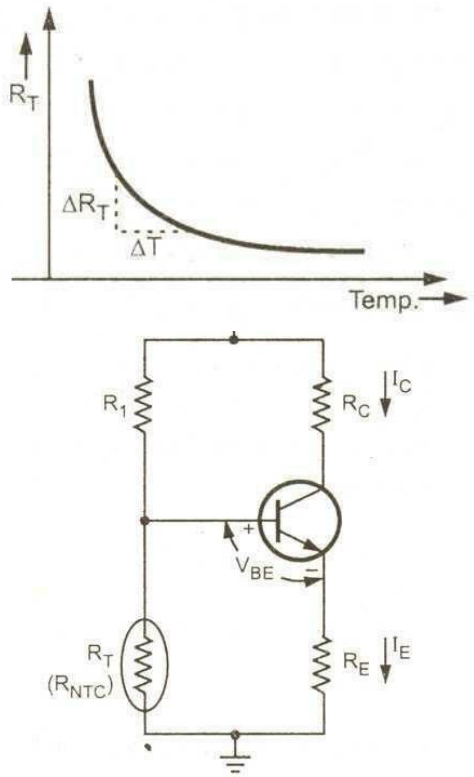
$$I_C = \beta I$$

In the above expression, I is almost constant and if IO of diode D and ICO of transistor track each other over the operating temperature range, then IC remains constant

Thermistor Compensation:

This method of transistor compensation uses temperature sensitive resistive elements, thermistor rather than diodes (or) transistors:

It has a negative temperature coefficient, its resistance decreases exponentially with increasing temperature as shown in the figure.



Slope of this curve is $\frac{\partial RT}{\partial T}$

The slope is negative. So we can say that thermistor has negative temperature coefficient of resistance. Figure below shows thermistor compensation technique. As shown in figure, R2 is replaced by thermistor RT in self bias circuit.

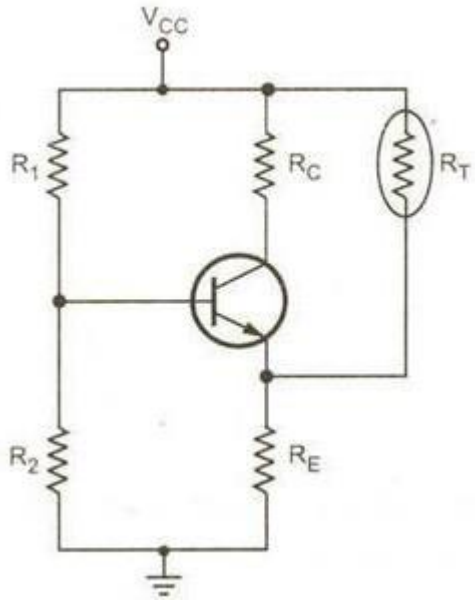
With increase in temperature, RT decreases. Hence voltage drop across it also decreases. This voltage drop is nothing but the voltage at the base with respect to ground. Hence, VBE decreases which reduces IB. This behavior will tend to offset the increase in collector current with temperature.

We know current equation

$$I_C = \beta I_B + (1 + \beta) I_{C0}$$

In this equation, there is increase in I_{CBO} and decreases in I_B which keeps I_C constant.

Consider another thermistor compensation technique shown in figure. Here, thermistor is connected between emitter and VCC to minimize the increase in collector current due to change in ICO, VBE (or) β with

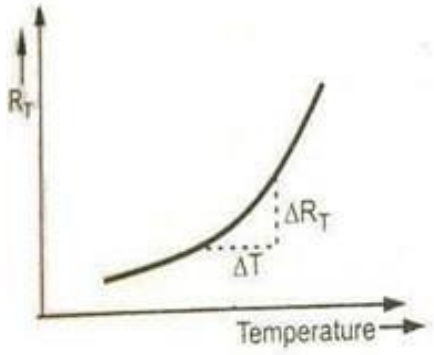


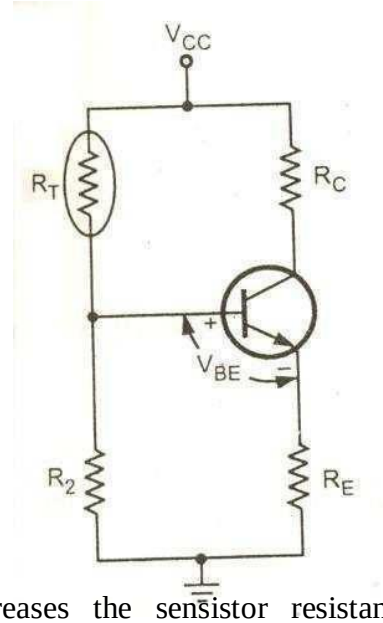
IC increase with temperature and RT decreases with increase in temperature. Therefore, current flowing through RE increases, which increases the voltage drop across it. Emitter to Base junction is forward biased. But due to increase in voltage drop across RE, emitter is made more positive, which reduces the forward bias voltage V_{BE}. Hence, base current reduces.

As I_{CBO} increases with temperature, IB decreases and hence IC remain fairly constant.

Sensistor Compensation:

This method of transistor compensation uses sensistor, which is temperature sensitive resistive element.





If the temperature increases the sensistor resistance increases. It has positive temperature co-efficient. As the temperature increases RT increases which decreases the current flowing through it. hence the current through R2 reduces which reduces the voltage drop across it.

Thermal Runaway:

The collector current for the CE circuit is given by

$$I_C = \beta I_B + (1 + \beta) I_{C0}$$

The three variables in the equation, β, IB and ICO increase with rise in temperature. In particular, the reverse saturation current (or) leakage current ICO changes greatly with temperature. Specifically, it doubles for every 10°C rise in temperature.

The collector current IC causes the collector-base junction temperature to rise which, in turn, increase ICO, as a result IC increase still further, which will further rise the temperature at the collector-base junction. This process is cumulative and it is referred to as self heating.

The excess heat produced at the collector-base junction may even burn and destroy the transistor. This situation is called “Thermal Runaway” of the transistor.

Thermal Resistance:

Transistor is a temperature dependent device. In order to keep the temperature within the

limits, the heat generated must be dissipated to the surroundings.

Most of the heat within the transistor is produced at the collector junction. If the temperature exceeds the permissible limit, the junction is destroyed. For Silicon transistor, the temperature is in the range 150^{o}C to225^{o}C. For Germanium, it is between 60^{o}C to 100^{o}C.

Let TA^{o}C be the ambient temperature i.e., the temperature of surroundings air around transistor and Tj^{o}C, the temperature of collector-base junction of the transistor.

Let PD be the power in watt dissipated at the collector junction.

The steady state temperature rise at the collector junction is proportional to the power dissipated at the junction. It is given by

$$\partial T = \partial T_J - \partial T_A = \theta$$

where θ is proportionality constant

$$\theta = \frac{T_J - T_A}{P_D}$$

The unit of θ, the thermal resistance, is ^{o}C/watt.

The typical values of θ for various transistors vary from 0.2^{o}C/watt for a high power transistor to 1000 ^{o}C/watt for a low power transistor.

Heat Sink:

As power transistors handle large currents, they always heat up during operation The metal sheet that helps to dissipate the additional heat from the transistor is known a *HEAT SINK*. The heat sink avoids the undesirable thermal effect such as thermal runaway.

The ability of heat sink depends on the material used, volume, area, shape, constant between case and sink and movement of air around the sink.

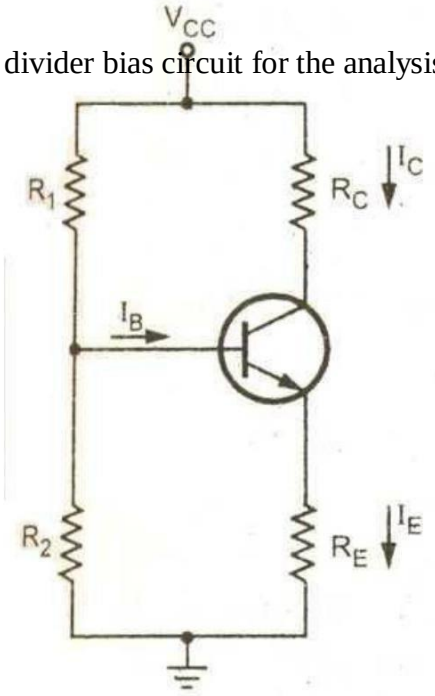
The condition for Thermal Stability:

As we know, the thermal runaway may even burn and destroy the transistor, it is necessary to avoid thermal runaway.

The required condition to avoid thermal runaway is that the rate at which heat is

released at the collector junction must not exceed the rate at which the heat can be condition.

Let us consider voltage divider bias circuit for the analysis.



From the fig pc is the power generated at the collector = dc power generated in the circuit-the maximum power losses in I^2R in across RE and RC.

If we consider ic=ie

$$PC = V_{CC}I_C - I_C^2(R_C + R_E)$$

Differentiating the above eq w.r.t to IC

$$\frac{\partial P_C}{\partial I_C} = V_{CC} - 2I_C(R_C + R_E) \text{.....(7)}$$

From eq (4) we can write

$$\frac{\partial P_C}{\partial I_C} \cdot \frac{\partial I_C}{\partial T_J} < \frac{1}{\theta}$$

in the above eq $\frac{\partial I_C}{\partial T_J}$ is written as

$$\frac{\partial I_C}{\partial T_J} = S\frac{\partial I_{C0}}{\partial T_J} + S'\frac{\partial V_{BE}}{\partial T_J} + S''\frac{\partial \beta}{\partial T_J}$$

Since junction current effects collector current by I_{CO} V_{BE} & β, among these three

the collector current mostly effected by I_{CO} therefore the above eq becomes

$$\frac{\partial I_C}{\partial T_J} = S\frac{\partial I_{C0}}{\partial T_J}$$

As the reverse saturation current increases for both ge.si is 7% per centigrade degree,we can write

$$\frac{\partial I_{C0}}{\partial T_J} = 0.07 I_{C0}$$

$$\frac{\partial I_{CO}}{\partial T_J} = s * 0.07 I_{C0} \text{ ……..(12)}$$

Substituting eq 12 in eq 7 we get

$$\frac{\partial P_C}{\partial I_C} = V_{CC} - 2I_C(R_C + R_E) * s * 0.07 I_{C0} \text{ ……(13)}$$

$$\frac{V_{CC}}{2} < I_C(R_C + R_E) \text{ … … … … (14)}$$

Applying kvl to the voltage divider bias circuit

$$V_{CC} = V_{CE} - I_C(R_C + R_E)$$

$$I_C(R_C + R_E) = V_{CC} - V_{CE}$$

substituting $I_C(R_C + R_E)$ IN EQ 14

$$\frac{V_{CC}}{2} < V_{CC} - V_{CE}$$

$$V_{CE} < V_{CC} - \frac{V_{CC}}{2}$$

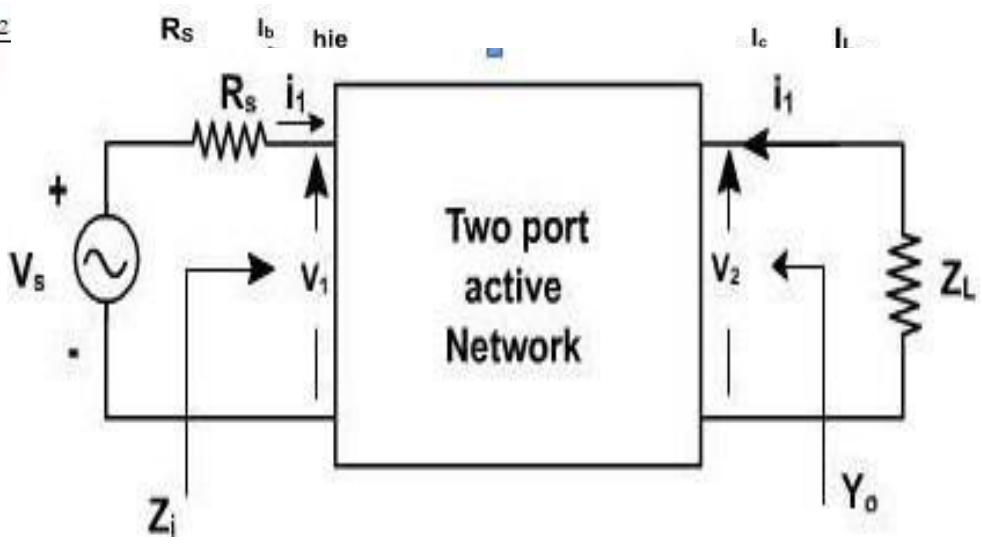
the above eq becomes

$V_{CE} < \frac{V_{CC}}{2}$ this is the required condition to satisfy to avoid the thermal runaway

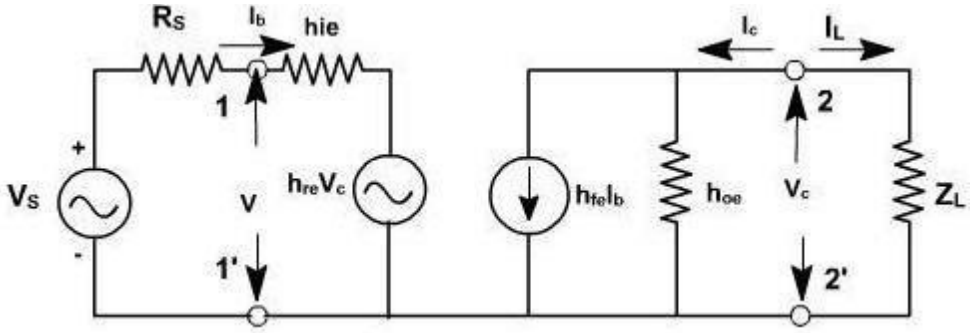
ANALYSIS OF A TRANSISTOR AMPLIFIER USING H-PARAMETERS:

To form a transistor amplifier it is only necessary to connect an external load and signal source as indicated in fig. and to bias the transistor properly

$A_I = \frac{I_L}{I_1} = \frac{-I_2}{I_1}$



Consider the two-port network of CE amplifier. R_S is the source resistance and Z_L is the load impedance h-parameters are assumed to be constant over the operating range. The ac equivalent circuit is shown in fig. 2. (Phasor notations are used assuming sinusoidal voltage input). The quantities of interest are the current gain, input impedance, voltage gain, and output impedance.



Current gain:

For the transistor amplifier stage, A_i is defined as the ratio of output to input currents.

$$A_{I=} \frac{I_L}{I_1} = \frac{-I_2}{I_1}$$

We know

$$V_{BE} = h_{ie} i_b + hre_{vce} \ldots\ldots\ldots\ldots\ldots\ldots (1)$$

$$i_c = h_{fe} i_b + h_{oe} v_{ce} \ldots\ldots\ldots\ldots\ldots (2)$$

From the fig $A_{I=}\ \frac{-i_c}{i_b}$ according to this we have to consider h parameter second eq i.e;

$$i_c = h_{fe} i_b + h_{oe} v_{ce}$$

From the fig $v_{ce} = -i_c R_L$ subsitute this value in above eq

$$i_c = h_{fe} i_b + h_{oe} - i_c R_L$$

$$i_c + i_c R_L h_{oe} = h_{fe} i_b$$

$$i_c(1 + R_L h_{oe}) = h_{fe} i_b$$

$\frac{i_c}{i_b} = \frac{h_{fe}}{(1+R_L h_{oe})}$ but we know $A_{I=}\ \frac{-i_c}{i_b}$

Therefore the above eq becomes $\frac{i_c}{i_b} = \frac{-h_{fe}}{(1+R_L h_{oe})}$

For CE transistor configuration

Vbe = hie Ib + hre Vce

Ic = h fe Ib + hoe Vce

The circuit can be redrawn like CC transistor configuration

Vbc = hie Ib + hrc Vec

Ic = hfe Ib + hoe Vec

UNIT 5

FIELD EFFECT TRANSISTOR

UNIT 5

FIELD EFFECT TRANSISTOR

5.1 INTRODUCTION

1. The Field effect transistor is abbreviated as FET , it is an another semiconductor device like a BJT which can be used as an amplifier or switch.
2. The Field effect transistor is a voltage operated device. Whereas Bipolar junction transistor is a current controlled device. Unlike BJT a FET requires virtually no input current.
3. This gives it an extremely high input resistance , which is its most important advantage over a bipolar transistor.
4. FET is also a three terminal device, labeled as source, drain and gate.
5. The source can be viewed as BJT's emitter, the drain as collector, and the gate as the counter part of the base.
6. The material that connects the source to drain is referred to as the channel.
7. FET operation depends only on the flow of majority carriers ,therefore they are called uni polar devices. BJT operation depends on both minority and majority carriers.
8. As FET has conduction through only majority carriers it is less noisy than BJT.
9. FETs are much easier to fabricate and are particularly suitable for ICs because they occupy less space than BJTs.
10. FET amplifiers have low gain bandwidth product due to the junction capacitive effects and produce more signal distortion except for small signal operation.
11. The performance of FET is relatively unaffected by ambient temperature changes. As it has a negative temperature coefficient at high current levels, it prevents the FET from thermal breakdown. The BJT has a positive temperature coefficient at high current levels which leads to thermal breakdown.

CLASSIFICATION OF FET:

There are two major categories of field effect transistors:

1. Junction Field Effect Transistors

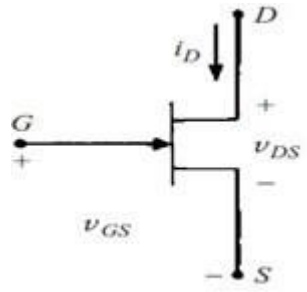
2. MOSFETs

These are further sub divided in to P- channel and N-channel devices.

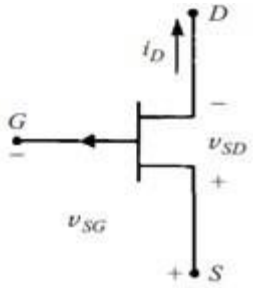
MOSFETs are further classified in to two types Depletion MOSFETs and Enhancement . MOSFETs

When the channel is of N-type the JFET is referred to as an N-channel JFET ,when the channel is of P-type the JFET is referred to as P-channel JFET.

The schematic symbols for the P-channel and N-channel JFETs are shown in the figure.



N-channel FET

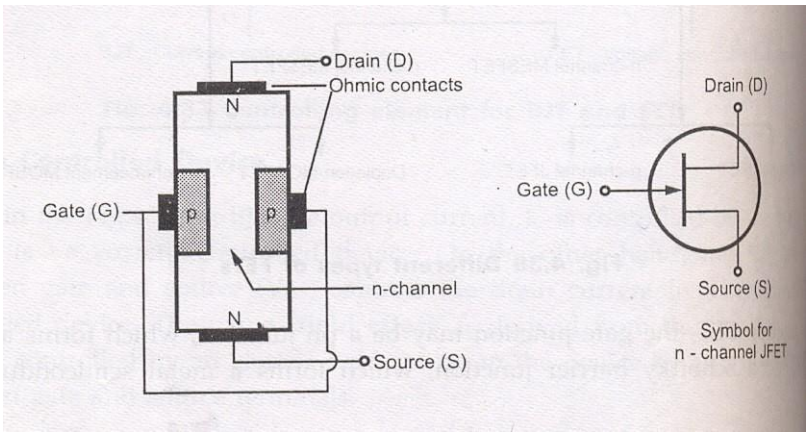


P-channel FET

CONSTRUCTION AND OPERATION OF N- CHANNEL FET

If the gate is an N-type material, the channel must be a P-type material.

CONSTRUCTION OF N-CHANNEL JFET



A piece of N- type material, referred to as channel has two smaller pieces of P-type material attached to its sides, forming PN junctions. The channel ends are designated as the drain and source. And the two pieces of P-type material are connected together and their terminal is called the gate. Since this channel is in the N-type bar, the FET is known as N-channel JFET.

OPERATION OF N-CHANNEL JFET:-

The overall operation of the JFET is based on varying the width of the channel to control the drain current.

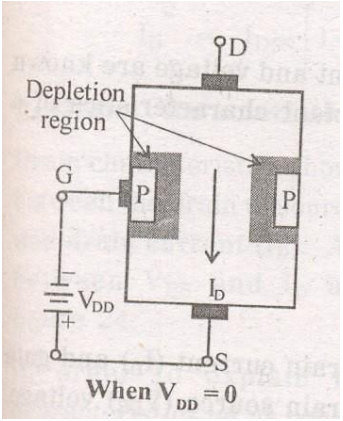
A piece of N type material referred to as the channel, has two smaller pieces of P type material attached to its sites, farming PN –Junctions. The channel's ends are designated the drain and the source. And the two pieces of P type material are connected together and their terminal is called the gate. With the gate terminal not connected and the potential applied positive at the drain negative at the source a drain current Id flows. When the gate is biased negative with respective to the source the PN junctions are reverse biased and depletion regions are formed. The channel is more lightly doped than the P type gate blocks, so the depletion regions penetrate deeply into the channel. Since depletion region is a region depleted of charge carriers it behaves as an Insulator. The result is that the channel is narrowed. Its resistance is increased and Id is reduced. When the negative gate bias voltage is further increased, the depletion regions meet at the center and Id is cut off completely.

There are two ways to control the channel width

1. By varying the value of Vgs
2. And by Varying the value of Vds holding Vgs constant

1 By varying the value of Vgs :-

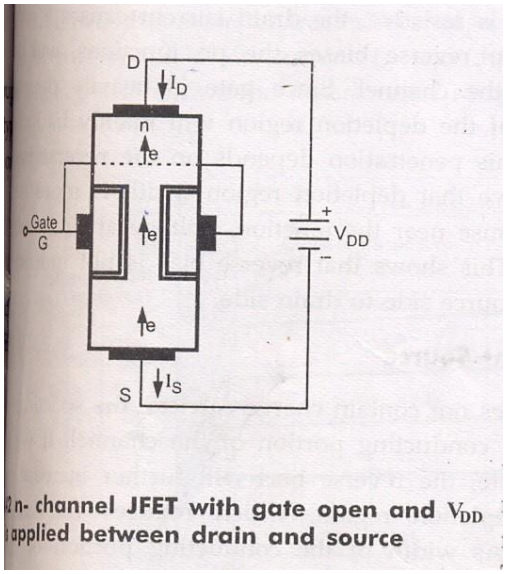
We can vary the width of the channel and in turn vary the amount of drain current. This can be done by varying the value of Vgs. This point is illustrated in the fig below. Here we are dealing with N channel FET. So channel is of N type and gate is of P type that constitutes a PN junction. This PN junction is always reverse biased in JFET operation .The reverse bias is applied by a battery voltage Vgs connected between the gate and the source terminal i.e positive terminal of the battery is connected to the source and negative terminal to gate.



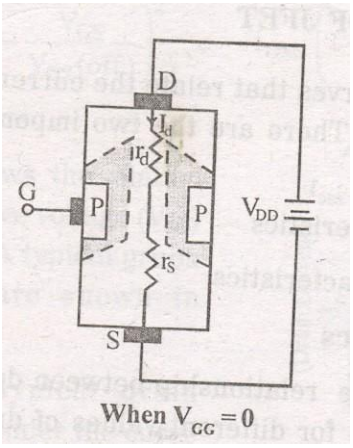
1) When a PN junction is reverse biased the electrons and holes diffuse across junction by leaving immobile ions on the N and P sides , the region containing these immobile ions is known as depletion regions.
2) If both P and N regions are heavily doped then the depletion region extends symmetrically on both sides.
3) But in N channel FET P region is heavily doped than N type thus depletion region extends more in N region than P region.
4) So when no Vds is applied the depletion region is symmetrical and the conductivity becomes Zero. Since there are no mobile carriers in the junction.
5) As the reverse bias voltage is increases the thickness of the depletion region also increases. i.e. the effective channel width decreases .
6) By varying the value of Vgs we can vary the width of the channel.

2 Varying the value of Vds holding Vgs constant :-

1) When no voltage is applied to the gate i.e. Vgs=0 , Vds is applied between source and drain the electrons will flow from source to drain through the channel constituting drain current Id .
2) With Vgs= 0 for Id= 0 the channel between the gate junctions is entirely open .In response to a small applied voltage Vds , the entire bar acts as a simple semi conductor resistor and the current Id increases linearly with Vds .
3) The channel resistances are represented as rd and rs as shown in the fig.



n- channel JFET with gate open and V_{DD} applied between drain and source



When $V_{GG} = 0$

4) This increasing drain current Id produces a voltage drop across rd which reverse biases the gate to source junction,(rd> rs) .Thus the depletion region is formed which is not symmetrical .
5) The depletion region i.e. developed penetrates deeper in to the channel near drain and less towards source because Vrd >> Vrs. So reverse bias is higher near drain than at source.
6) As a result growing depletion region reduces the effective width of the channel. Eventually a voltage Vds is reached at which the channel is pinched off. This is the voltage where the current Id begins to level off and approach a constant value.
7) So, by varying the value of Vds we can vary the width of the channel holding Vgs constant.

When both Vgs and Vds is applied:-

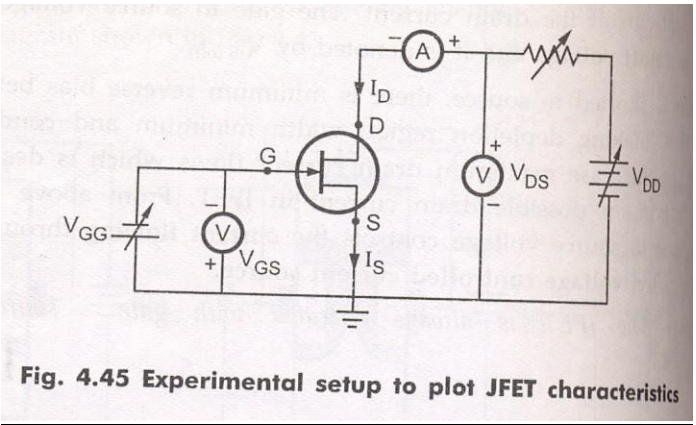
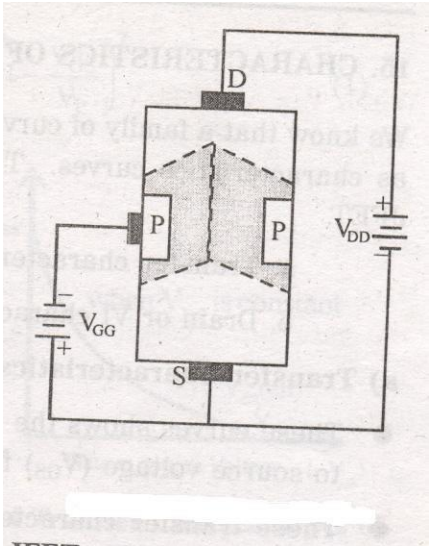


Fig. 4.45 Experimental setup to plot JFET characteristics

It is of course in principle not possible for the channel to close Completely and there by reduce the current Id to Zero for, if such indeed, could be the case the gate voltage Vgs is applied in the direction to provide additional reverse bias

1) When voltage is applied between the drain and source with a battery Vdd, the electrons flow from source to drain through the narrow channel existing between the depletion regions. This constitutes the drain current Id, its conventional direction is from drain to source.
2) The value of drain current is maximum when no external voltage is applied between gate and source and is designated by Idss.



3) When Vgs is increased beyond Zero the depletion regions are widened. This reduces the effective width of the channel and therefore controls the flow of drain current through the channel.
4) When Vgs is further increased a stage is reached at which to depletion regions touch each other that means the entire channel is closed with depletion region. This reduces the drain current to Zero.

CHARACTERISTICS OF N-CHANNEL JFET:-

The family of curves that shows the relation between current and voltage are known as characteristic curves.

There are two important characteristics of a JFET.

1) Drain or VI Characteristics
2) Transfer characteristics

1. Drain Characteristics:-

Drain characteristics shows the relation between the drain to source voltage Vds and drain current Id. In order to explain typical drain characteristics let us consider the curve with Vgs= 0.V.

1) When Vds is applied and it is increasing the drain current ID also increases linearly up to knee point.
2) This shows that FET behaves like an ordinary resistor.This region is called as ohmic region.

3) ID increases with increase in drain to source voltage. Here the drain current is increased slowly as compared to ohmic region.

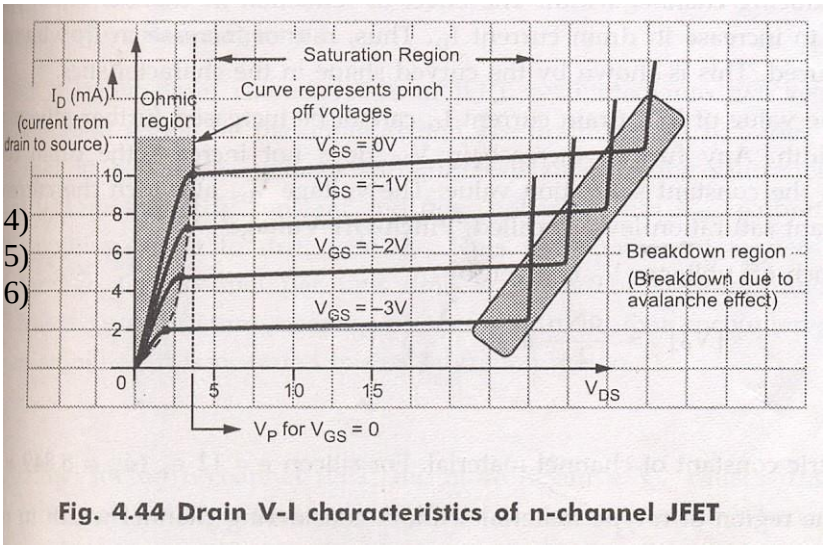


Fig. 4.44 Drain V-I characteristics of n-channel JFET

4)
5)
6)

4) It is because of the fact that there is an increase in VDS .This in turn increases the reverse bias voltage across the gate source junction .As a result of this depletion region grows in size thereby reducing the effective width of the channel.

5) All the drain to source voltage corresponding to point the channel width is reduced to a minimum value and is known as pinch off.

6) The drain to source voltage at which channel pinch off occurs is called pinch off voltage(Vp).

PINCH OFF Region:-

1) This is the region shown by the curve as saturation region.
2) It is also called as saturation region or constant current region. Because of the channel is occupied with depletion region , the depletion region is more towards the drain and less towards the source, so the channel is limited, with this only limited number of carriers are only allowed to cross this channel from source drain causing a current that is constant in this region. To use FET as an amplifier it is operated in this saturation region.
3) In this drain current remains constant at its maximum value IDSS.

4) The drain current in the pinch off region depends upon the gate to source voltage and is given by the relation

$$I_d = I_{dss} [1-V_{gs/Vp}]^2$$

This is known as shokley's relation.

BREAKDOWN REGION:-

1) The region is shown by the curve .In this region, the drain current increases rapidly as the drain to source voltage is increased.
2) It is because of the gate to source junction due to avalanche effect.
3) The avalanche break down occurs at progressively lower value of VDS because the reverse bias gate voltage adds to the drain voltage thereby increasing effective voltage across the gate junction
   This causes
   1. The maximum saturation drain current is smaller
   2. The ohmic region portion decreased.
4) It is important to note that the maximum voltage VDS which can be applied to FET is the lowest voltage which causes available break down.

2. TRANSFER CHARACTERISTICS:-

These curves shows the relationship between drain current ID and gate to source voltage VGS for different values of VDS.

1) First adjust the drain to source voltage to some suitable value , then increase the gate to source voltage in small suitable value.
2) Plot the graph between gate to source voltage along the horizontal axis and current ID on the vertical axis. We shall obtain a curve like this.

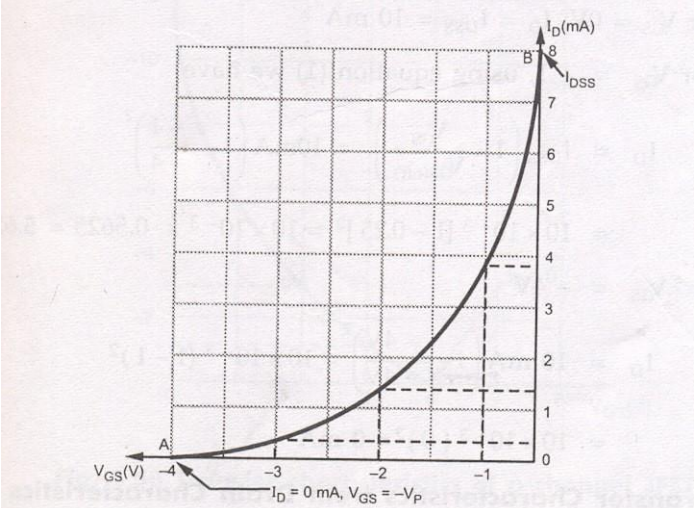


Fig. 4.48 Transfer characteristics of n-channel JFET

3) As we know that if V_{gs} is more negative curves drain current to reduce . where V_{gs} is made sufficiently negative, I_d is reduced to zero. This is caused by the widening of the depletion region to a point where it is completely closes the channel. The value of V_{gs} at the cutoff point is designed as V_{gsoff}

4) The upper end of the curve as shown by the drain current value is equal to I_{dss} that is when V_{gs} = 0 the drain current is maximum.

5) While the lower end is indicated by a voltage equal to V_{gsoff}
6) If Vg_s continuously increasing , the channel width is reduced , then I_d =0
7) It may be noted that curve is part of the parabola; it may be expressed as $I_d=I_{dss}[1-V_{gs}/V_{gsoff}]^2$

DIFFERENCE BETWEEN V_p AND V_{gsoff} –

Vp is the value of V_{gs} that causes the JFET to become constant current component, It is measured at V_{gs} =0V and has a constant drain current of I_d =I_{dss} .Where V_{gsoff} is the value of V_{gs} that reduces I_d to approximately zero.

Why the gate to source junction of a JFET be always reverse biased ?

The gate to source junction of a JFET is never allowed to become forward biased because the gate material is not designed to handle any significant amount of current. If the junction is allowed to become forward biased, current is generated through the gate material. This current may destroy the component.

There is one more important characteristic of JFET reverse biasing i.e. J FET ‘s have extremely high characteristic gate input impedance. This impedance is typically in the high mega ohm range. With the advantage of extremely high input impedance it draws no current from the source. The high input impedance of the JFET has led to its extensive use in integrated circuits. The low current requirements of the component makes it perfect for use in ICs. Where thousands of transistors must be etched on to a single piece of silicon. The low current draw helps the IC to remain relatively cool, thus allowing more components to be placed in a smaller physical area.

JFET PARAMETERS

The electrical behavior of JFET may be described in terms of certain parameters. Such parameters are obtained from the characteristic curves.

A C Drain resistance(r_d):

It is also called dynamic drain resistance and is the a.c.resistance between the drain and source terminal,when the JFET is operating in the pinch off or saturation region.It is given by the ratio of small change in drain to source voltage ΔV_{ds} to the corresponding change in drain current ΔI_d for a constant gate to source voltage $V_{gs.}$

Mathematically it is expressed as $r_d=\Delta V_{ds/} \Delta I_d$ where V_{gs} is held constant.

TRANCE CONDUCTANCE (g_m):

It is also called forward transconductance . It is given by the ratio of small change in drain current (ΔI_d) to the corresponding change in gate to source voltage (ΔV_{ds})

Mathematically the transconductance can be written as

$$g_m=\Delta I_{d/}\Delta V_{ds}$$

AMPLIFICATION FACTOR (μ)

It is given by the ratio of small change in drain to source voltage (ΔV_{ds}) to the corresponding change in gate to source voltage (ΔV_{gs})for a constant drain current (I_d).

Thus $\mu=\Delta V_{ds}/\Delta V_{gs}$ when I_d held constant

The amplification factor μ may be expressed as a product of transconductance (g_m)and ac drain resistance (r_d)

$\mu=\Delta V_{ds}/\Delta V_{gs}=g_m\ r_d$

THE FET SMALL SIGNAL MODEL:-

The linear small signal equivalent circuit for the FET can be obtained in a manner similar to that used to derive the corresponding model for a transistor.

We can express the drain current iD as a function f of the gate voltage and drain voltage V_{ds}.

$I_d = f(V_{gs}, V_{ds})$ ---------- (1)

The transconductance g_m and drain resistance r_d:-

If both gate voltage and drain voltage are varied, the change in the drain current is approximated by using taylors series considering only the first two terms in the expansion

$$\Delta i_d = \frac{\partial id}{\partial V_{gs}}|v_{ds}=\text{constant} \cdot \Delta v_{gs} + \frac{\partial id}{\partial V_{ds}}|vgs=\text{constant} \Delta v_{ds}$$

we can write $\Delta i_d = i_d$

$\Delta v_{gs} = v_{gs}$

$\Delta v_{ds} = v_{ds}$

$$I_d = g_m v_{gs} + \frac{1}{r_d} \text{ Vds} \rightarrow (1)$$

Where $g_m = \frac{\partial id}{\partial V_{gs}}|\text{Vds} \cong \frac{\Delta id}{\Delta V_{gs}}|\text{Vds}$

$$g_m = \frac{id}{Vgs}|\text{Vds}$$

Is the mutual conductance or transconductance .It is also called as gfs or yfs common source forward conductance .

The second parameter r_d is the drain resistance or output resistance is defined as

$$r_d = \frac{\partial Vds}{\partial id}|_{Vgs} \cong \frac{\Delta vds}{\Delta ids}|_{Vgs} = \frac{Vds}{id}|_{Vgs}$$

$$r_d = \frac{Vds}{id}|_{Vgs}$$

The reciprocal of the rd is the drain conductance gd .It is also designated by Yos and Gos and called the common source output conductance . So the small signal equivalent circuit for FET can be drawn in two different ways.

1. small signal current –source model

2. small signal voltage-source model.

A small signal current –source model for FET in common source configuration can be drawn satisfying Eq→(1) as shown in the figure(a)

This low frequency model for FET has a Norton's output circuit with a dependent current generator whose magnitude is proportional to the gate-to –source voltage. The proportionality factor is the transconductance 'g_m'. The output resistance is 'r_d'. The input resistance between the gate and source is infinite, since it is assumed that the reverse biased gate draws no current. For the same reason the resistance between gate and drain is assumed to be infinite.

The small signal voltage-source model is shown in the figure(b).

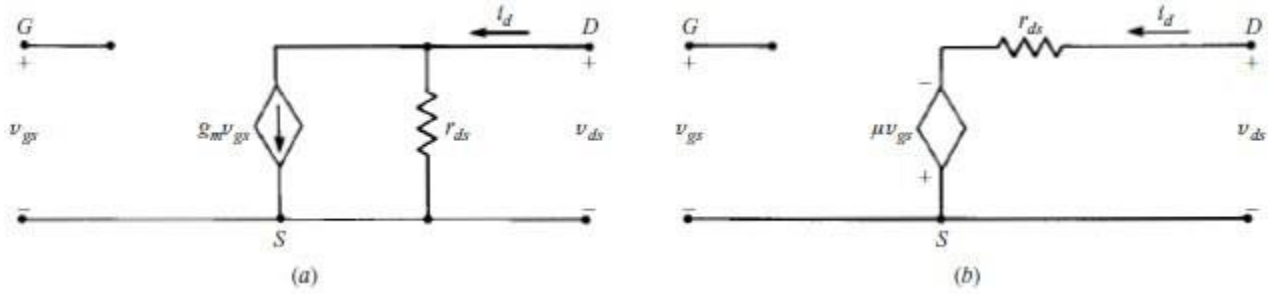
This can be derived by finding the Thevenin's equivalent for the output part of fig(a) .

These small signal models for FET can be used for analyzing the three basic FET amplifier configurations:

1.common source (CS) 2.common drain (CD) or source follower

3. common gate(CG).

(a)Small Signal Current source model for FET (b)Small Signal voltage source model for FET

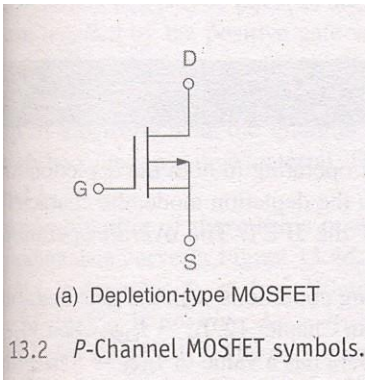


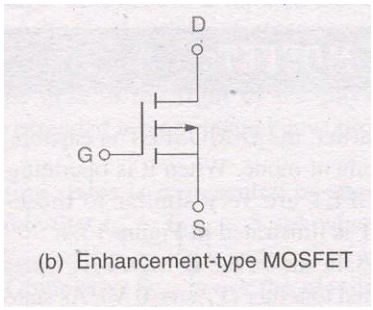
Here the input circuit is kept open because of having high input impedance and the output circuit satisfies the equation for ID

MOSFET:-

We now turn our attention to the insulated gate FET or metal oxide semi conductor FET which is having the greater commercial importance than the junction FET.

Most MOSFETS however are triodes, with the substrate internally connected to the source. The circuit symbols used by several manufacturers are indicated in the Fig below.





(a) Depletion type MOSFET (b) Enhancement type MOSFET

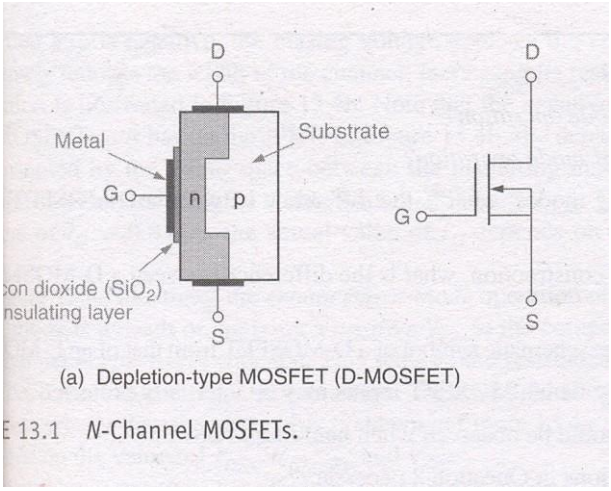
Both of them are P- channel

Here are two basic types of MOSFETS

(1) Depletion type (2) Enhancement type MOSFET.

D-MOSFETS can be operated in both the depletion mode and the enhancement mode. E MOSFETS are restricted to operate in enhancement mode. The primary difference between them is their physical construction.

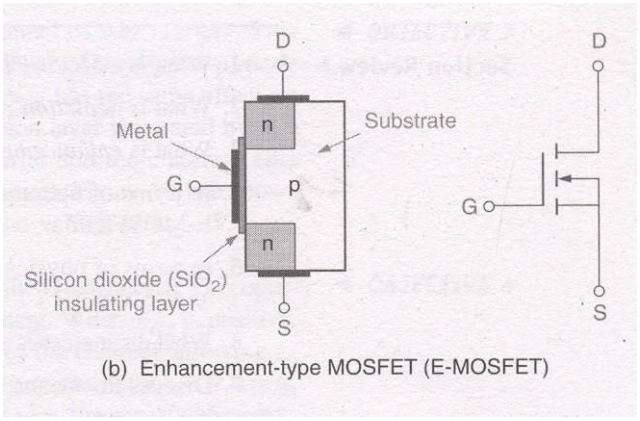
The construction difference between the two is shown in the fig given below.



(a) Depletion-type MOSFET (D-MOSFET)

E 13.1 *N*-Channel MOSFETs.

As we can see the D MOSFET have physical channel between the source and drain terminals(Shaded area)



(b) Enhancement-type MOSFET (E-MOSFET)

The E MOSFET on the other hand has no such channel physically. It depends on the gate voltage to form a channel between the source and the drain terminals.

Both MOSFETS have an insulating layer between the gate and the rest of the component. This insulating layer is made up of SIO_2 a glass like insulating material. The gate material is made up of metal conductor .Thus going from gate to substrate, we can have metal oxide semi conductor which is where the term MOSFET comes from.

Since the gate is insulated from the rest of the component, the MOSFET is sometimes referred to as an insulated gate FET or IGFET.

The foundation of the MOSFET is called the substrate. This material is represented in the schematic symbol by the center line that is connected to the source.

In the symbol for the MOSFET, the arrow is placed on the substrate. As with JFET an arrow pointing in represents an N-channel device, while an arrow pointing out represents p-channel device.

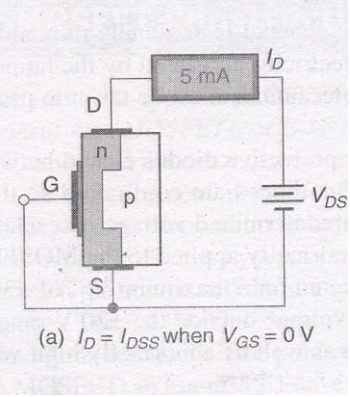
CONSTRUCTION OF AN N-CHANNEL MOSFET:-

The N- channel MOSFET consists of a lightly doped p type substance into which two heavily doped n+ regions are diffused as shown in the Fig. These n+ sections , which will act as source and drain. A thin layer of insulation silicon dioxide (SIO_2) is grown over the surface of the structure, and holes are cut into oxide layer, allowing contact with the source and drain. Then the gate metal area is overlaid on the oxide, covering the entire channel region.Metal contacts are made to drain and source and the contact to the metal over the channel area is the gate terminal.The metal area of the gate, in conjunction with the insulating dielectric oxide layer and the semiconductor channel, forms a parallel plate capacitor. The insulating layer of sio2

Is the reason why this device is called the insulated gate field effect transistor. This layer results in an extremely high input resistance (10 10 to 10power 15ohms) for MOSFET.

DEPLETION MOSFET

The basic structure of D –MOSFET is shown in the fig. An N-channel is diffused between source and drain with the device an appreciable drain current IDSS flows foe zero gate to source voltage, Vgs=0.



Depletion mode operation:-

1) The above fig shows the D-MOSFET operating conditions with gate and source terminals shorted together(VGS=0V)

2) At this stage ID= IDSS where VGS=0V, with this voltage VDS, an appreciable drain current IDSS flows.

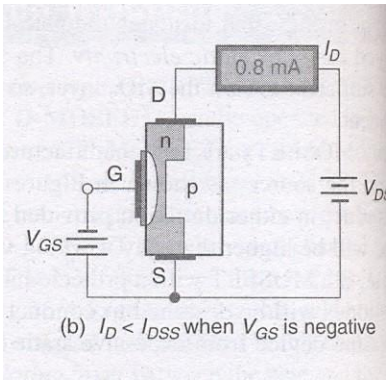
3) If the gate to source voltage is made negative i.e. VGs is negative .Positive charges are induced in the channel through the SIO2 of the gate capacitor.

4) Since the current in a FET is due to majority carriers(electrons for an N-type material) , the induced positive charges make the channel less conductive and the drain current drops as Vgs is made more negative.

5) The re distribution of charge in the channel causes an effective depletion of majority carriers , which accounts for the designation depletion MOSFET.

6) That means biasing voltage Vgs depletes the channel of free carriers This effectively reduces the width of the channel , increasing its resistance.

7) Note that negative Vgs has the same effect on the MOSFET as it has on the JFET.

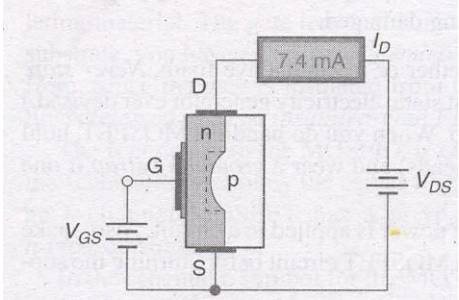


(b) $I_D < I_{DSS}$ when V_{GS} is negative

8) As shown in the fig above, the depletion layer generated by Vgs (represented by the white space between the insulating material and the channel) cuts into the channel, reducing its width. As a result ,Id<Idss.The actual value of ID depends on the value of Idss,Vgs(off) and Vgs.

Enhancement mode operation of the D-MOSFET:-

1) This operating mode is a result of applying a positive gate to source voltage Vgs to the device.
2) When Vgs is positive the channel is effectively widened. This reduces the resistance of the channel allowing ID to exceed the value of IDSS
3) When Vgs is given positive the majority carriers in the p-type are holes. The holes in the p type substrate are repelled by the +ve gate voltage.
4) At the same time, the conduction band electrons (minority carriers) in the p type material are attracted towards the channel by the +gate voltage.
5) With the build up of electrons near the channel , the area to the right of the physical channel effectively becomes an N type material.
6) The extended n type channel now allows more current, Id> Idss



(c) $I_D > I_{DSS}$ when V_{GS} is positive

FIGURE 13.4 D-MOSFET operation.

Characteristics of Depletion MOSFET:-

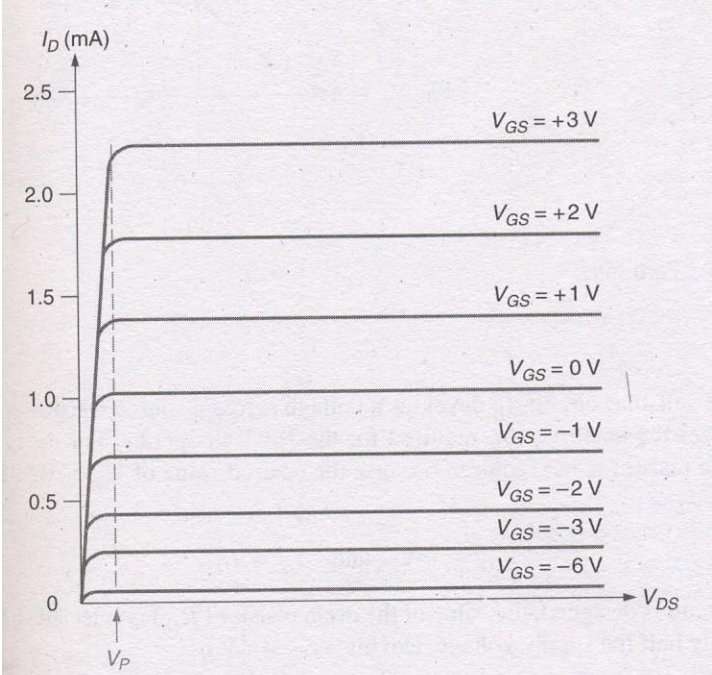
The fig. shows the drain characteristics for the N channel depletion type MOSFET

1) The curves are plotted for both Vgs positive and Vgs negative voltages
.
2) When Vgs=0 and negative the MOSFET operates in depletion mode when Vgs is positive ,the MOSFET operates in the enhancement mode.
3) The difference between JFET and D MOSFET is that JFET does not operate for positive values of Vgs.

4) When Vds=0, there is no conduction takes place between source to drain, if Vgs<0 and Vds>0 then Id increases linearly.

5) But as Vgs,0 induces positive charges holes in the channel, and controls the channel width. Thus the conduction between source to drain is maintained as constant, i.e. Id is constant.

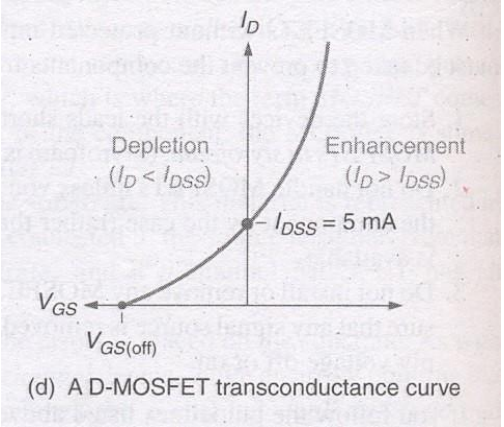
6) If Vgs>0 the gate induces more electrons in channel side, it is added with the free electrons generated by source. again the potential applied to gate determines the channel width and maintains constant current flow through it as shown in Fig



6 MOSFET drain curves.

TRANSFER CHARACTERISTICS:-

The combination of 3 operating states i.e. Vgs=0V, VGs<0V, Vgs>0V is represented by the D MOSFET transconductance curve shown in Fig.



(d) A D-MOSFET transconductance curve

1) Here in this curve it may be noted that the region AB of the characteristics similar to that of JFET.

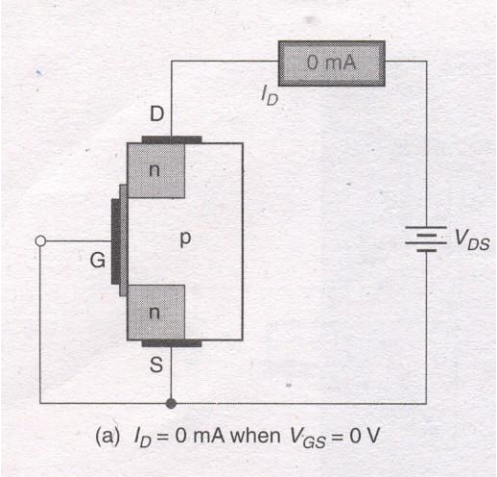
2) This curve extends for the positive values of Vgs

3) Note that Id=Idss for Vgs=0V when Vgs is negative,Id< Idss when Vgs= Vgs(off) ,Id is reduced to approximately omA.Where Vgs is positive Id>Idss.So obviously Idss is not the maximum possible value of Id for a MOSFET.

4) The curves are similar to JFET so thet the D MOSFET have the same transconductance equation.

E-MOSFETS

The E MOSFET is capable of operating only in the enhancement mode.The gate potential must be positive w.r.t to source.



(a) $I_D = 0$ mA when $V_{GS} = 0$ V

1) when the value of Vgs=0V, there is no channel connecting the source and drain materials.

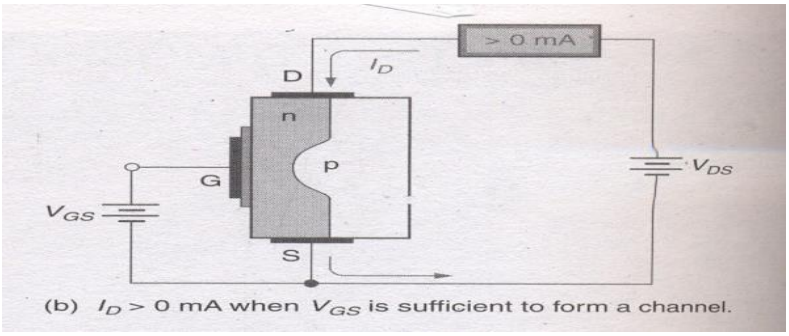
2) As aresult , there can be no significant amount of drain current.
3) When Vgs=0, the Vdd supply tries to force free electrons from source to drain but the presence of p-region does not permit the electrons to pass through it. Thus there is no drain current at Vgs=0,

4) If Vgs is positive, it induces a negative charge in the p type substrate just adjacent to the SIO2 layer.

5) As the holes are repelled by the positive gate voltage, the minority carrier electrons attracted toward this voltage. This forms an effective N type bridge between source and drain providing a path for drain current.

6) This +ve gate voltage forma a channel between the source and drain.

7) This produces a thin layer of N type channel in the P type substarate.This layer of free electrons is called N type inversion layer.



(b) $I_D > 0$ mA when V_{GS} is sufficient to form a channel.

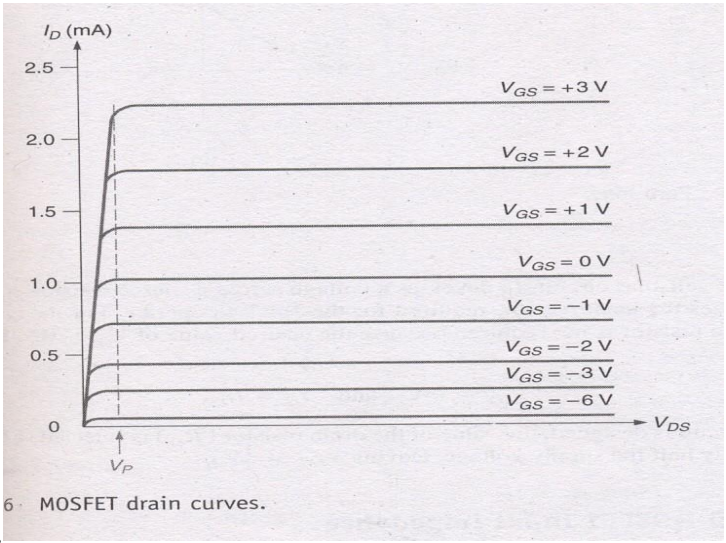
8) The minimum Vgs which produces this inversion layer is called threshold voltage and is designated by Vgs(th).This is the point at which the device turns on is called the threshold voltage Vgs(th)
9) When the voltage Vgs is <Vgs (th) no current flows from drain to source.

10) How ever when the voltage Vgs > Vgs (th) the inversion layer connects the drain to source and we get significant values of current.

CHARACTERISTICS OF E MOSFET:-

DRAIN CHARACTERISTICS

The volt ampere drain characteristics of an N-channel enhancement mode MOSFET are given in the fig.



6 MOSFET drain curves.

TRANSFER CHARACTERISTICS:-

1) The current Idss at Vgs≤ 0 is very small beinf of the order of a few nano amps.
2) As Vgs is made +ve , the current Id increases slowly at forst, and then much more rapidly with an increase in Vgs.
3) The standard transconductance formula will not work for the E MOSFET.
4) To determine the value of ID at a given value of VGs we must use the following relation

$$Id = K[V_{gs} - V_{gs(Th)}]^2$$

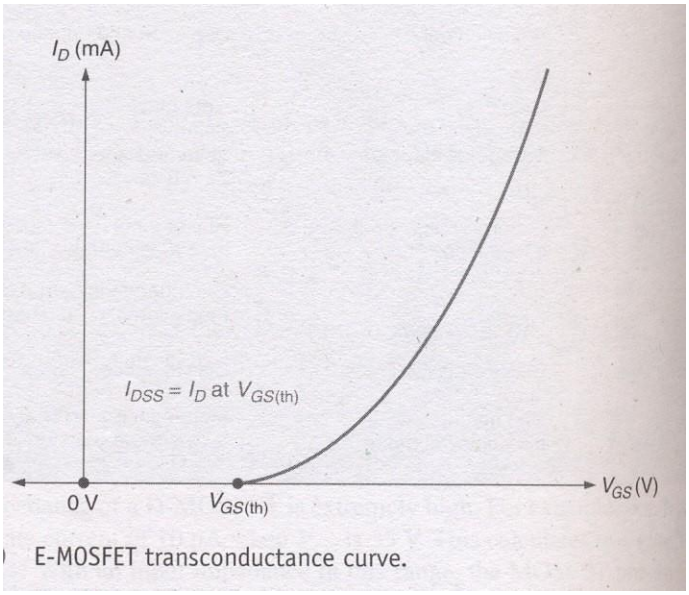
Where K is constant for the MOSFET . found as

$$K = \frac{Id(on)}{[vgs(on) - Vgs(Th)]2}$$

From the data specification sheets, the 2N7000 has the following ratings.

Id(on)= 75mA(minimum).

And Vgs(th)=0.8(minimum)



E-MOSFET transconductance curve.

APPLICATION OF MOSFET

One of the primary contributions to electronics made by MOSFETs can be found in the area of digital (computer electronics). The signals in digital circuits are made up of rapidly switching dc levels. This signal is called as a rectangular wave ,made up of two dc levels (or logic levels). These logic levels are 0V and +5V.

A group of circuits with similar circuitry and operating characteristics is referred to as a logic family. All the circuits in a given logic family respond to the same logic levels, have similar speed and power-handling capabilities , and can be directly connected together. One such logic family is complementary MOS (or CMOS) logic. This logic family is made up entirely of MOSFETs.

FET AMPLIFIERS

INTRODUCTION

Field Effect Transistor (FET) amplifiers provide an excellent voltage gain and high input impedence. Because of high input impedence and other characteristics of JFETs they are preferred over BJTs for certain types of applications.

There are 3 basic FET circuit configurations:

i) Common Source

ii) Common Drain

iii) Common Gain

Similar to BJT CE,CC and CB circuits, only difference is in BJT large output collector current is controlled by small input base current whereas FET controls output current by means of small input voltage. In both the cases output current is controlled variable.

FET amplifier circuits use voltage controlled nature of the JFET. In Pinch off region, I_D depends only on V_{GS}.

Common Source (CS) Amplifier

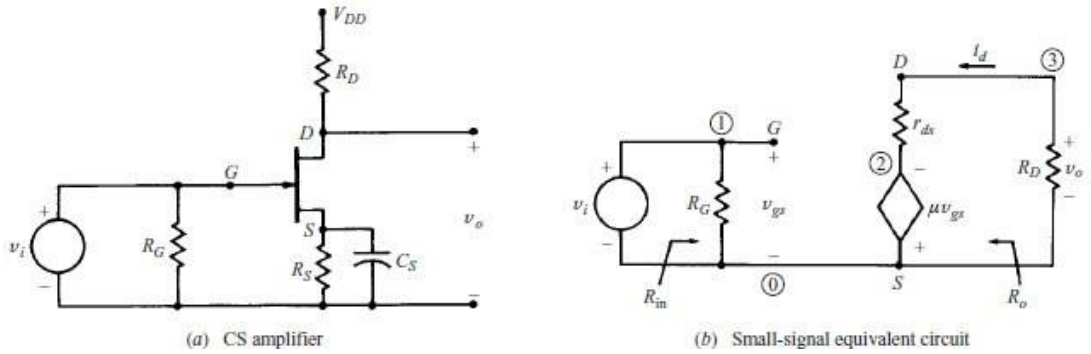


Fig. 7.1 (a) CS Amplifier (b) Small-signal equivalent circuit

A simple Common Source amplifier is shown in Fig. 7.1(a) and associated small signal equivalent circuit using voltage-source model of FET is shown in Fig. 7.1(b)

Voltage Gain

Source resistance (R_S) is used to set the Q-Point but is bypassed by C_S for mid-frequency operation. From the small signal equivalent circuit ,the output voltage

$$V_O = -R_D \mu V_{gs}(R_D + r_d)$$

Where $V_{gs} = V_i$, the input voltage,

Hence, the voltage gain,

$$A_V = V_O / V_i = -R_D \mu (R_D + r_d)$$

Input Impedence

From Fig. 7.1(b) Input Impedence is

$$Z_i = R_G$$

For voltage divider bias as in CE Amplifiers of BJT

$$R_G = R_1 \parallel R_2$$

Output Impedance

Output impedance is the impedance measured at the output terminals with the input voltage $V_I = 0$

From the Fig. 7.1(b) when the input voltage $V_i = 0$, $V_{gs} = 0$ and hence

$$\mu V_{gs} = 0$$

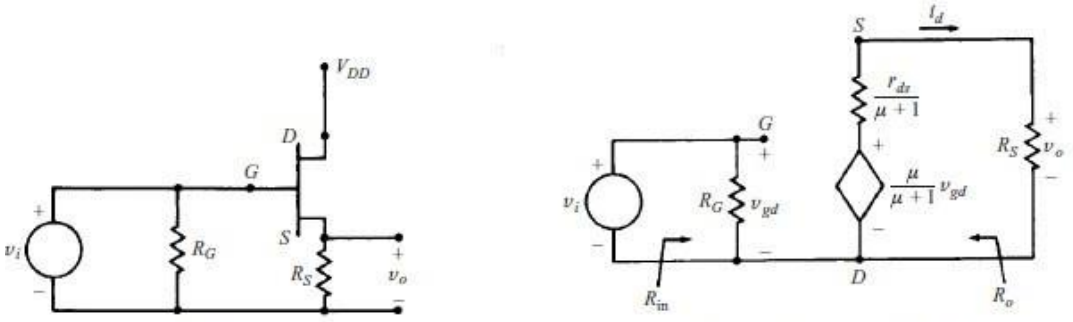
The equivalent circuit for calculating output impedence is given in Fig. 7.2.

Output impedence $Z_o = r_d \parallel R_D$

Normally r_d will be far greater than R_D . Hence $Z_o \approx R_D$

Common Drain Amplifier

A simple common drain amplifier is shown in Fig. 7.2(a) and associated small signal equivalent circuit using the voltage source model of FET is shown in Fig. 7.2(b).Since voltage V_{gd} is more easily determined than V_{gs}, the voltage source in the output circuit is expressed in terms of V_{gs} and Thevenin's theorem.



(a) CD or SF amplifier (b) Small-signal equivalent circuit

Fig. 7.2 (a)CD Amplifier (b)Small-signal equivalent circuit

Voltage Gain

The output voltage,

$$V_O = R_S \mu V_{gd} / (\mu + 1) R_S + r_d$$

Where $V_{gd} = V_i$ the input voltage.

Hence, the voltage gain,

$$A_v = V_O / V_i = R_S\mu / (\mu + 1) R_S + r_d$$

Input Impedence

From Fig. 7.2(b), Input Impedence $Z_i = R_G$

Output Impedence

From Fig. 7.2(b), Output impedence measured at the output terminals with input voltage $V_i = 0$ can be calculated from the following equivalent circuit.

As $V_i = 0$: $V_{gd} = 0$: $\mu v_{gd} / (\mu + 1) = 0$

Output Impedence

$$Z_O = r_d / (\mu + 1) \parallel R_S$$

When $\mu \gg 1$

$$Z_O = (r_d / \mu) \parallel R_S = (1/g_m) \parallel R_S$$

5.12 BIASING FET:-

For the proper functioning of a linear FET amplifier, it is necessary to maintain the operating point Q stable in the central portion of the pinch off region The Q point should be independent of device parameter variations and ambient temperature variations

This can be achieved by suitably selecting the gate to source voltage VGS and drain current ID which is referred to as biasing

JFET biasing circuits are very similar to BJT biasing circuits The main difference between JFET circuits and BJT circuits is the operation of the active components themselves

There are mainly two types of Biasing circuits

1. Self bias
2. Voltage divider bias.

SELF BIAS:-

Self bias is a JFET biasing circuit that uses a source resistor to help reverse bias the JFET gate.

A self bias circuit is shown in the fig 7.3

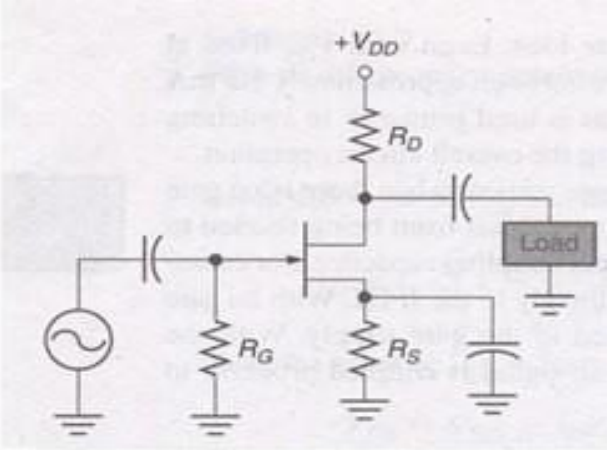


fig 7.3

Self bias is the most common type of JFET bias. This JFET must be operated such that gate source junction is always reverse biased. This condition requires a negative VGS for an N channel JFET and a positive VGS for P channel JFET. This can be achieved using the self bias arrangement as shown in Fig 7.3. The gate resistor RG doesn't affect the bias because it has essentially no voltage drop across it, and : the gate remains at 0V .RG is necessary only to isolate an ac signal from ground in amplifier applications. The voltage drop across resistor RS makes gate source junction reverse biased.

DC analysis of self Bias:-

In the following DC analysis , the N channel J FET shown in the fig7.4. is used for illustration.

For DC analysis we can replace coupling capacitors by open circuits and we can also replace the resistor RG by a short circuit equivalent.

:. IG = 0

The relation between ID and VGS is given by

$$Id=Idss[1-\frac{Vgs}{Vp}]^2$$

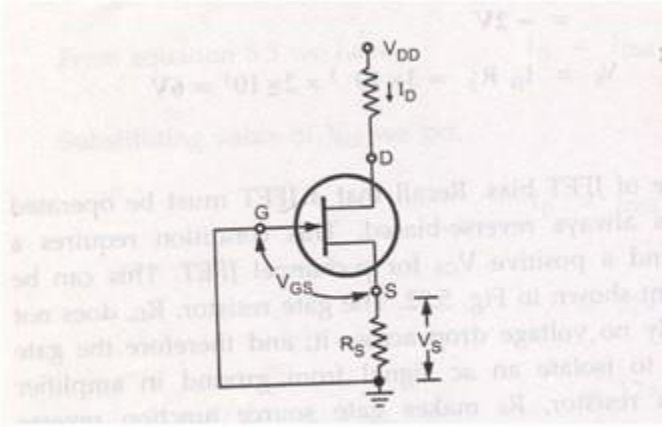


fig 7.4

VGS for N channel JFET is =-id Rs

Substuting this value in the above equation

$$Id=Idss[1-\frac{(-IdRs)}{Vp}]^2$$

$$Id=Idss[1+\frac{(IdRs)}{Vp}]^2$$

For the N-chanel FET in the above figure

Is produces a voltage drop across Rs and makes the source positive w.r.t ground

in any JFET circuit all the source current passes through the device to drain circuit this is due to the fact that there is no significant gate current

therefore we can define source current as Is=Id and Vg=0 then

Vs= Is Rs =IdRs

Vgs=Vg-Vs=0-IdRs=-IdRs

Drawing the self bias line:-

Typical transfer characteristics for a self biased JFET are shown in the fig7.5.

The maximum drain current is 6mA and the gate source cut off voltage is -3V. This means the gate voltage has to be between 0 and -3V.

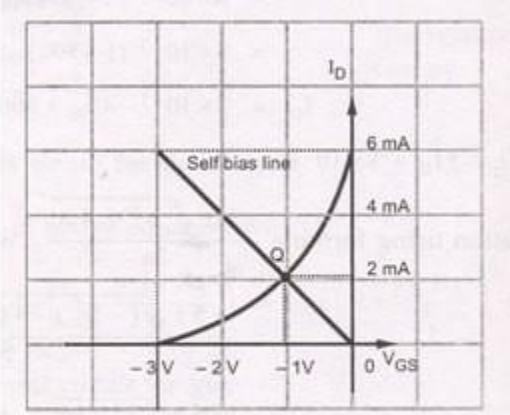


fig 7.5 Transfer characteristics

Now using the equation VGS = -IDRS and assuming RS of any suitable value we can draw the self bias line.

Let us assume RS = 500Ω

With this Rs , we can plot two points corresponding to ID = 0 and Id = IDSS

for ID = 0

VGS = -ID RS

VGS = 0X (500.Ω) = 0V

So the first point is (0 ,0)

(I_d, VGS)

For ID= IDSS=6mA

VGS = (-6mA) (500 Ω) = -3V

So the 2nd Point will be (6mA,-3V)

By plotting these two points, we can draw the straight line through the points. This line will intersect the transconductance curve and it is known as self bias line. The intersection point gives the operating point of the self bias JFET for the circuit.

At Q point , the ID is slightly > than 2mA and VGS is slightly > -1V. The Q point for the self bias JFET depends on the value of Rs.If Rs is large, Q point far down on the transconductance curve, ID is small, when Rs is small Q point is far up on the curve , ID is large.

VOLTAGE DIVIDER BIAS:-

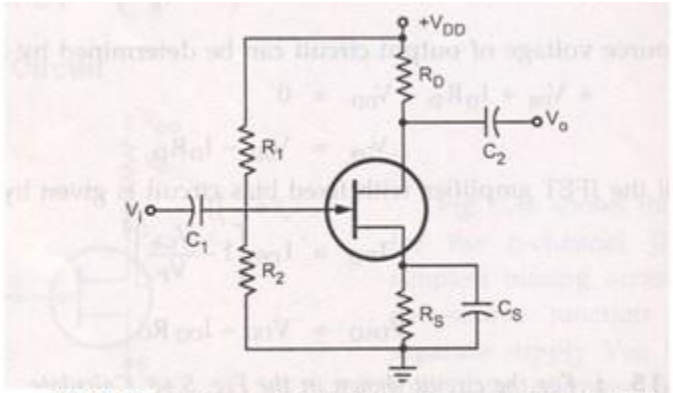


fig 7.6 **Voltage divider bias for n-channel JFET**

The fig7.6 shows N channel JFET with voltage divider bias. The voltage at the source of JFET must be more positive than the voltage at the gate in order to keep the gate to source junction reverse biased. The source voltage is

VS = IDRS

The gate voltage is set by resistors R1 and R2 as expressed by the following equation using the voltage divider formula.

$$Vg=\left(\frac{R2}{(R1+R2)}\right)Vdd$$

For dc analysis fig 7.7

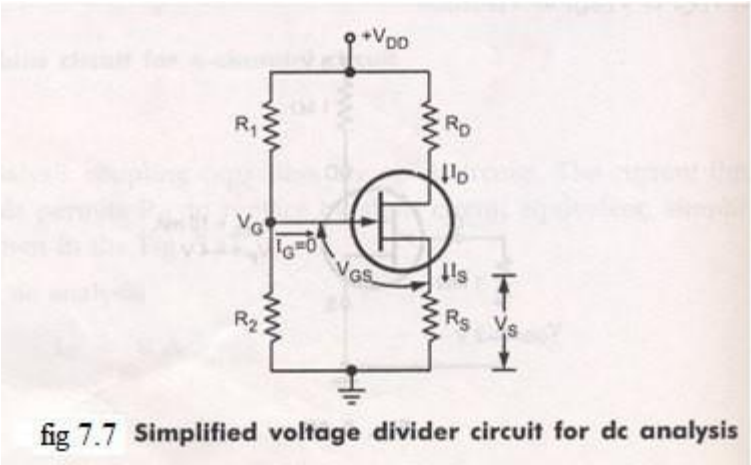


fig 7.7 **Simplified voltage divider circuit for dc analysis**

Applying KVL to the input circuit

VG-VGS-VS =0

:: VGS = VG-Vs=VG-ISRS

VGS = VG-IDRS :: IS = ID

Applying KVL to the input circuit we get

VDS+IDRD+VS-VDD =0

::VDS = VDD-IDRD-IDRS

VDS = VDD-ID (RD +RS)

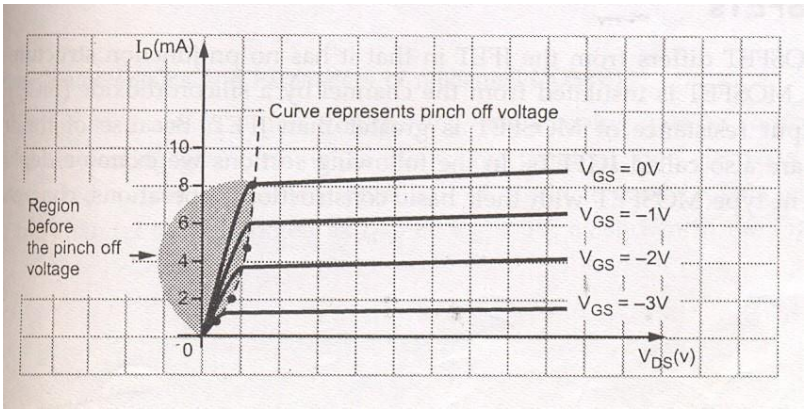
The Q point of a JFET amplifier , using the voltage divider bias is

IDQ = IDSS [1-VGS/VP]2

VDSQ = VDD-ID (RD+RS)

JFET AS A VVR OR VDR:-

Let us consider the drain characteristics of FET as shown in the fig.



In this characteristics we can see that in the region before pinch off voltage, drain characteristics are linear, i.e. FET operation is linear. In this region the FET is useful as a voltage controlled resistor,i.e. the drain to source resistance is controlled by the bias voltage VGS.(In this region only FET behaves like an ordinary resistor This resistances can be varied by VGS) .The operation of FET in the region is useful in most linear applications of FET.In such an application the FET is also referred to as a voltage variable resistor (VVR) or voltage dependent resistor (VDR).

The drain to source conductance (rd)

$g_d=\frac{Id}{Vd}$ for small values of VDS which may also be expressed as

$g_d=g_{d0}(1-(\frac{VGS}{Vp})^{1/2})$

Where g_{d0} is the value of drain conductance

When the variation of the rd with VGS can be closely approximated by the expression

$rd=(\frac{r0}{1-KVgs})$ Where ro = drain resistance at zero gate bias.K = a constant, dependent upon FET type

APPLICATION OF VVR

The VVR property of FET can be used to vary the voltage gain of a multistage amplifier A, as the signal level is increased. This action is called AGC automatic gain control. A typical arrangement is shown in the fig.

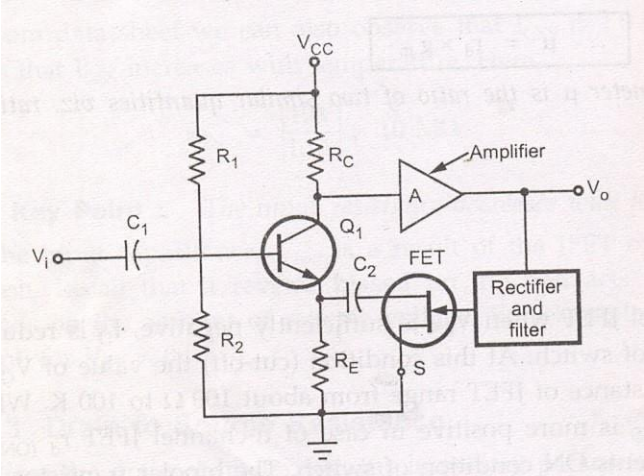


Fig. 4.54 AGC amplifier using FET as a voltage variable resistor

Here maximum value of signal is taken rectified; filter to produce a DC voltage proportional to the output signal level. This voltage is applied to the gate of JFET, this causing the resistance between drain and source to change. As this resistance is connected across RE, so effective RE also changes according to change in the drain to source resistance. When output signal level increases, the drain to source resistance rd increases, increasing effective RE. Increase in RE causes the gain of transistor Q1 to decrease, reducing the output signal. Exactly reverse process takes place when output signal level decreased.

:: The output signal level is maintained constant. It is to be noted that the DC bias conditions of Q1 are not affected by JFET since FET is isolated from Q1 by capacitor C2

Comparison of BJT & JFET

	JFET	BJT
1.	Unipolar device (current conduction is only due to one type of majority carrier either electron or hole).	Bipolar device (current condition, by both types of carriers, i.e., majority and minority-electrons and holes)
2.	The operation depends on the control of a junction depletion width under reverse bias.	The operation depends on the injection of minority carriers across a forward biased junction.
3.	Voltage driven device. The current through the two terminals is controlled by a voltage at the third terminal (gate).	Current driven device. The current through the two terminals is controlled by a current at the third terminal (base).
4.	Low noise level.	High noise level.
5.	High input impedance (due to reverse bias).	Low input impedance (due to forward bias).
6.	Gain is characterised by transconductance.	Gain is characterized by voltage gain.
7.	Better thermal stability.	Less thermal stability.